Product Change Notification / SYST-25GSAN503

Date:

26-Mar-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification Errata Document Revision

Affected CPNs:

SYST-25GSAN503_Affected_CPN_03262021.pdf
SYST-25GSAN503_Affected_CPN_03262021.csv

Notification Text:

SYST-25GSAN503

Microchip has released a new Product Documents for the PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Updated Table 2 and 37-1 and Section 4.1 Minimum VDD Specification. Other minor corrections.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 26 Mar 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F15356-E/ML
PIC16F15356-E/MV
PIC16F15356-E/SO
PIC16F15356-E/SP
PIC16F15356-E/SS
PIC16F15356-E/SSVAO
PIC16F15356-I/ML
PIC16F15356-I/MV
PIC16F15356-I/SO
PIC16F15356-I/SP
PIC16F15356-I/SS
PIC16F15356T-E/5NVAO
PIC16F15356T-E/MV
PIC16F15356T-E/SS
PIC16F15356T-E/SSV03
PIC16F15356T-E/SSVAO
PIC16F15356T-I/ML
PIC16F15356T-I/MV
PIC16F15356T-I/SO
PIC16F15356T-I/SS
PIC16F15356T-I/SSV01
PIC16F15356T-I/SSVAO
PIC16F15375-E/ML
PIC16F15375-E/MV
PIC16F15375-E/MVVAO
PIC16F15375-E/P
PIC16F15375-E/PT
PIC16F15375-I/ML
PIC16F15375-I/MV
PIC16F15375-I/P
PIC16F15375-I/PT
PIC16F15375T-E/PT
PIC16F15375T-E/PTVAO
PIC16F15375T-I/MV
PIC16F15375T-I/PT
PIC16F15376-E/ML
PIC16F15376-E/MV
PIC16F15376-E/P
PIC16F15376-E/PT
PIC16F15376-I/ML
PIC16F15376-I/MV
PIC16F15376-I/P
PIC16F15376-I/PT
PIC16F15376T-I/ML
PIC16F15376T-I/MV
PIC16F15376T-I/PT

PIC16F15376T-I/PTVAO
PIC16F15385-E/MV
PIC16F15385-E/PT
PIC16F15385-E/PTVAO
PIC16F15385-I/MV
PIC16F15385-I/PT
PIC16F15385-I/PTVAO
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PIC16F15386T-I/PT
PIC16LF15356-E/ML
PIC16LF15356-E/MV
PIC16LF15356-E/MVVAO
PIC16LF15356-E/SO
PIC16LF15356-E/SP
PIC16LF15356-E/SS
PIC16LF15356-I/ML
PIC16LF15356-I/MV
PIC16LF15356-I/SO
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PIC16LF15385-E/MV
PIC16LF15385-E/PT
PIC16LF15385-I/MV
PIC16LF15385-I/PT
PIC16LF15385T-E/MV
PIC16LF15385T-I/MV
PIC16LF15385T-I/PT
PIC16LF15386-E/MV
PIC16LF15386-E/PT
PIC16LF15386-E/PTVAO
PIC16LF15386-I/MV
PIC16LF15386-I/PT
PIC16LF15386T-I/MV
PIC16LF15386T-I/PT

PIC16(L)F15356/75/76/85/86

PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F15356/75/76/85/86 family devices that you have received conform functionally to the current Device Data Sheet (DS40001866**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F15356/75/76/85/86 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15356/75/76/85/86 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A1	A2
PIC16F15356	30B0h	2001h	2002h
PIC16LF15356	30B1h	2001h	2002h
PIC16F15375	30B2h	2001h	2002h
PIC16LF15375	30B3h	2001h	2002h
PIC16F15376	30B4h	2001h	2002h
PIC16LF15376	30B5h	2001h	2002h
PIC16F15385	30B6h	2001h	2002h
PIC16LF15385	30B7h	2001h	2002h
PIC16F15386	30B8h	2001h	2002h
PIC16LF15386	30B9h	2001h	2002h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F153XX Memory Programming Specification"* (DS40001838) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A1	A2
Analog-to-Digital Converter (ADC)	ADC Positive Voltage Reference	1.1	Using FVR as the positive voltage reference to the ADC can cause missing codes in the conversion result.	X	X
Development Support	Data Breakpoints	2.1	Data breakpoints are not available on Banks 32 through 63.	X	X
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	3.1	WWDT does not work with SOSC as the clock source.	X	X
Electrical Specifications	Minimum V_{DD} Specification for LF Devices	4.1	V_{DDMIN} specifications are changed for LF devices only.	X	X
	Fixed Voltage Reference (FVR) Accuracy	4.2	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X
	ADC Offset Error	4.3	ADC Offset Error specification changed.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Positive Voltage Reference

Using the FVR as the positive voltage reference to the ADC can cause an increase in missing codes.

Work around

1. Increase the bit conversion time, known as TAD, to 8 us.
2. Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Development Support

2.1 Data Breakpoints

Data breakpoints are not available on Banks 32 through 63. Any breakpoints that are placed in Banks 32 through 63 will fail to be recognized.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

3. Module: Windowed Watchdog Timer (WWDT)

3.1 WWDT Clock Source Selection

When the WDTCS <2:0> bits of the WDTCON1 register are set to 'b010', selecting the Secondary Oscillator SOSC 32 kHz, as the clock source, the WWDT does not operate.

Work around

Use the LFINTOSC or MFINTOSC clock sources for the WWDT.

Affected Silicon Revisions

A1	A2						
X	X						

4. Module: Electrical Specifications

4.1 Minimum VDD Specifications for LF Devices

VDDMIN at -40°C to +25°C = 2.3V. (See **TABLE 37-1: Supply Voltage** on the following page for reference.)

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4.3 ADC Offset Error

The table containing the Offset Error specification (AD04:EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSb.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

TABLE 37-1: SUPPLY VOLTAGE

PIC16LF15356/75/76/85/86			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D002	V_{DD}		1.8	—	3.6	V	$F_{OSC} \leq 16$ MHz, $+25°C \leq T_A \leq +125°C$
			2.3	—	3.6	V	$F_{OSC} \leq 16$ MHz, $-40°C \leq T_A \leq +25°C$
			2.5	—	3.6	V	$F_{OSC} > 16$ MHz

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001866**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Interrupt-On-Change (PORTE)

Bits <2:0> are unimplemented in registers IOCEP, IOCEN, and IOCEF, as indicated in the following register tables.

REGISTER 17-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	**U-0**	**U-0**	**U-0**
—	—	—	—	IOCEP3**(1)**	**—**	**—**	**—**
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bit
1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 Unimplemented: Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

REGISTER 17-11: IOCEN: INTERRUPT-ON-CHANGE PORTE NEGATIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	**U-0**	**U-0**	**U-0**
—	—	—	—	IOCEN3**(1)**	**—**	**—**	**—**
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEN:** Interrupt-on-Change PORTE Negative Edge Enable bit
1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 Unimplemented: Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

REGISTER 17-12: IOCEF: INTERRUPT-ON-CHANGE PORTE FLAG REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	**U-0**	**U-0**	**U-0**
—	—	—	—	IOCEP3(1)	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEF:** Interrupt-on-Change PORTE Flag bit
1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change

bit 2-0 Unimplemented: Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

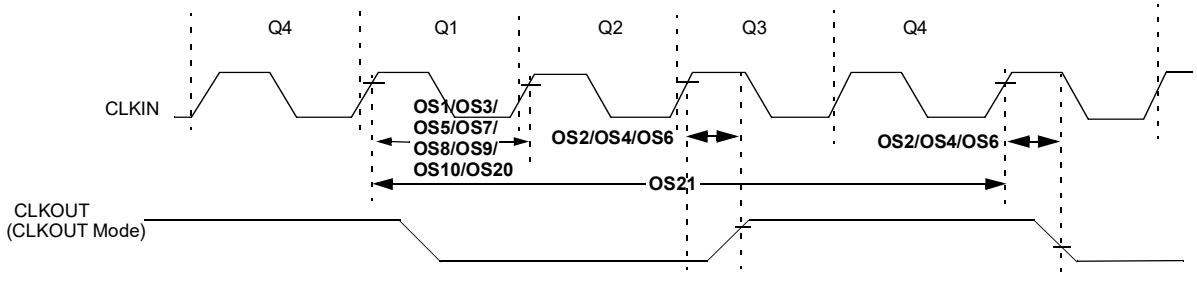
2. Module: Section 4.2.3 Boot Block

If **$\overline{\text{BBEN}}$ = 0**, the Boot Block is enabled and a specific address range is alloted as the Boot Block based on the value of the BBSIZE bits of Configuration Word (Register 5-4) and the sizes provided in Table 5-1.

3. Module: Electrical Specifications

3.1 Figure 37-5: Clock Timing

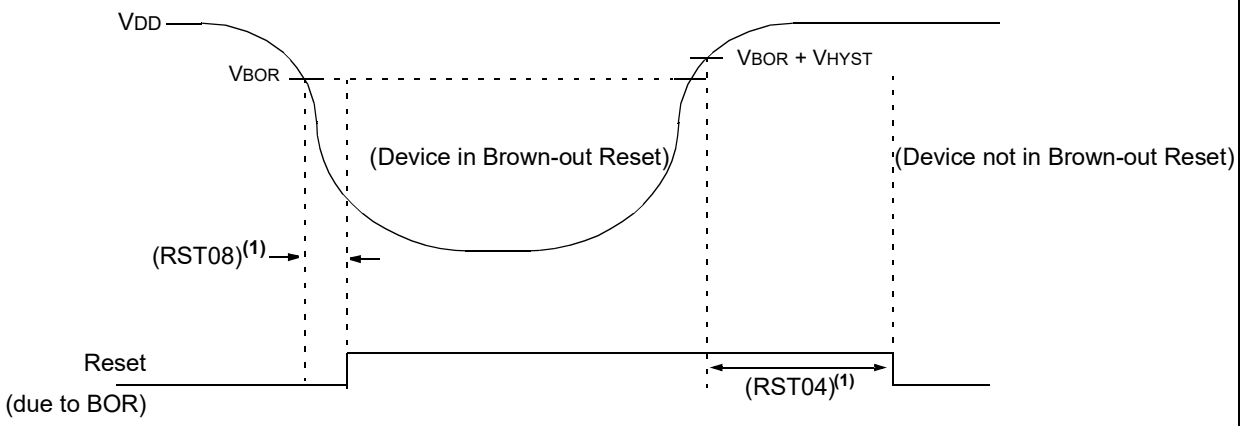
Figure 37-5 incorrectly shows the location of parameters OS1, OS2, OS3, OS4, OS5, OS6, OS7, OS8, OS9, OS10, OS20 and OS21. The correct location for the above-mentioned parameters is depicted in the following figure.



Note 1: See Table 37-7.

3.2 Figure 37-9: Brown-Out Reset Timing and Characteristics

Note 1 in Figure 37-9 is incorrect. The correct note along with the figure is depicted below.



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '**0**'.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev D Document (03/2021)

Updated Table 2 and 37-1 and Section 4.1 Minimum V_{DD} Specification. Other minor corrections.

Data Sheet Clarifications:

Added Module 3: Electrical Specifications.

Rev C Document (11/2020)

Added Table 37-1 and Section 4.3 ADC Offset Error; Updated Table 2 and Section 4.1.

Rev B Document (11/2018)

Added Module 4: Electrical Specifications, 4.1 and 4.2.

Data Sheet Clarifications:

Removed Modules 1 and 2. Added Module 1: Interrupt-on-Change (PORTE); Added Module 2: Section 4.2.3 Boot Block.

Rev A Document (01/2017)

Initial release of this document.