

# MOSFET - N-Channel Shielded Gate PowerTrench®

150 V, 22 mΩ, 41.9 A

## NTMFS022N15MC

### Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	150	V
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJC</sub> (Note 2)	I <sub>D</sub>	41.9	A
Power Dissipation R <sub>θJC</sub> (Note 2)	P <sub>D</sub>	80.6	W
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2)	I <sub>D</sub>	7.3	A
Power Dissipation R <sub>θJA</sub> (Notes 1, 2)	P <sub>D</sub>	2.5	W
Pulsed Drain Current	I <sub>DM</sub>	183	A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L</sub> = 8 A <sub>pk</sub> , L = 3 mH)	E <sub>AS</sub>	96	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

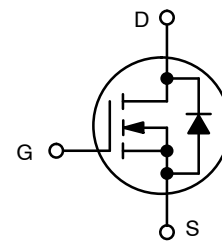
1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



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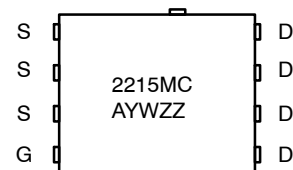
V <sub>(BR)DSS</sub>	R <sub>DS(ON) MAX</sub>	I <sub>D MAX</sub>
150 V	22 mΩ @ 10 V	41.9 A



N-CHANNEL MOSFET



### MARKING DIAGRAM



2215MC = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS022N15MC (Pb-Free/Halogen Free)	Power 56 (PQFN8)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS022N15MC

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	1.55	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		83		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 100\ \mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 100\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-7.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 18\text{ A}$		18.1	22	m $\Omega$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 8\text{ V}, I_D = 9\text{ A}$		19.7	25.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 18\text{ A}$		35		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		1315		pF
Output Capacitance	$C_{OSS}$			380		
Reverse Transfer Capacitance	$C_{RSS}$			6		
Gate-Resistance	$R_G$			0.6	1.2	$\Omega$
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 18\text{ A}$		17		nC
Threshold Gate Charge	$Q_{G(TH)}$			4.4		
Gate-to-Source Charge	$Q_{GS}$			7.2		
Gate-to-Drain Charge	$Q_{GD}$			2.7		
Plateau Voltage	$V_{GP}$			5.6		
Output Charge	$Q_{OSS}$	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		41		nC

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 18\text{ A}, R_G = 6\ \Omega$		14		ns
Rise Time	$t_r$			2.8		
Turn-Off Delay Time	$t_{d(OFF)}$			17		
Fall Time	$t_f$			2.9		

### DRAIN-SOURCE DIODE CHARACTERISTICS

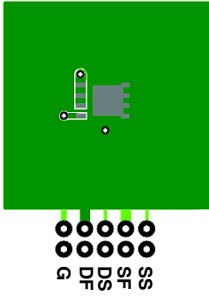
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$	$T_J = 25^\circ\text{C}$		0.88	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 18\text{ A}$			45		ns
Reverse Recovery Charge	$Q_{RR}$				155		nC
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 18\text{ A}$			28		ns
Reverse Recovery Charge	$Q_{RR}$				242		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

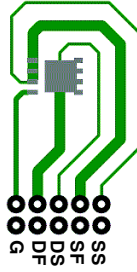
# NTMFS022N15MC

## NOTES:

3. Switching characteristics are independent of operating junction temperatures.
4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

# NTMFS022N15MC

## TYPICAL CHARACTERISTICS

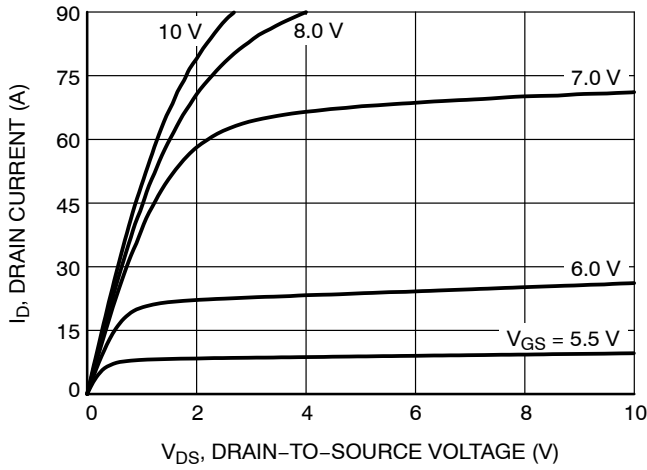


Figure 1. On-Region Characteristics

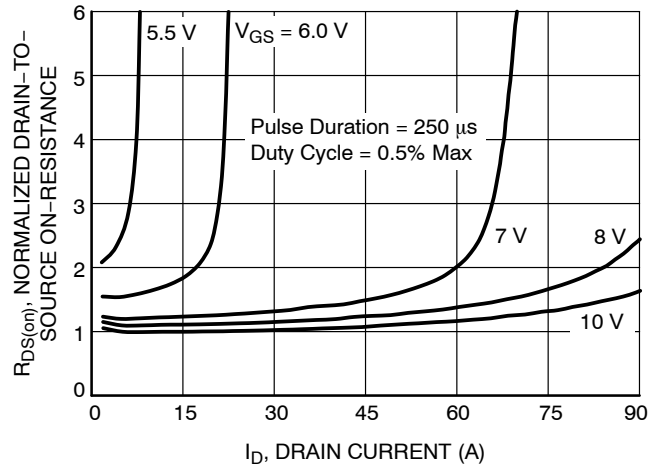


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

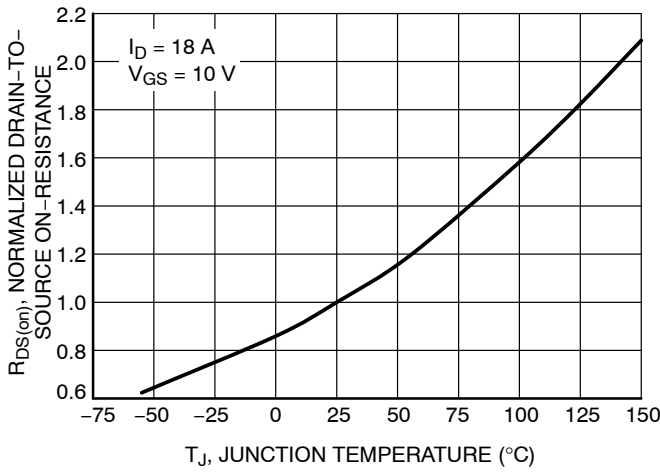


Figure 3. Normalized On-Resistance vs. Junction Temperature

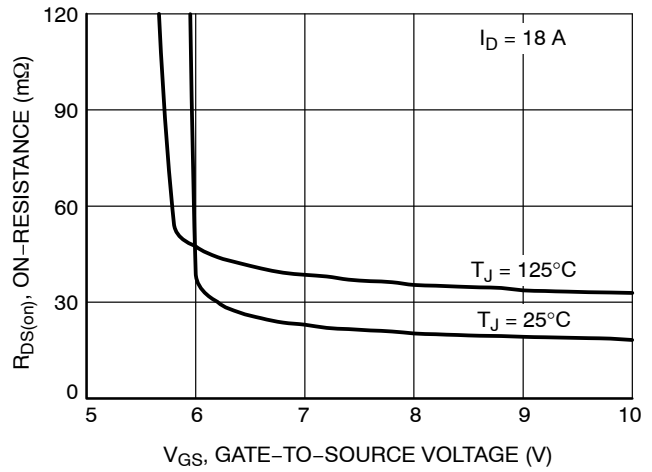


Figure 4. On-Resistance vs. Gate-to-Source Voltage

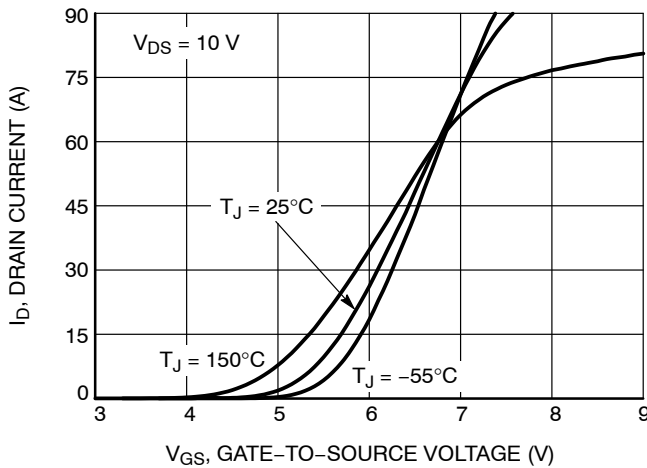


Figure 5. Transfer Characteristics

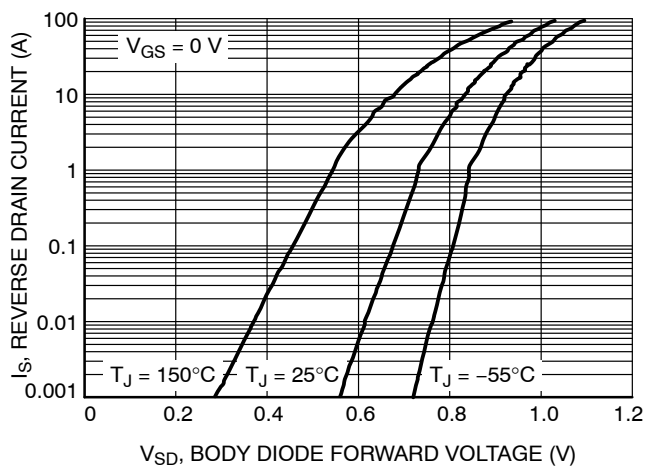


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

# NTMFS022N15MC

## TYPICAL CHARACTERISTICS

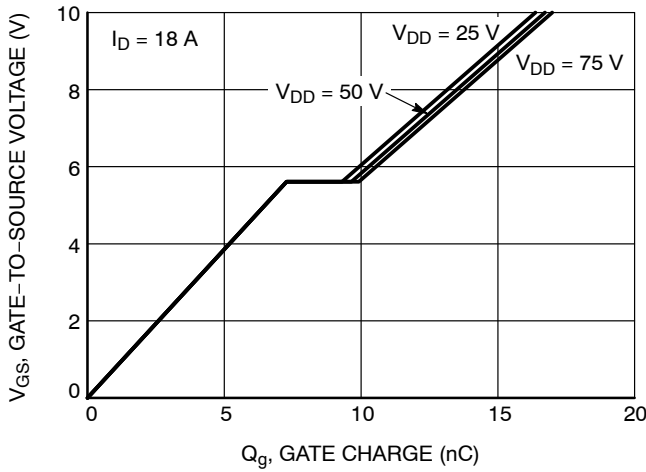


Figure 7. Gate Charge Characteristics

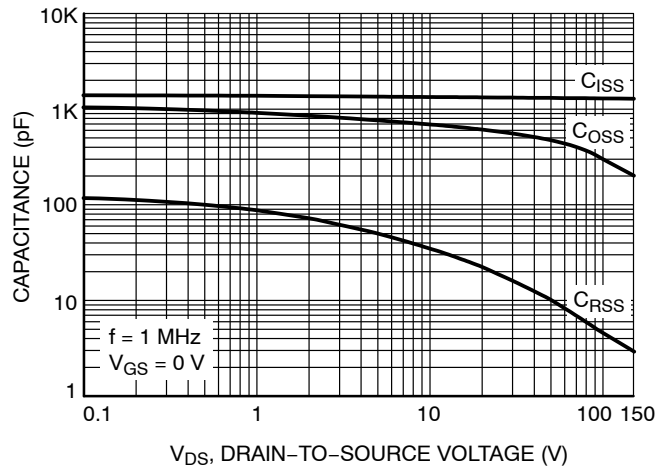


Figure 8. Capacitance vs. Drain-to-Source Voltage

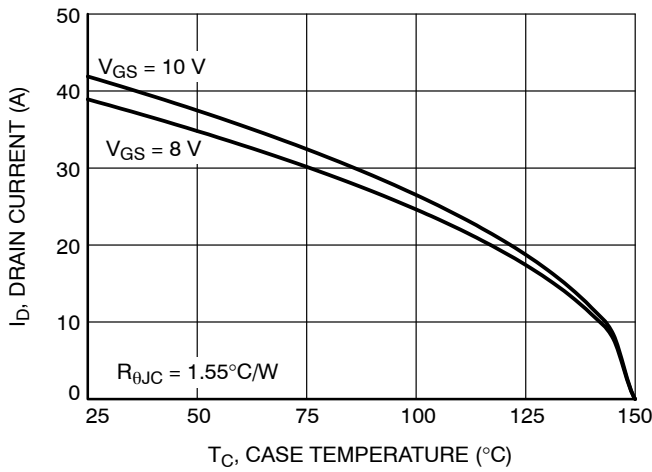


Figure 9. Drain Current vs. Case Temperature

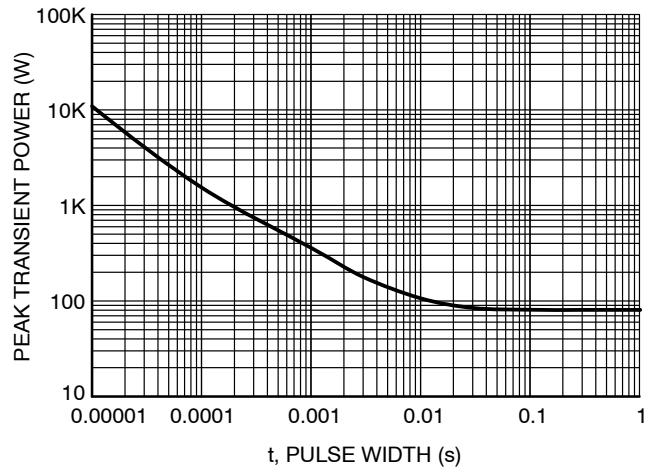


Figure 10. Peak Power

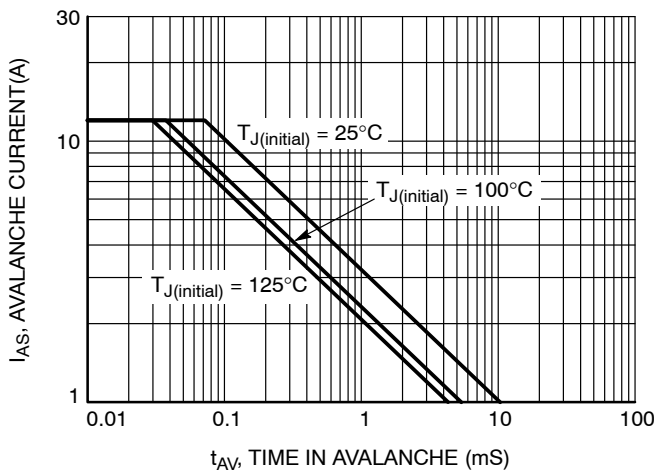


Figure 11. Unclamped Inductive Switching Capability

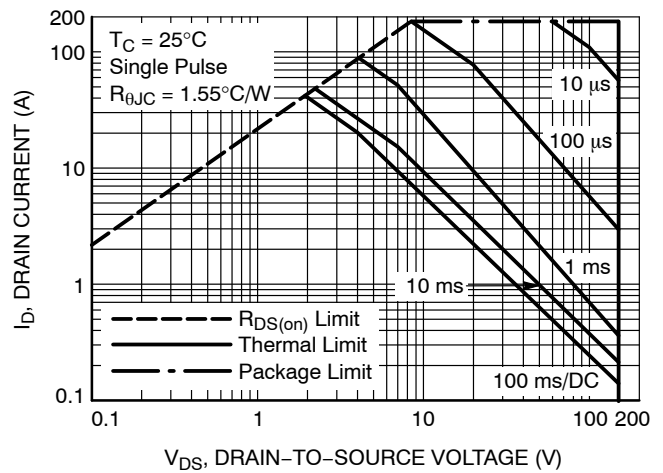


Figure 12. Forward Bias Safe Operating Area

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## TYPICAL CHARACTERISTICS

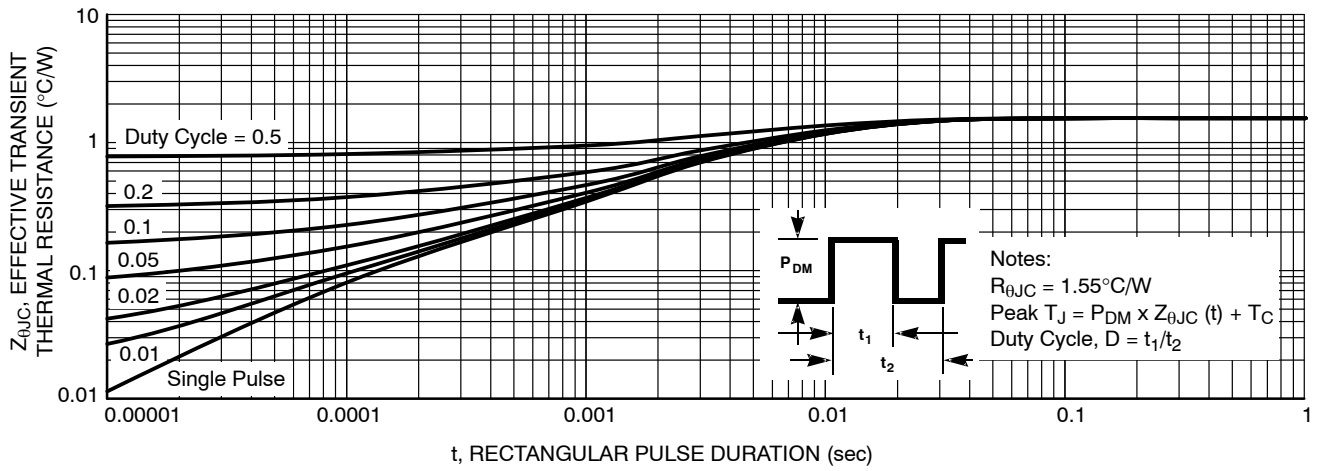
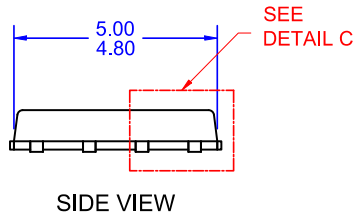
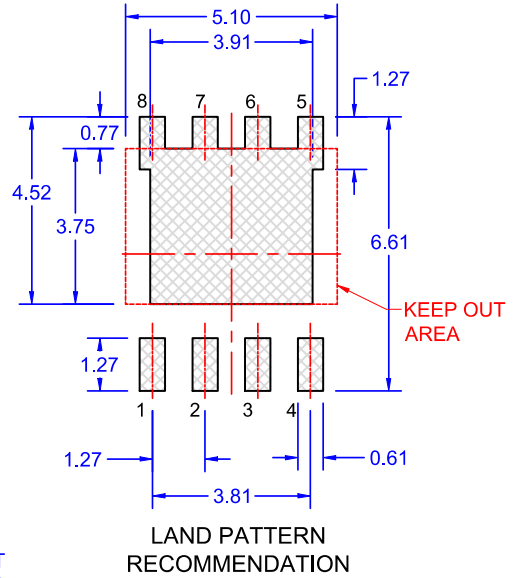
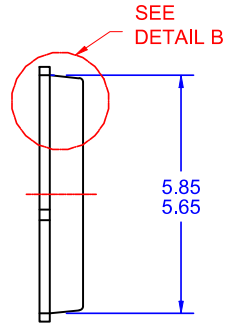
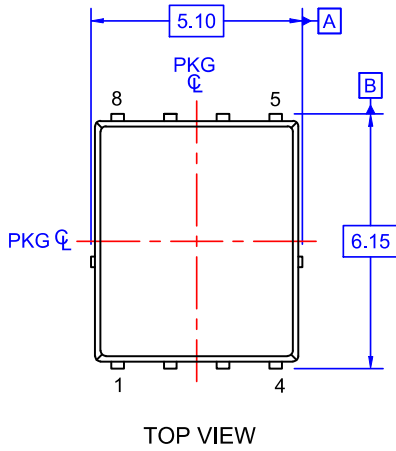


Figure 13. Transient Thermal Impedance

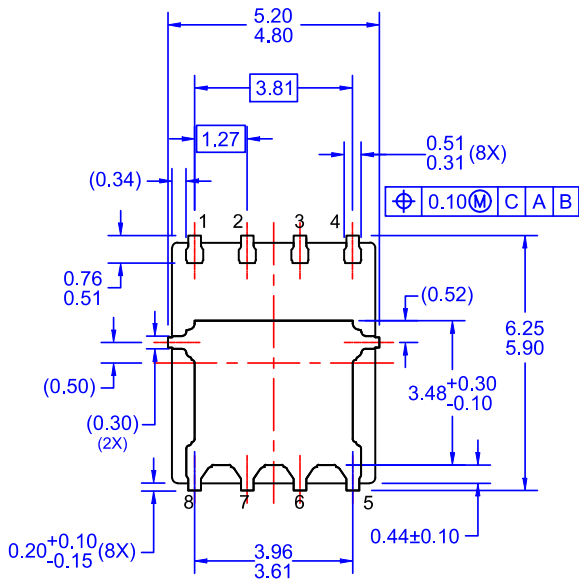
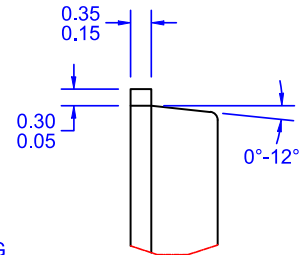
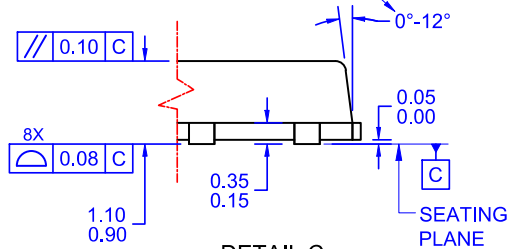
# NTMFS022N15MC

## PACKAGE DIMENSIONS

PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



- NOTES: UNLESS OTHERWISE SPECIFIED
- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
  - B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - C. ALL DIMENSIONS ARE IN MILLIMETERS.
  - D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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