

## 24-Bit, 96 kHz Stereo D/A Converter for Audio

### Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.0 V or +5.0 V Power Supply
- Low Clock Jitter Sensitivity
- Filtered Line-level Outputs
- On-chip Digital De-emphasis for 32, 44.1 and 48 kHz
- 33 mW with 3V Supply
- Popguard® Technology for Control of Clicks and Pops
- Lead-free Packaging Available

### Description

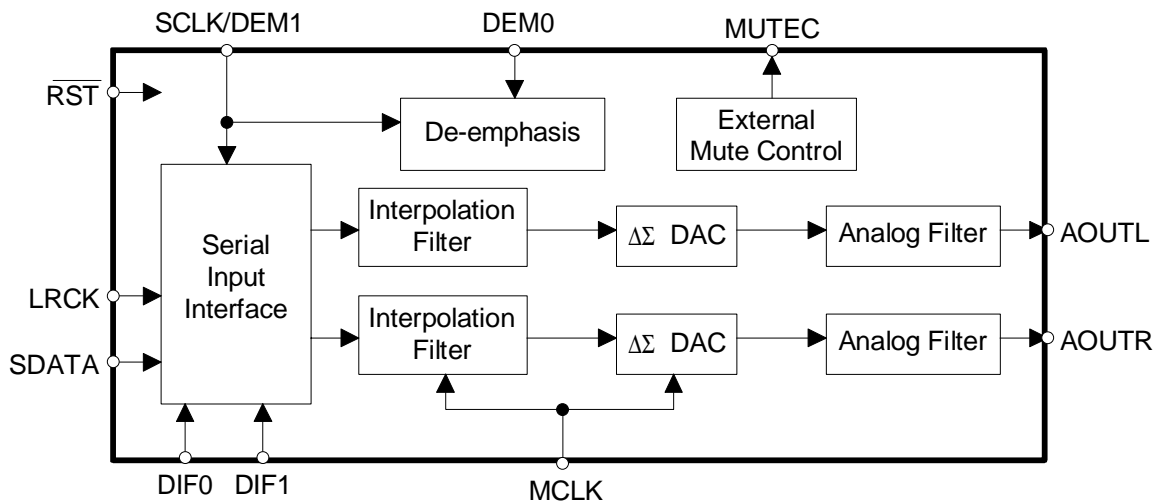
The CS4340 is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma dig-

ital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4340 accepts data at audio sample rates from 4 kHz to 100 kHz, consumes very little power, and operates over a wide power supply range. The features of the CS4340 are ideal for DVD players, CD players, set-top box and automotive systems.

### ORDERING INFORMATION

CS4340-DSZ	16-pin SOIC, Lead Free,	-40 to 85 °C
CS4340-KS	16-pin SOIC	-10 to 70 °C
CS4340-KSZ	16-pin SOIC, Lead Free,	-10 to 70 °C
CS4340-CZZ	16-pin TSSOP, Lead Free,	-10 to 70 °C
CDB4340	Evaluation Board	



**TABLE OF CONTENTS**

<b>1. CHARACTERISTICS AND SPECIFICATIONS .....</b>	<b>4</b>
SPECIFIED OPERATING CONDITIONS .....	4
ABSOLUTE MAXIMUM RATINGS .....	4
ANALOG CHARACTERISTICS (CS4340-KS/KSZ/CZZ).....	5
ANALOG CHARACTERISTICS (CS4340-DSZ) .....	7
COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE.....	8
SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE.....	11
SWITCHING CHARACTERISTICS - INTERNAL SERIAL CLOCK .....	12
DC ELECTRICAL CHARACTERISTICS.....	13
DIGITAL INPUT CHARACTERISTICS .....	13
DIGITAL INTERFACE SPECIFICATIONS.....	13
<b>2. PIN DESCRIPTION .....</b>	<b>14</b>
<b>3. TYPICAL CONNECTION DIAGRAM .....</b>	<b>15</b>
<b>4. APPLICATIONS .....</b>	<b>16</b>
4.1 Sample Rate Range/Operational Mode .....	16
4.2 System Clocking .....	16
4.2.1 Internal Serial Clock Mode .....	16
4.2.2 External Serial Clock Mode .....	17
4.3 Digital Interface Format .....	17
4.4 De-Emphasis .....	18
4.5 Power-up Sequence .....	19
4.6 Popguard® Transient Control .....	19
4.6.1 Power-up .....	19
4.6.2 Power-down .....	19
4.6.3 Discharge Time .....	19
4.7 Mute Control .....	20
4.8 Grounding and Power Supply Arrangements .....	20

---

**Contacting Cirrus Logic Support**

For all product questions and inquiries contact a Cirrus Logic Sales Representative.  
To find one nearest you go to [www.cirrus.com](http://www.cirrus.com)

---

**IMPORTANT NOTICE**

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.



## 1. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at  $T_A = 25\text{ C.}$ )

### SPECIFIED OPERATING CONDITIONS (All voltages with respect to AGND = 0 V.)

Parameters	Symbol	Min	Nom	Max	Units	
<b>DC Power Supply</b>						
Nominal 3.3V	VA	2.7	3.3	3.6	V	
Nominal 5.0V	VA	4.75	5.0	5.5	V	
Specified Operating Temperature (Power Applied)	-KS/KSZ/CZZ	$T_A$	-10	-	+70	C
	-DSZ	$T_A$	-40		+85	C

**ABSOLUTE MAXIMUM RATINGS** (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current (Note 1)	$I_{in}$	-	$\pm 10$	mA
Digital Input Voltage	$V_{IND}$	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	$T_A$	-55	125	°C
Storage Temperature	$T_{stg}$	-65	150	°C

Notes: 1. Any pin except supplies.

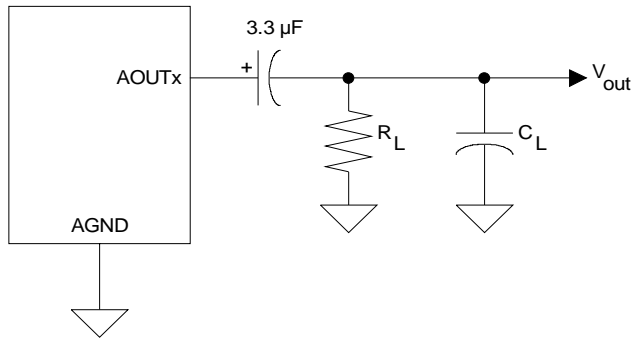
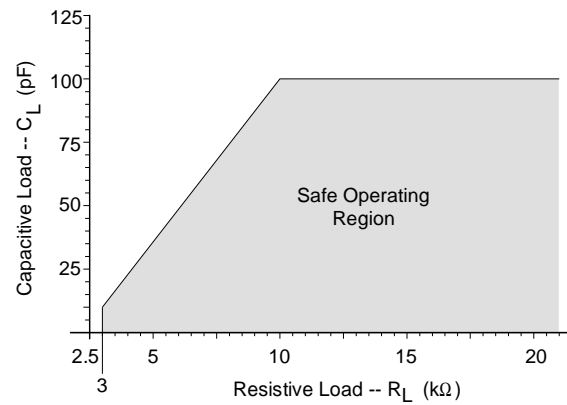
**ANALOG CHARACTERISTICS (CS4340-KS/KSZ/CZZ)** (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$  (see Figure 1).)

Parameter		VA = 5.0 V			VA = 3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>Single-Speed Mode</b>		<b>Fs = 48 kHz</b>						
Dynamic Range 18 to 24-Bit	(Note 2)							
	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise 18 to 24-Bit	(Note 2)							
	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	(Note 2)							
	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
<b>Double-Speed Mode</b>		<b>Fs = 96 kHz</b>						
Dynamic Range 18 to 24-Bit	(Note 2)							
	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise 18 to 24-Bit	(Note 2)							
	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	(Note 2)							
	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

**ANALOG CHARACTERISTICS (CS4340-KS/KSZ/CZZ)** (Continued)

Parameters	Symbol	Min	Typ	Max	Units
<b>Dynamic Performance for All Modes</b>					
Interchannel Isolation (1 kHz)		-	102	-	dB
<b>DC Accuracy</b>					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
<b>Analog Output Characteristics and Specifications</b>					
Full Scale Output Voltage		0.6•VA	0.7•VA	0.8•VA	V <sub>pp</sub>
Output Impedance		-	100	-	Ω
Minimum AC-Load Resistance (Note 3)	R <sub>L</sub>	-	3	-	kΩ
Maximum Load Capacitance (Note 3)	C <sub>L</sub>	-	100	-	pF

- Notes: 2. One-half LSB of triangular PDF dither is added to data.  
 3. Refer to Figure 2.


**Figure 1. Output Test Load**

**Figure 2. Maximum Loading**

**ANALOG CHARACTERISTICS (CS4340-DSZ)** (Test conditions (unless otherwise specified):

 Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$  (see Figure 1).)

Parameter		VA = 5.0 V			VA = 3.0 V			Unit	
		Min	Typ	Max	Min	Typ	Max		
<b>Single-Speed Mode</b>		<b>Fs = 48 kHz</b>							
Dynamic Range 18 to 24-Bit	(Note 2)								
	unweighted	93	98	-	89	94	-	dB	
	A-Weighted	96	101	-	92	97	-	dB	
16-Bit	unweighted	-	92	-	-	92	-	dB	
	A-Weighted	-	95	-	-	95	-	dB	
Total Harmonic Distortion + Noise 18 to 24-Bit	(Note 2)								
	0 dB	-	-91	-86	-	-94	-87	dB	
	-20 dB	-	-78	-	-	-74	-	dB	
	-60 dB	-	-38	-	-	-34	-	dB	
	16-Bit	0 dB	-	-90	-	-	-91	-	dB
		-20 dB	-	-72	-	-	-72	-	dB
		-60 dB	-	-32	-	-	-32	-	dB
	<b>Double-Speed Mode</b>		<b>Fs = 96 kHz</b>						
	Dynamic Range 18 to 24-Bit	(Note 2)							
		unweighted	93	98	-	89	94	-	dB
		A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB	
	A-Weighted	-	95	-	-	95	-	dB	
Total Harmonic Distortion + Noise 18 to 24-Bit	(Note 2)								
	0 dB	-	-91	-86	-	-94	-87	dB	
	-20 dB	-	-78	-	-	-74	-	dB	
	-60 dB	-	-38	-	-	-34	-	dB	
	16-Bit	0 dB	-	-90	-	-	-91	-	dB
		-20 dB	-	-72	-	-	-72	-	dB
		-60 dB	-	-32	-	-	-32	-	dB

**ANALOG CHARACTERISTICS (CS4340-DSZ) (Continued)**

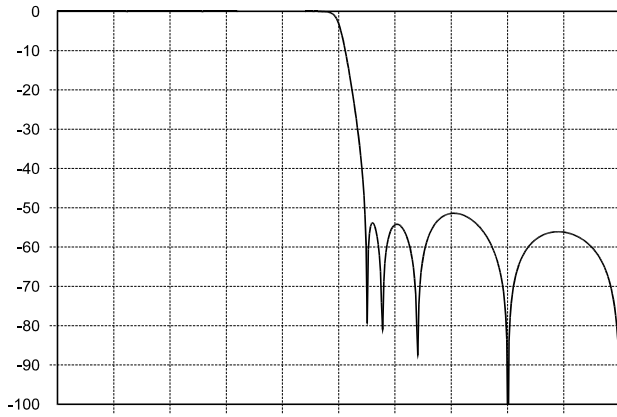
Parameters	Symbol	Min	Typ	Max	Units
<b>Dynamic Performance for All Modes</b>					
Interchannel Isolation (1 kHz)		-	102	-	dB
<b>DC Accuracy</b>					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
<b>Analog Output Characteristics and Specifications</b>					
Full Scale Output Voltage		0.6•VA	0.7•VA	0.8•VA	V <sub>pp</sub>
Output Impedance		-	100	-	Ω
Minimum AC-Load Resistance (Note 3)	R <sub>L</sub>	-	3	-	kΩ
Maximum Load Capacitance (Note 3)	C <sub>L</sub>	-	100	-	pF

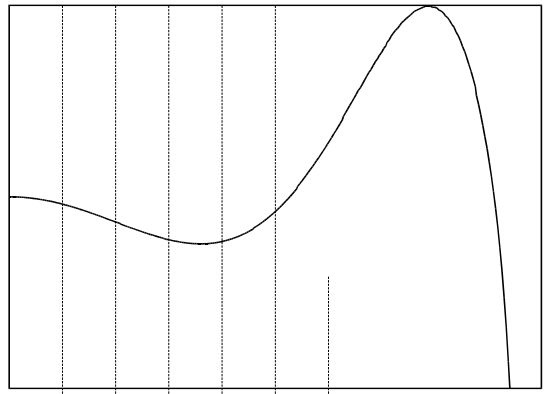
**COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE** (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter	Min	Typ	Max	Unit	
<b>Single-Speed Mode - (4 kHz to 50 kHz sample rates)</b>					
Passband	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz	-0.02	-	+0.08	dB	
StopBand	0.5465	-	-	Fs	
StopBand Attenuation (Note 4)	50	-	-	dB	
Group Delay	-	9/Fs	-	s	
Passband Group Delay Deviation 0 - 20 kHz	-	±0.36/Fs	-	s	
De-emphasis Error (Relative to 1 kHz) (Note 5)	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
<b>Double-Speed Mode - (50 kHz to 100 kHz sample rates)</b>					
Passband	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz	-0.06	-	+0.2	dB	
StopBand	0.577	-	-	Fs	
StopBand Attenuation (Note 4)	55	-	-	dB	
Group Delay	-	4/Fs	-	s	
Passband Group Delay Deviation 0 - 40 kHz	0 - 40 kHz	-	±1.39/Fs	-	s
	0 - 20 kHz	-	±0.23/Fs	-	s

- Notes: 4. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.  
 For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
5. De-emphasis is only available in Single-Speed Mode.

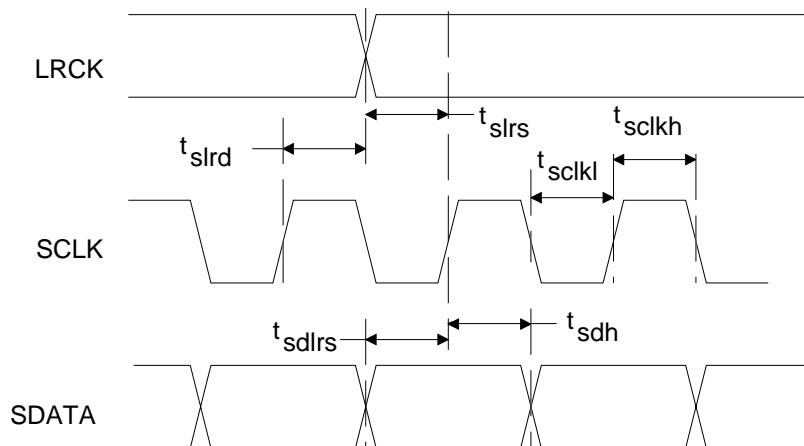






**SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE**

Parameters	Symbol	Min	Max	Units	
MCLK Frequency		1.024	25.6	MHz	
MCLK Duty Cycle		45	55	%	
Input Sample Rate	Single-Speed Mode	$F_s$	4	50	kHz
	Double-Speed Mode	$F_s$	50	100	kHz
LRCK Duty Cycle		40	60	%	
SCLK Pulse Width Low	$t_{sckl}$	20	-	ns	
SCLK Pulse Width High	$t_{sckh}$	20	-	ns	
SCLK Frequency	Single-Speed Mode	-	$128 \times F_s$	Hz	
	Double-Speed Mode	-	$64 \times F_s$	Hz	
SCLK rising to LRCK edge delay	$t_{slrd}$	20	-	ns	
SCLK rising to LRCK edge setup time	$t_{slrs}$	20	-	ns	
SDIN valid to SCLK rising setup time	$t_{sdls}$	20	-	ns	
SCLK rising to SDIN hold time	$t_{sdh}$	20	-	ns	

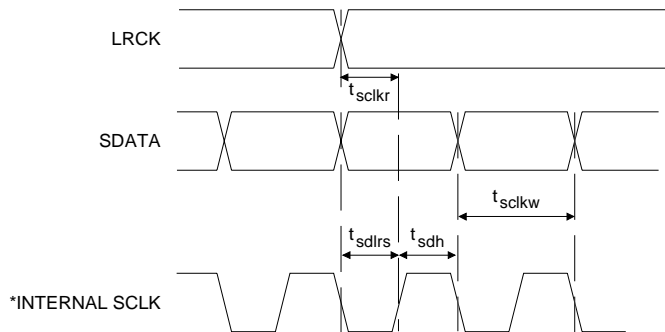

**Figure 11. Serial Input Timing (External SCLK)**

## SWITCHING CHARACTERISTICS - INTERNAL SERIAL CLOCK

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		1.024	-	25.6	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate	Single-Speed Mode Double-Speed Mode	F <sub>s</sub> F <sub>s</sub>	- -	50 100	kHz kHz
LRCK Duty Cycle			(Note 6)		%
SCLK Period	(Note 7) t <sub>sclkw</sub>	$\frac{1}{\text{SCLK}}$	-	-	s
SCLK rising to LRCK edge	t <sub>sclkr</sub>	-	$\frac{t_{\text{sclkw}}}{2}$	-	s
SDATA valid to SCLK rising setup time	t <sub>sdlrs</sub>	$\frac{1}{(512)F_s} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t <sub>sdh</sub>	$\frac{1}{(512)F_s} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t <sub>sdh</sub>	$\frac{1}{(384)F_s} + 15$	-	-	ns

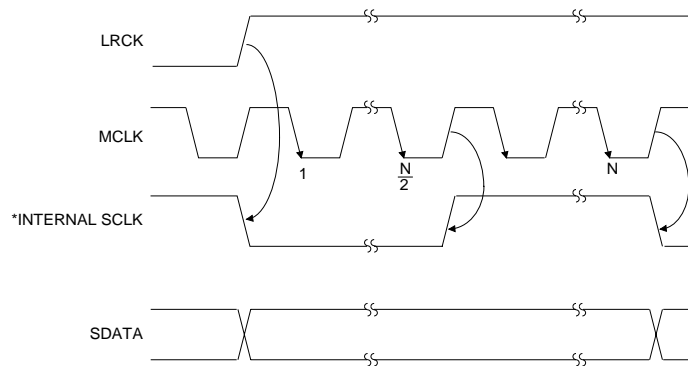
Notes: 6. The Duty Cycle must be 50% +/- 1/2 MCLK Period.

7. See section 4.2.1 for derived internal frequencies.



**Figure 12. Internal Serial Mode Input Timing**

\*The SCLK pulses shown are internal to the CS4340.



**Figure 13. Internal Serial Clock Generation**

\* The SCLK pulses shown are internal to the CS4340. N equals MCLK divided by SCLK

**DC ELECTRICAL CHARACTERISTICS** (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Typ	Max	Units	
<b>Normal Operation</b> (Note 8)						
Power Supply Current	VA = 5.0 V	$I_A$	-	15	18	mA
	VA = 3.0 V	$I_A$	-	11	14	mA
Power Dissipation	VA = 5.0 V		-	75	90	mW
	VA = 3.0 V		-	33	42	mW
<b>Power-down Mode</b> (Note 9)						
Power Supply Current	VA = 5.0 V	$I_A$	-	60	-	A
	VA = 3.0 V		-	30	-	A
Power Dissipation	VA = 5.0 V		-	0.3	-	mW
	VA = 3.0 V		-	0.09	-	mW
<b>All Modes of Operation</b>						
Power Supply Rejection Ratio (Note 10)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V <sub>Q</sub> Nominal Voltage			-	0.45•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 8. Normal operation is defined as  $\overline{RST} = HI$  with a 997 Hz, 0 dBFS input sampled at the highest Fs for each speed mode, and open outputs, unless otherwise specified.

9. Power Down Mode is defined as  $\overline{RST} = LO$  with all clocks and data lines held static.

10. Valid with the recommended capacitor values on Filt+ and V<sub>Q</sub> as shown in Figure 14. Increasing the capacitance will also increase the PSRR.

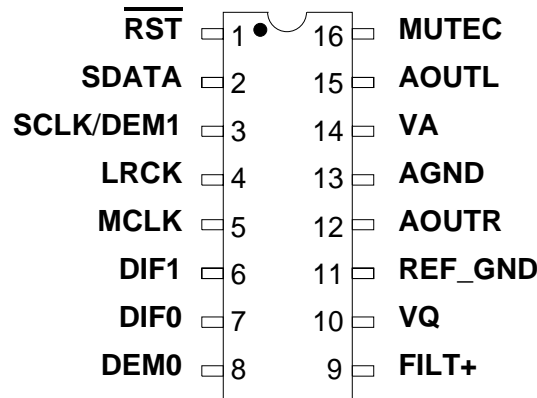
**DIGITAL INPUT CHARACTERISTICS** (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	$I_{in}$	-	-	±10	A
Input Capacitance		-	8	-	pF

**DIGITAL INTERFACE SPECIFICATIONS** (AGND = 0 V; all voltages with respect to AGND.)

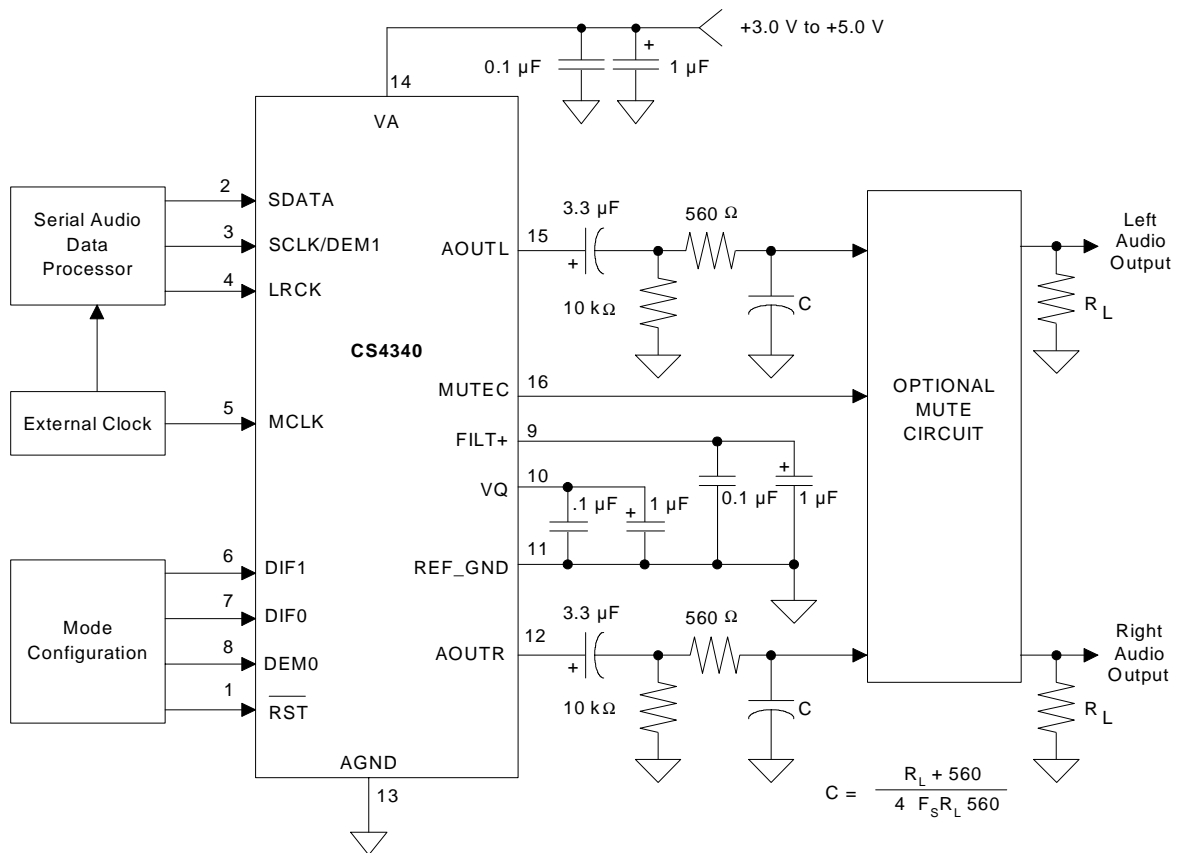
Parameters	Symbol	Min	Max	Units
<b>3.3 V Logic</b> (3.0 V to 3.6 V DC Supply)				
High-Level Input Voltage	V <sub>IH</sub>	2.0	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	0.8	V
<b>5.0 V Logic</b> (4.75 V to 5.25 V DC Supply)				
High-Level Input Voltage	V <sub>IH</sub>	2.0	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	0.8	V

## 2. PIN DESCRIPTION



Pin Name	#	Pin Description
<b>RST</b>	1	<b>Reset (Input)</b> - Powers down device.
<b>SDATA</b>	2	<b>Serial Audio Data (Input)</b> - Input for two's complement serial audio data.
<b>SCLK</b>	3	<b>Serial Clock (Input)</b> -Serial clock for the serial audio interface.
<b>DEM1</b> <b>DEM0</b>	3 8	<b>De-emphasis Control (Input)</b> - Selects the standard 15 s/50 s digital de-emphasis filter response for 44.1 kHz sample rate.
<b>LRCK</b>	4	<b>Left Right Clock (Input)</b> - Determines which channel, Left or Right, is currently active on the serial audio data line.
<b>MCLK</b>	5	<b>Master Clock (Input)</b> - Clock source for the delta-sigma modulator and digital filters.
<b>DIF1</b> <b>DIF0</b>	6 7	<b>Digital Interface Format (Input)</b> - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data.
<b>FILT+</b>	9	<b>Positive Voltage Reference (Output)</b> - Positive voltage reference for the internal sampling circuits.
<b>VQ</b>	10	<b>Quiescent Voltage (Output)</b> - Filter connection for internal quiescent reference voltage.
<b>REF_GND</b>	11	<b>Reference Ground (Input)</b> - Ground reference for the internal sampling circuits.
<b>AOUTR</b> <b>AOUTL</b>	12 15	<b>Analog Outputs (Output)</b> - The full scale analog output level is specified in the <i>Analog Characteristics</i> table.
<b>AGND</b>	13	<b>Analog Ground (Input)</b>
<b>VA</b>	14	<b>Power (Input)</b> - Positive power for the analog, digital and serial audio interface sections.
<b>MUTEC</b>	16	<b>Mute Control (Output)</b> - Control signal for an optional mute circuit.

### 3. TYPICAL CONNECTION DIAGRAM



**Figure 14. Typical Connection Diagram**

## 4. APPLICATIONS

### 4.1 Sample Rate Range/Operational Mode

The device operates in one of two operational modes determined by the Master Clock to Left/Right Clock ratio (see section 4.2). Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (Fs)	MODE
4 kHz - 50 kHz	Single-Speed Mode
50 kHz - 100 kHz	Double-Speed Mode

**Table 1. CS4340 Speed Modes**

### 4.2 System Clocking

The device requires external generation of the master (MCLK) and left/right (LRCK) clocks. The device also requires external generation of the serial clock (SCLK) if the internal serial clock is not used. The LRCK, defined also as the input sample rate  $F_s$ , must be synchronously derived from MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2 and 3.

Sample Rate (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

**Table 2. Single-Speed Mode Standard Frequencies**

Sample Rate (kHz)	MCLK (MHz)	
	128x	192x
64	8.1920	12.2880
88.2	11.2896	16.9344
96	12.2880	18.4320

**Table 3. Double-Speed Mode Standard Frequencies**

#### 4.2.1 Internal Serial Clock Mode

The device will enter the Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK. In this mode, the SCLK is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK ratio is either 32, 48, or 64 depending upon the MCLK/LRCK ratio and the Digital Interface Format selection (see Table 4).



The internal serial clock is utilized when additional de-emphasis control is required. Operation in the Internal Serial Clock mode is identical to operation with an external SCLK synchronized with LRCK; however, External SCLK mode is recommended for system clocking applications.

Input MCLK/LRCK Ratio	Digital Interface Format Selection				Internal SCLK/LRCK Ratio
	I <sup>2</sup> S up to 24 Bits	Left Justified 24 Bits	Right Justified 24 Bits	Right Justified 16 Bits	
512, 256, 128	X	-	-	X	32
384, 192	X	X	X	X	48
512, 256, 128	-	X	X	-	64

**Table 4. Internal SCLK/LRCK Ratio**

### 4.2.2 External Serial Clock Mode

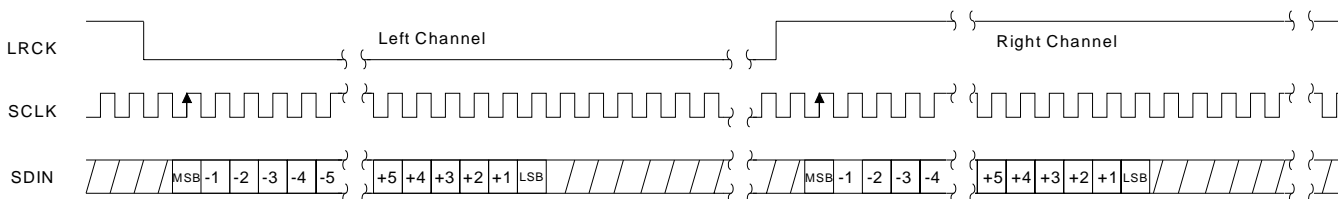
The device will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK.

### 4.3 Digital Interface Format

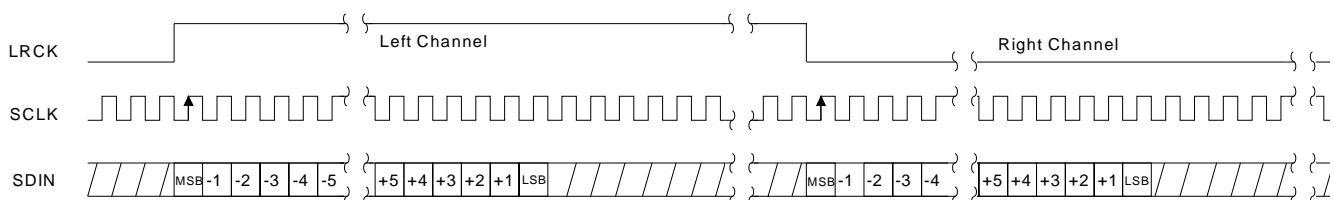
The device will accept audio samples in several digital interface formats as illustrated in Table 5. The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 15 through 18.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I <sup>2</sup> S, up to 24-bit data	0	15
0	1	Left Justified, up to 24-bit data	1	16
1	0	Right Justified, 24-bit Data	2	17
1	1	Right Justified, 16-bit Data	3	18

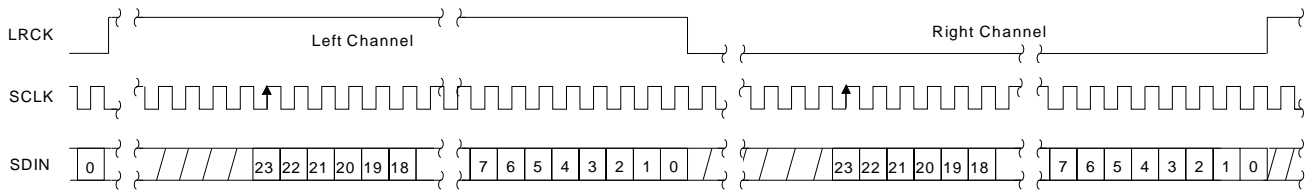
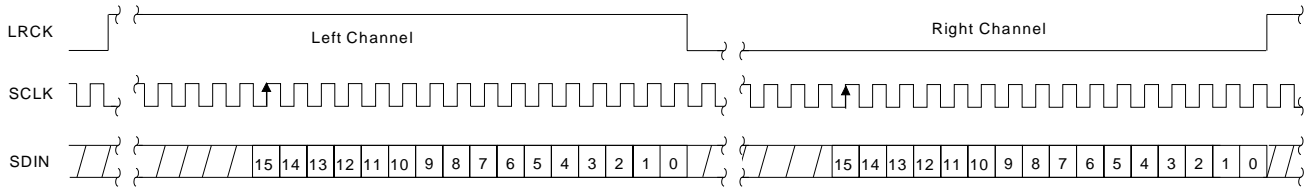
**Table 5. Digital Interface Format - DIF1 and DIF0**



**Figure 15. CS4340 Format 0 - I<sup>2</sup>S up to 24-Bit Data**



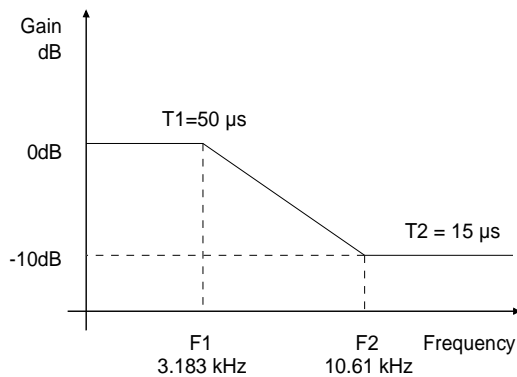
**Figure 16. CS4340 Format 1 - Left Justified up to 24-Bit Data**


**Figure 17. CS4340 Format 2 - Right Justified, 24-Bit Data**

**Figure 18. CS4340 Format 3 - Right Justified, 16-Bit Data**

## 4.4 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 19 shows the de-emphasis curve for  $F_s$  equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate,  $F_s$ .

Pin 8 is available for de-emphasis control and selects the 44.1 kHz de-emphasis filter. If the Internal Serial Clock is used, pin 3 is also available for additional de-emphasis control and, in combination with pin 8, selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see Table 6 for the desired de-emphasis control.


**Figure 19. De-Emphasis Curve**

<i>Internal SCLK</i>		
DEM1	DEM0	Description
0	0	Disabled
0	1	44.1 kHz
1	0	48 kHz
1	1	32 kHz

<i>External SCLK</i>	
DEM0	Description
0	Disabled
1	44.1 kHz

**Table 6. De-Emphasis Control**

## 4.5 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supply and configuration pins are stable, and the clocks are locked to the appropriate frequencies discussed in section 4.2. It is also recommended that reset be enabled if the analog supply drops below the minimum specified operating voltage to prevent power glitch related issues.

## 4.6 Popguard® Transient Control

The CS4340 uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when  $\overline{\text{RST}}$  is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

### 4.6.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach  $V_Q$  and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

### 4.6.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by enabling  $\overline{\text{RST}}$ . When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

### 4.6.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3  $\mu\text{F}$  capacitor, the minimum power-down time will be approximately 0.4 seconds.

## 4.7 Mute Control

The Mute Control pin goes high during power-up initialization, reset, or if the MCLK to LRCK ratio is incorrect. The pin will also go high following the reception of 8192 consecutive audio samples of static 0 or -1 on both the left and right channels. A single sample of non-zero data on either channel will cause the Mute Control pin to go low. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4340 data sheet for a suggested mute circuit.

## 4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4340 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 14 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF\_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC.

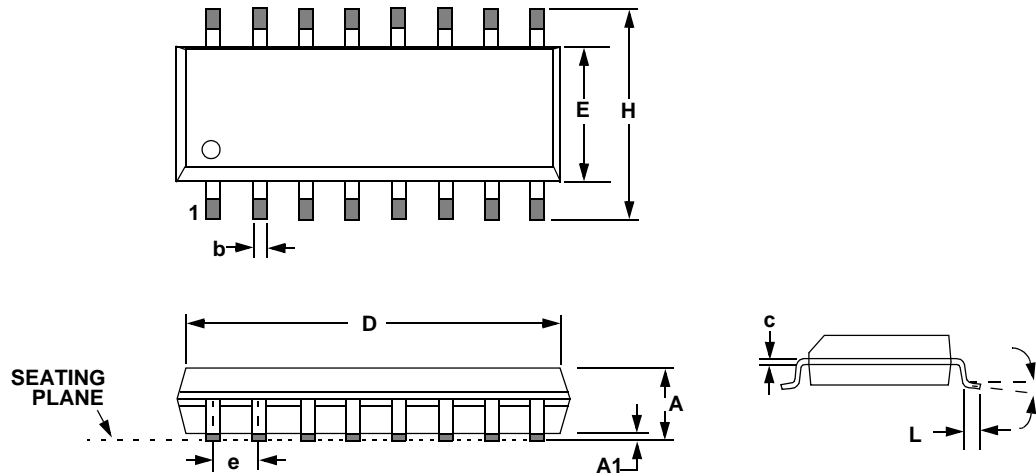
All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1  $\mu$ F, must be positioned to minimize the electrical path from FILT+ and REF\_GND (as well as VQ and REF\_GND), and should also be located on the same layer as the DAC. The CDB4340 evaluation board demonstrates the optimum layout and power supply arrangements.

## **5. PARAMETER DEFINITIONS**

**Total Harmonic Distortion + Noise (THD+N)**

## **6. REFERENCES**

- 1) CDB4340 Evaluation Board Datasheet

**7. PACKAGE DIMENSIONS**
**7.1 SOIC**
**16L SOIC (150 MIL BODY) PACKAGE DRAWING**


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	0.064	0.069	1.35	1.63	1.75
A1	0.004	0.006	0.010	0.10	0.15	0.25
b	0.013	0.016	0.020	0.33	0.41	0.51
C	0.0075	0.008	0.010	0.19	0.20	0.25
D	0.386	0.390	0.394	9.80	9.91	10.00
E	0.150	0.154	0.157	3.80	3.90	4.00
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.228	0.236	0.244	5.80	6.0	6.20
L	0.016	0.025	0.050	0.40	0.64	1.27
	0°	4°	8°	0°	4°	8°

**JEDEC #: MS-012**

Controlling Dimension is Millimeters





---

## 8. PACKAGE THERMAL RESISTANCE

Package	Symbol	Min	Typ	Max	Units
SOIC (for multi-layer boards)	JA	-	74	-	°C/Watt
TSSOP (for multi-layer boards)	JA	-	89	-	°C/Watt