CS5330A/31A

8-Pin, Stereo A/D Converter for Digital Audio

Features

- Single +5 V Power Supply
- 18-Bit Resolution
- 94 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  - 0.05dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 150 mW
  - Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz

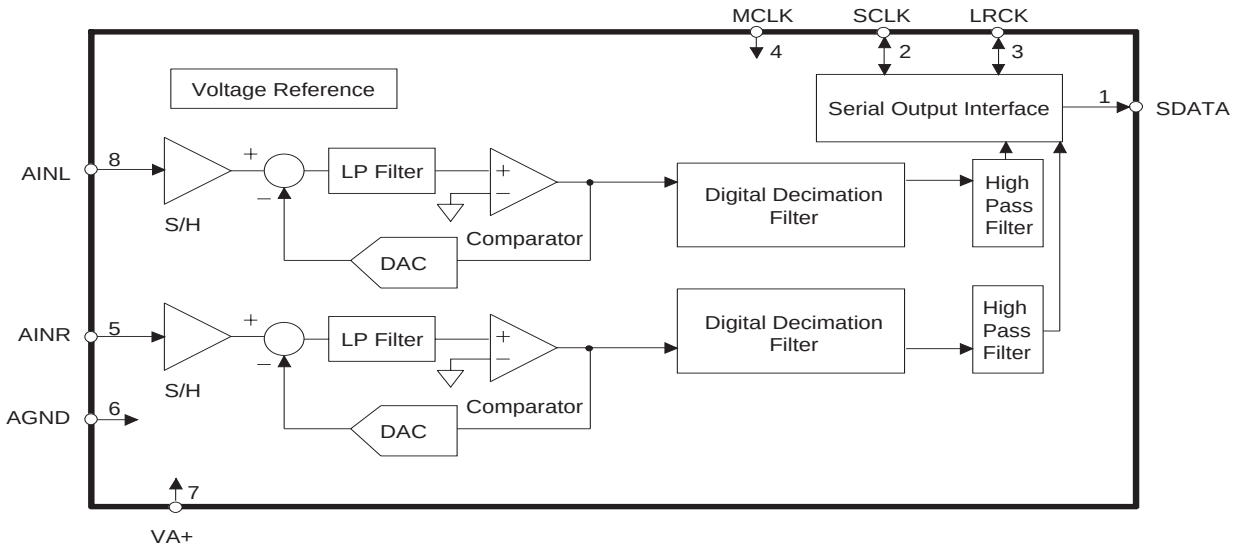
General Description

The CS5330A/31A is a complete stereo analog-to-digital converter that performs anti-alias filtering, sampling and analog-to-digital conversion generating 18-bit values for both left and right inputs in serial form. The output sample rate can be infinitely adjusted between 2 kHz and 50 kHz.

The CS5330A/31A operates from a single +5 V supply and requires only 150 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 128X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband to 21.7 kHz, 0.05 dB passband ripple and >80 dB stopband rejection. The device also contains a high-pass filter to remove DC offsets.

The device is available in an 8-pin SOIC package in both Commerical (-10° to +70° C) and Automotive grades (- 40° to +85° C). Please refer to "Ordering Information" on page 16 for complete details.



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1. PIN DESCRIPTIONS

Pin Name	#	Pin Description
SDATA	1	**Audio Serial Data Output** (*Output*) **-** Two's complement MSB-first serial data is output on this pin. A 47 kΩ resistor on this pin will place the CS5330A/31A into Master Mode.
SCLK	2	**Serial Data Clock** (*Input/Output*) **-** SCLK is an input clock at any frequency from 32x to 64x the output word rate. SCLK can also be an output clock at 64x if in the Master Mode. Data is clocked out on the falling edge of SCLK.
LRCK	3	**Left/Right Clock** (*Input/Output*) **-** LRCK selects the left or right channel for output on SDATA. The LRlo an Theowng Tw006 Tc0.0047 Tw[resistor)6(on this)-5.4( )6(pin will)6(plac)-5.4(e th)]TJ13.8855 1

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(AGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Unit
Analog Supply Voltage		VA+	4.75	5.0	5.25	V
Ambient Operating Temperature (Power Applied)	KS, KSZ BS, DS	T_A	-10 -40	- -	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS

(AGND = 0V, all voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Unit
Analog Supply Voltage		VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Note 2)	Iin	-	-	±10	mA
Analog Input Voltage	(Note 3)	VINA	-0.7	-	VA+0.7	V
Digital Input Voltage	(Note 3)	VIND	-0.7	-	VA+0.7	V
Ambient Temperature (power applied)		TA	-55	-	+125	°C
Storage Temperature		Tstg	-65	-	+150	°C

Notes:

1. Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any Pin except supplies. Transient current of up to +/- 100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS

(-1 dBFS Input Sinewave, 997 Hz; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+)

Parameter	Symbol	5330A/31A-KS/KSZ Min	Typ	Max	5331A-DSZ Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range A-weighted		88	94	-	86	94	-	dB
unweighted		86	92	-	84	92	-	dB
Total Harmonic Distortion + Noise (Note 4)	THD+N							
-1 dB		-	-84	75	-	-84	75	dB
-20 dB		-	-72	66	-	-72	66	dB
-60 dB		-	-32	26	-	-32	26	dB
Total Harmonic Distortion -1 dB	THD	-	0.003	0.02	-	0.003	0.2	%
Interchannel Phase Deviation		-	0	-	-	0	-	Degree
Interchannel Isolation (dc to 20 kHz)		-	90	-	-	90	-	dB
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Error		-	-	±10	-	-	±10	%
Gain Drift		-	150	-	-	150	-	ppm/°C
Offset Error (Note 5)		-	-	0	-	-	0	LSB
Analog Input								
Full-scale Input Voltage	VIN	3.6	4.0	4.4	3.6	4.0	4.4	Vpp
Input Impedance (Fs = 48 kHz)	ZIN	-	100	-	-	100	-	kΩ
Input Bias Voltage		2.2	2.4	2.6	2.2	2.4	2.6	V
Power Supplies								
Power Supply Current VA+	IA+	-	30	42	-	30	42	mA
Power down		-	100	1000	-	100	1000	µA
Power Dissipation Normal		-	150	220	-	150	220	mW
Power down		-	0.5	5.25	-	0.5	5.25	mW
Power Supply Rejection Ratio	PSRR	-	50	-	-	50	-	dB
* Refer to Parameter Definitions at the end of this data sheet.								

4. Referenced to typical full-scale input voltage.
5. Internal highpass filter removes offset.

DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at Io = -20 µA	V_{OH}	VA-1.0	-	-	V
Low-Level Output Voltage at Io = 20 µA	V_{OL}	-	-	0.4	V
Input leakage Current	I_{in}	-	-	±10.0	µA

DIGITAL FILTER CHARACTERISTICS

(FS = 48 kHz)

Parameter			Symbol	Min	Typ	Max	Unit
Passband	(0.05)	(Note 6)		0.02	-	21.7	kHz
Passband Ripple				-	-	±0.05	dB
Stopband		(Note 6)		29	-	6115	kHz
Stopband Attenuation		(Note 7)		80	-	-	dB
Group Delay		(Note 8)	t_{gd}	-	15/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0	µs
High Pass Filter Characteristics							
Frequency Response:	-3 dB -0.1 dB	(Note 6)		- -	3.7 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 6)		-	10	-	Degree
Passband Ripple				-	-	0	dB

6. Filter characteristics scale with output sample rate.
7. The analog modulator samples the input at 6.144 MHz for an output sample rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.7 kHz where n = 0,1,2,3…).
8. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312µs.

SWITCHING CHARACTERISTICS

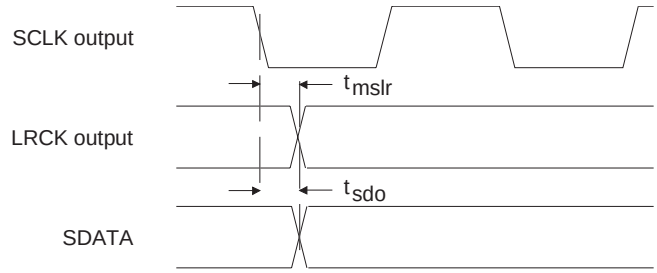
(Inputs: Logic 0 = 0V, Logic 1 = VA+; C_L = 20 pF) Switching characteristics are guaranteed by characterization.

Parameter		Symbol	Min	Typ	Max	Unit
Output Sample Rate		Fs	2	-	50	kHz
MCLK Period	MCLK/LRCK = 256	t_{clkw}	78	-	1000	ns
MCLK Low	MCLK/LRCK = 256	t_{clkl}	31	-	1000	ns
MCLK High	MCLK/LRCK = 256	t_{clkh}	31	-	1000	ns
MCLK Period	MCLK/LRCK = 384	t_{clkw}	52	-	1000	ns
MCLK Low	MCLK/LRCK = 384	t_{clkl}	20	-	1000	ns
MCLK High	MCLK/LRCK = 384	t_{clkh}	20	-	1000	ns
MCLK Period	MCLK/LRCK = 512	t_{clkw}	39	-	1000	ns
MCLK Low	MCLK/LRCK = 512	t_{clkl}	13	-	1000	ns
MCLK High	MCLK/LRCK = 512	t_{clkh}	13	-	1000	ns
MASTER MODE						
SCLK falling to LRCK		t_{mslr}	-10	-	10	ns
SCLK falling to SDATA valid		t_{sdo}	-10	-	35	ns
SCLK Duty cycle			-	50	-	%
SLAVE MODE						
LRCK duty cycle			25	50	75	%
SCLK Period		t_{clkw}	(Note 9)	-	-	ns
SCLK Pulse Width Low		t_{clkl}	(Note 10)	-	-	ns
SCLK Pulse Width High		t_{clkh}	20	-	-	ns
SCLK falling to SDATA valid		t_{dss}	-	-	(Note 11)	ns
LRCK edge to MSB valid		t_{lrdss}	-	-	(Note 11)	ns
SCLK rising to LRCK edge delay		t_{slr1}	20	-	-	ns
LRCK edge to rising SCLK setup time		t_{slr2}	(Note 11)	-	-	ns

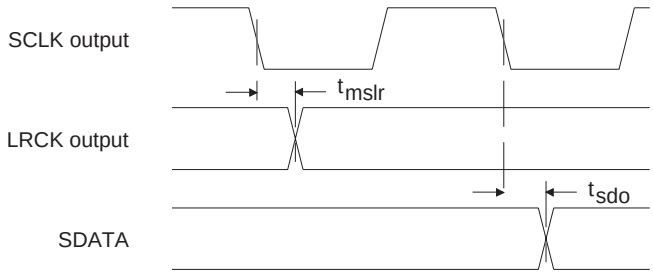
9. $\frac{1}{64\ F_s}$

10. $\frac{1}{128\ F_s}$ - 15 ns

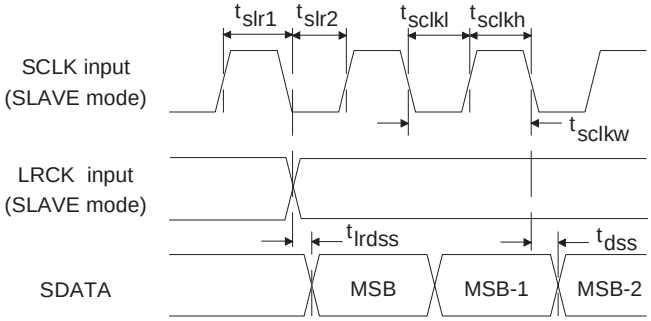
11. $\frac{1}{256\ F_s}$ + 5 ns



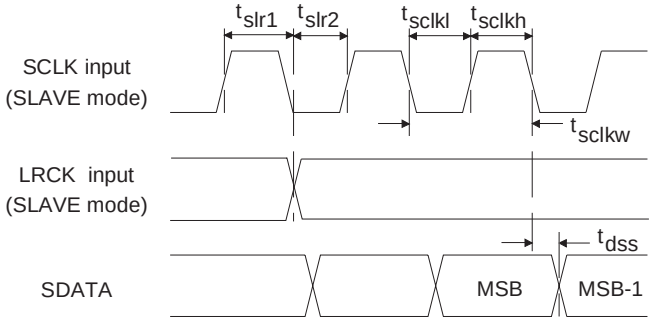
SCLK to SDATA LRCK - MASTER mode (CS5330A)



SCLK to SDATA LRCK - MASTER mode (CS5331A)



SCLK to LRCK & SDATA - SLAVE mode (CS5330A)



SCLK to LRCK & SDATA - SLAVE mode (CS5331A)

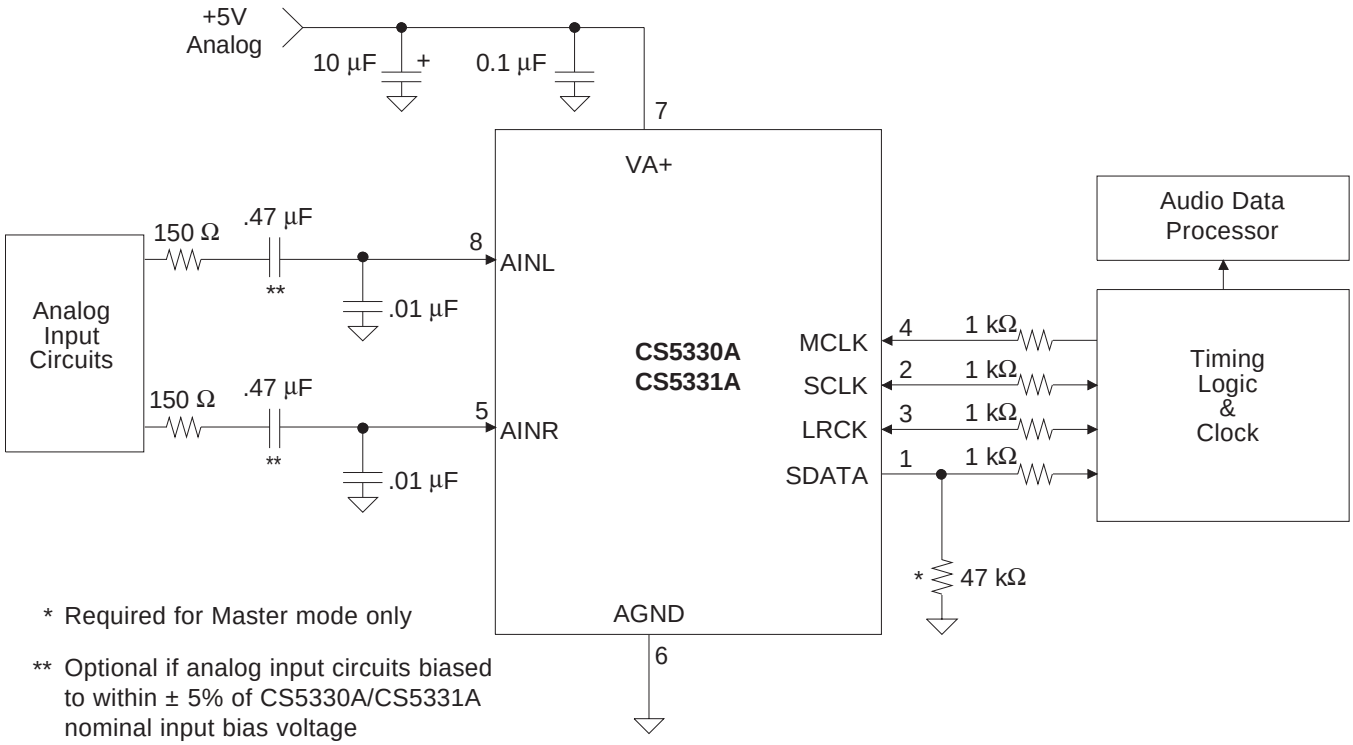


Figure 1. Typical Connection Diagram

3. GENERAL DESCRIPTION

The CS5330A and CS5331A are 18-bit, 2-channel Analog-to-Digital Converters designed for digital audio applications. Each device uses two one-bit delta-sigma modulators which simultane-ously sample the analog input signals at 128 times the output sample rate (Fs). The resulting serial bit streams are digitally filtered, yielding pairs of 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters and do not require external sample-and-hold amplifiers or a voltage reference.

The CS5330A and CS5331A differ only in the output serial data format. These formats are dis-cussed in the following sections and shown in Figures 2 and 3.

An on-chip voltage reference provides for a single-ended input signal range of 4.0 Vpp. Output data is available in serial form, coded as 2's complement 18-bit numbers. Typical power con-sumption is 150 mW which can be further reduced to 0.5 mW using the Power-Down mode.

For more information on delta-sigma modulation, see the references at the end of this data sheet.

3.1 System Design

Very few external components are required to support the ADC. Normal power supply decou-pling components and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3.1.1 Master Clock

The master clock (MCLK) runs the digital filter and is used to generate the delta-sigma modula-tor sampling clock. Table 1 shows some common master clock frequencies. The output sample rate is equal to the frequency of the Left / Right Clock (LRCK). The serial nature of the output data results in the left and right data words being read at different times. However, the words within an LRCK cycle represent simultaneously sampled analog inputs. The serial clock (SCLK) shifts the digitized audio data from the internal data registers via the SDATA pin.

3.1.2 Serial Data Interface

LRCK (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

The CS5330A and CS5331A can be operated in either Master mode, where SCLK and LRCK are outputs, or SLAVE mode, where SCLK and LRCK are inputs.

3.1.3 Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from MCLK. The CS5330A/31A will divide MCLK by 4 to generate a SCLK which is 64× Fs and by 256 to generate LRCK. The CS5330A and CS5331A can be placed in the Master mode with a 47 kohm pull-down resistor on the SDATA pin as shown in Figure 1.

3.1.4 Slave Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLK and be equal to Fs. The frequency of SCLK should be equal to 64x LRCK, though other frequencies are possible.

MCLK frequencies of 256x, 384x, and 512x Fs are supported. The ratio of the applied MCLK to LRCK is automatically detected during power-up and internal dividers are set to generate the ap-propriate internal clocks.

3.1.5 CS5330A

The CS5330A data output format is shown in Figure 2. Notice that the MSB is clocked by the transition of LRCK and the remaining seventeen data bits are clocked by the falling edge of SCLK. The data bits are valid during the rising edge of SCLK.

3.1.6 CS5331A

The CS5331A data output format is shown in Figure 3. Notice the one SCLK period delay be-tween the LRCK transitions and the MSB of the data. The falling edges of SCLK cause the ADC to output the eighteen data bits. The data bits are valid during the rising edge of SCLK. LRCK is also inverted compared to the CS5330A interface. The CS5331A interface is compatible with I^2S.

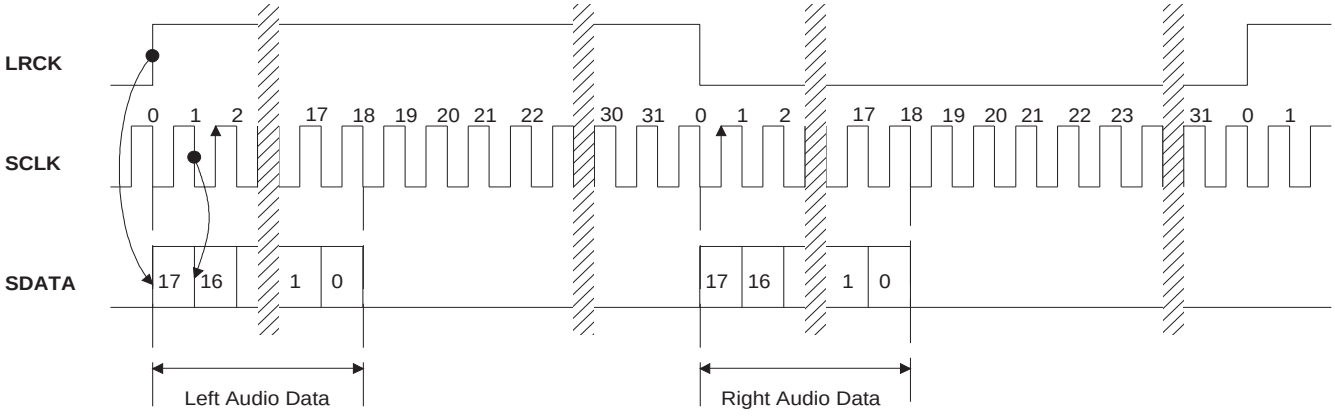


Figure 2. Data Output Timing-CS5330A

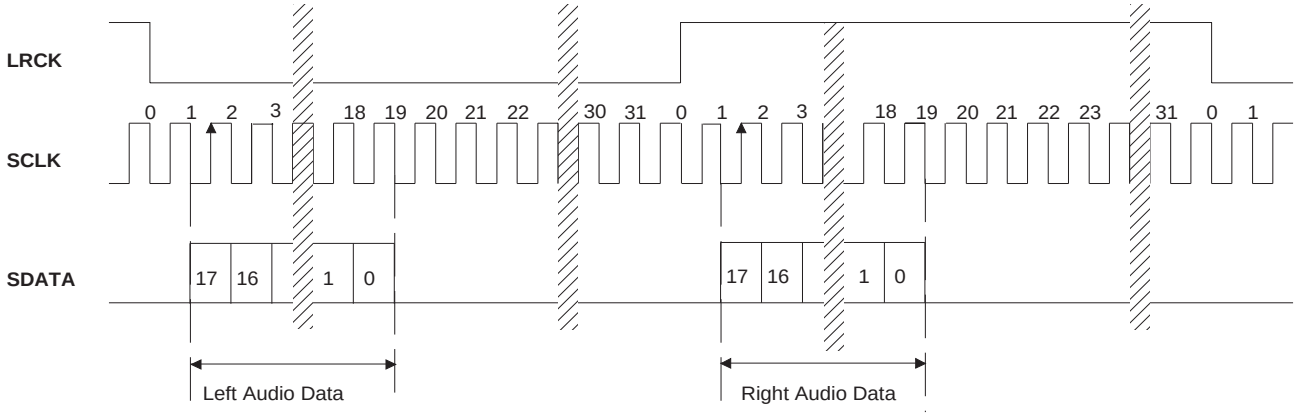


Figure 3. Data Output Timing - CS5331A (I²S Compatible)

3.1.7 Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented to the modula-tors via the AINR and AINL pins. Each analog input will accept a maximum of 4 Vpp centered at +2.4 V.

The CS5330A/31A samples the analog inputs at 128 × Fs, 6.144 MHz for a 48 kHz sample-rate. The digital filter rejects all noise above 29 kHz except for frequencies right around 6.144 MHz ±21.7 kHz (and multiples of 6.144 MHz). Most audio signals do not have significant energy at 6.144 MHz. Nevertheless, a 150 Ω resistor in series with each analog input and a 10 nF capacitor across the inputs will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. It is also important that the self-resonant frequency of the capacitor be well above the modulator sampling frequency. General purpose ceramics and film capacitors do not meet these requirements. However, NPO and COG capacitors are acceptable. If active circuitry precedes the ADC, it is recom-mended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with Fs.

3.1.8 High-Pass Filter

The operational amplifiers in the input circuitry driving the CS5330A/31A may generate a small DC offset into the A/D converter. The CS5330A/31A includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between de-vices in a multichannel system.

The characteristics of this first-order high pass filter are outlined in the “Digital Filter Characteristics” on page 6

3.1.9 Initialization and Power-Down

The Initialization and Power-Down sequence is shown in Figure 4. Upon initial power-up, the digital filters and delta-sigma modulators are reset and the internal voltage reference is powered down. The device will remain in the Initial Power-Down mode until MCLK is presented. Once MCLK is available, the CS5330A/31A will make a master/slave mode decision based upon the presence/absence of a 47 kohm pull-down resistor on SDATA as shown in Figure 1. The master/slave decision is made during initial power-up as shown in Figure 4.

In master mode, SCLK and LRCK are outputs where the MCLK/LRCK frequency ratio is 256x. LRCK will appear as an output 127 MCLK cycles into the initialization sequence. At this time, power is applied to the internal voltage reference and the analog inputs will move to approximately 2.4 Volts. SDATA is static low during the initialization and high pass filter settling sequence, which requires 11,265 LRCK cycles (235 ms at a 48 kHz output sample rate).

In slave mode, SCLK and LRCK are inputs where the MCLK/LRCK frequency ratio must be either 256x, 384x, or 512x. Once the MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. At this time, power is applied to the internal voltage reference and the analog inputs will move to approximately 2.4 Volts. SDATA is static high during the initialization and high pass filter settling sequence, which requires 11,265 LRCK cycles (235 ms at a 48 kHz sample rate).

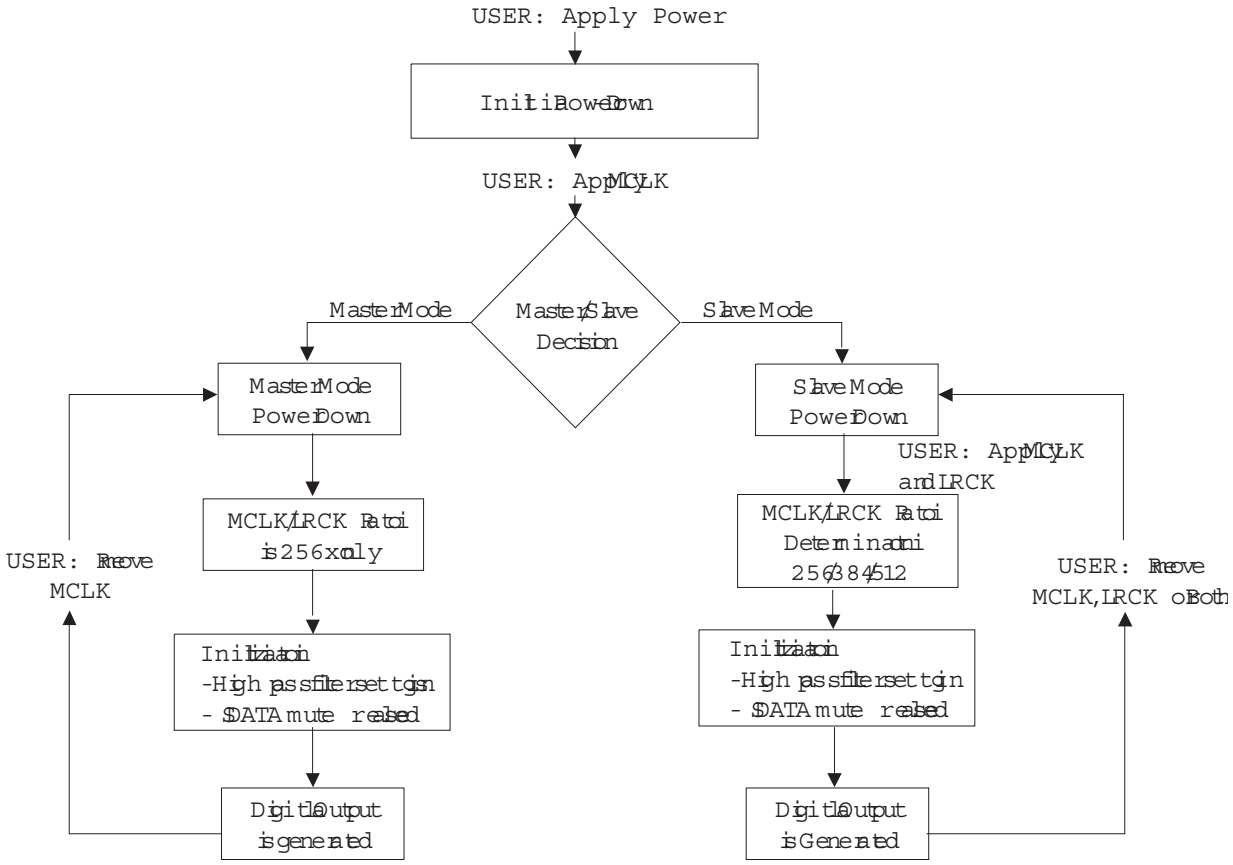


Figure 4. CS5330A/31A Initialization and Power-Down Sequence

The CS5330A and CS5331A have a Power-Down mode wherein typical consumption drops to 0.5 mW. This is initiated when a loss of clock is detected on either the LRCK or MCLK pins in Slave Mode, or the MCLK pin in Master Mode. The initialization sequence will begin when MCLK, and LRCK for slave mode, are restored. In slave mode power-down, the CS5330A and CS5331A will adapt to changes in MCLK/LRCK frequency ratio during the initialization sequence. It is recommended that clocks not be applied to the device prior to power supply settling. A reset circuit may be implemented by gating the MCLK signal.

3.1.10 Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5V supply. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs. The printed circuit board layout should have separate analog and digital regions and ground planes. An evaluation board, CDB5330A or CDB5331A, is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the CS5330A and CS5331A.

3.1.11 Digital Filter

Figures 5 through 8 show the attenuation characteristics of the digital filter included in the ADC. The filter response scales linearly with sample rate. The x-axis has been normalized to Fs, and can be scaled by multiplying the x-axis by the system sample rate, i.e. 48 kHz.

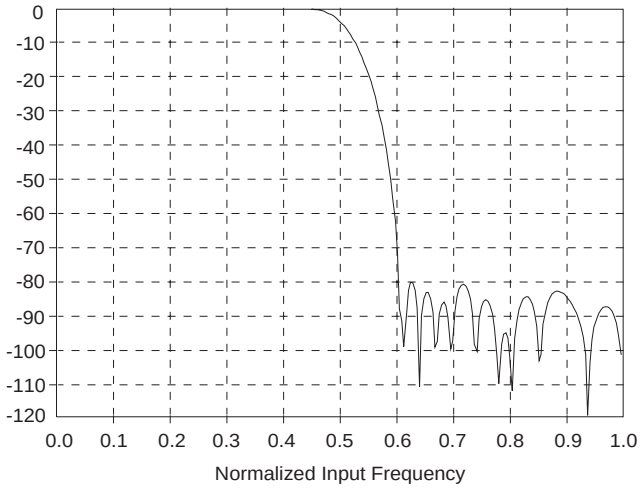


Figure 5. CS5330A/31A Digital Filter Stopband Rejection

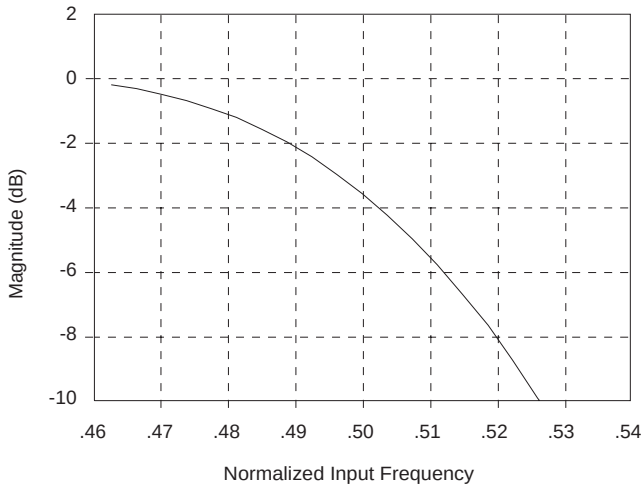


Figure 6. CS5330A/31A Digital Filter Transition Band

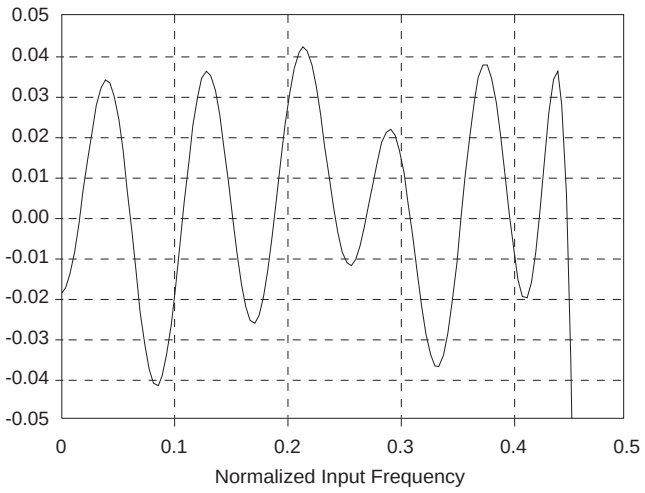


Figure 7. CS5330A/31A Digital Filter Passband Ripple

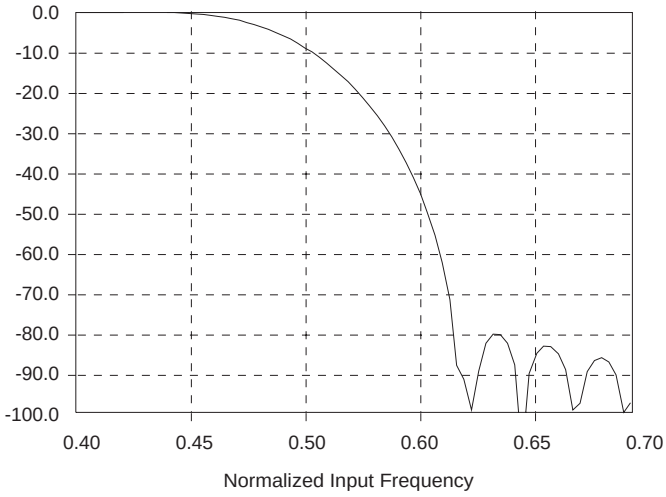


Figure 8. CS5330A/31A Digital Filter Transition Band

4. PARAMETER DEFINITIONS

Resolution

The total number of possible output codes is equal to 2 N, where N = the number of bits in the output word for each channel.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion+Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

Interchannel Phase Deviation

The phase difference between the left and right channel sampling times.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test AC grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation of the measured full-scale amplitude from the ideal full-scale amplitude value.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

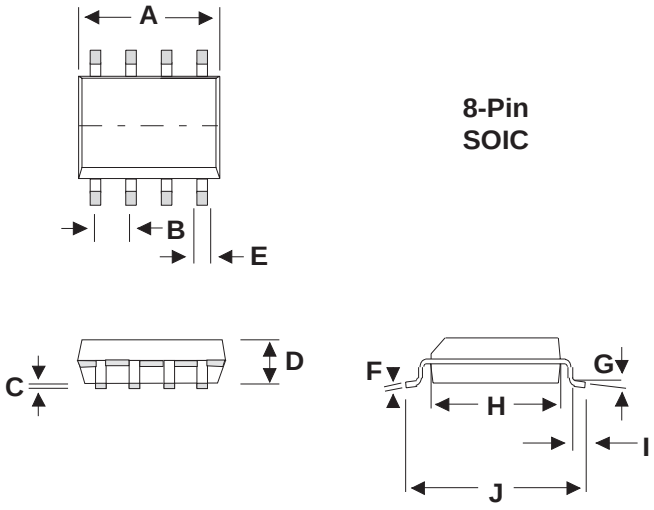
Bipolar Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in LSBs.

5. REFERENCES

1. *Area Efficient Decimation Filter for an 18-Bit Delta- Sigma ADC*, by K. Lin and J.J. Paulos. Paper presented at the 98th Convention of the Audio Engineering Society, February 1995.
2. *An 18-Bit, 8-Pin Stereo Digital-to-Analog Converter*, by J.J. Paulos, A.W. Krone, G.D. Kamath and S.T. Dupuie. Paper presented at the 97th Convention of the Audio Engineering Society, November 1994.
3. *An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example*, by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
4. *The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's*, by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.
5. *A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio*, by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

6. PACKAGE DESCRIPTIONS



8-Pin SOIC

	Millimeters		Inches	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	5.15	5.35	0.203	0.210
B	1.27 TYP		0.050 TYP	
C	0	0.25	0	0.010
D	1.77	1.88	0.070	0.074
E	0.33	0.51	0.013	0.020
F	.15	0.25	0.006	0.010
G	0°	8°	0°	8°
H	5.18	5.4	0.204	0.213
I	0.48	0.76	0.019	0.030
J	7.67	8.1	0.302	0.319

Note: The EIAJ Package is not a standard JEDEC package size.

7. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5330A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	NO	Commercial	-10° to +70° C	Bulk	CS5330A-KS
						Tape & Reel	CS5330A-KSR
CS5331A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	NO	Commercial	-10° to +70° C	Bulk	CS5331A-KS
						Tape & Reel	CS5331A-KSR
CS5330A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	YES	Commercial	-10° to +70° C	Bulk	CS5330A-KSZ
						Tape & Reel	CS5330A-KSZR
CS5331A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	YES	Commercial	-10° to +70° C	Bulk	CS5331A-KSZ
						Tape & Reel	CS5331A-KSZR
CS5330A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	NO	Automotive	-40° to +85° C	Bulk	CS5330A-BS
						Tape & Reel	CS5330A-BSR
CS5331A	8-pin, Stereo A/D Converter for Digital Audio	8-SOIC	YES	Automotive	-40° to +85° C	Bulk	CS5331A-DSZ
						Tape & Reel	CS5331A-DSZR

8. REVISION HISTORY

Release	Changes
F5	Updated Ordering Information

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.