CS5360

24-Bit Stereo A/D Converter for Digital Audio

Features

- 24 Bit Conversion
- 105 dB Dynamic Range
- -95 dB THD+N
- 128X Oversampling
- Fully Differential Inputs
- Linear Phase Digital Anti-Alias Filtering
  - 21.7 kHz passband (Fs = 48kHz)
  - 85 dB stop band attenuation
  - 0.0025 dB pass band ripple
- High Pass Filter - DC Offset Removal
- Peak Signal Level Detector
  - High Resolution and Bar Graph Modes
- Pin Compatible with CS5334 and CS5335

Description

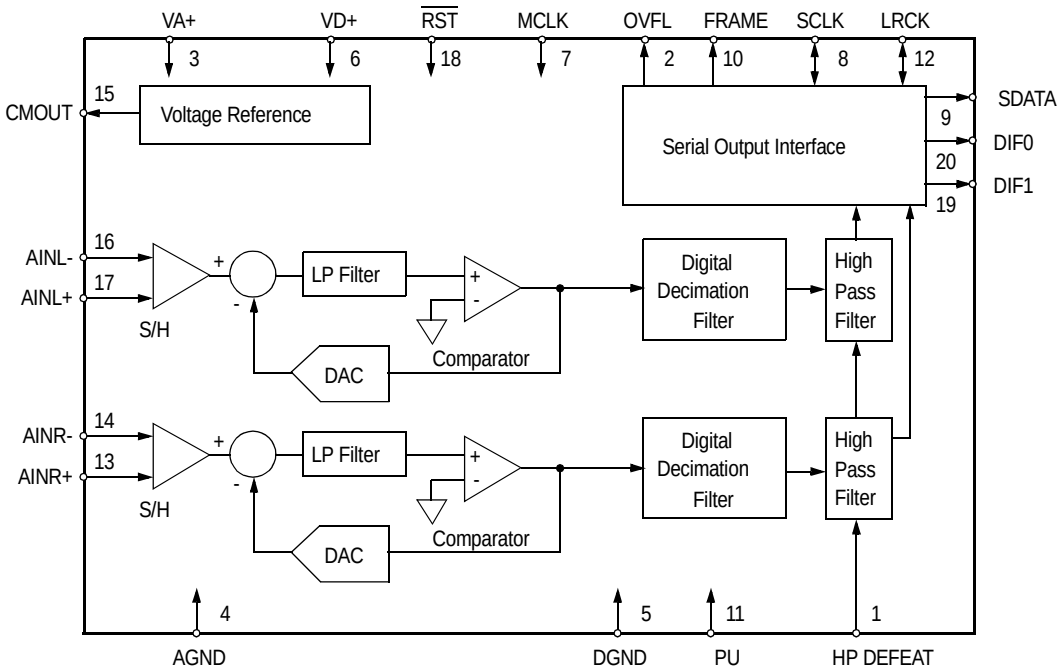
The CS5360 is a 2-channel, single +5 V supply, 24-bit analog-to-digital converter for digital audio systems. The CS5360 performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5360 uses 4th-order, delta-sigma modulation with 128X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. This ADC uses a differential architecture which provides excellent noise rejection.

The CS5360 has a filter passband to 21.7 kHz. The filter has linear phase, 0.0025 dB passband ripple, and >85 dB stopband rejection. An on-chip high pass filter is also included to remove DC offsets.

ORDERING INFORMATION

CS5360-KS	-10° to 70°C	20-pin Plastic SSOP
CS5360-BS	-40° to 85°C	20-pin Plastic SSOP



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(T_A = 25 °C; VA+ = VD+ = 5 V; -1 dB Input sinewave, 997 Hz; Fs = 48 kHz; MCLK = 12.288 MHz; SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified; Logic 0 = 0 V, Logic 1 = VD+)

Parameter	Symbol	5360-KS Min	5360-KS Typ	5360-KS Max	5360-BS Min	5360-BS Typ	5360-BS Max	Units
Temperature Range	T_A	-10 to +70			-40 to +85			°C
Dynamic Performance								
Dynamic Range A-weighted		100 97	105 102	- -	95 92	105 102	- -	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
-1 dB		-	-95	-90	-	-95	-85	dB
-20 dB		-	-82	-77	-	-82	-72	dB
-60 dB		-	-42	-37	-	-42	-32	dB
Interchannel Phase Deviation		-	0.01	-	-	0.01	-	Degree
Interchannel Isolation (dc to 20 kHz)		-	105	-	-	105	-	dB
dc Accuracy								
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB
Gain Error		-	-	±5	-	-	±5	%
Gain Drift		-	200	-	-	200	-	ppm/°C
Offset Error with HPF		-	0	-	-	0	-	LSB
HP defeat with CAL		-	±100	-	-	±100	-	LSB
Analog Input								
Input Voltage Range (Differential)	VIN	1.9	2.0	2.1	1.9	2.0	2.1	Vrms
Input Impedance	ZIN	-	30	-	-	30	-	kΩ
Input Bias Voltage		-	2.2	-	-	2.2	-	V
Common Mode Rejection Ratio	CMRR	-	60	-	-	60	-	dB
Power Supplies								
Power Supply Current I_A		-	40	45	-	40	45	mA
I_D		-	25	30	-	25	30	mA
Power Down (I_A + I_D)		-	0.5	-	-	0.5	-	mA
Power Dissipation Normal		-	325	375	-	325	375	mW
Power Down		-	2.5	-	-	2.5	-	mW
Power Supply Rejection Ratio		-	55	-	-	55	-	dB

Notes: 1. Referenced to nominal input level.

Specifications are subject to change without notice

DIGITAL FILTER CHARACTERISTICS (Note 2, T_A = 25 °C; VA+ = VD+ = 5 V ±5%; Fs = 48 kHz)

Parameter			Symbol	Min	Typ	Max	Unit
Passband		(Note 3)		0.02	-	21.7	kHz
Passband Ripple				-	-	±0.0025	dB
Stopband		(Note 3)		26.3	-	6118	kHz
Stopband Attenuation		(Note 4)		85	-	-	dB
Group Delay (Fs = Output Sample Rate)			t_{gd}	-	32/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0	µs
High Pass Filter Characteristics							
Frequency Response	-3 dB -0.1 dB	(Note 3)		- -	0.9 20	- -	Hz
Phase Deviation	@20 Hz	(Note 3)		-	2.6	-	Degree
Passband Ripple				-	-	0	dB

Notes: 2. Filter response is not tested but is guaranteed by design.

3. Filter characteristics scale with output sample rate.

4. The analog modulator samples the input at 6.144 MHz for an output sample rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.7 kHz where n = 0, 1, 2, 3, ...).

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = VD+ = 5 V ±5%)

Parameter	Symbol	Min	Max	Unit
High-level Input Voltage	V_{IH}	2.4	-	V
Low-level Input Voltage	V_{IL}	-	0.8	V
High-level Output Voltage at Io = -20 µA	V_{OH}	(VD+) - 1.0	-	V
Low-level Output Voltage at Io = 20 µA	V_{OL}	-	0.4	V
Input Leakage Current	I_{in}	-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC Power Supply		VA+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{INA}	-0.7	(VA+) + 0.7	V
Digital Input Voltage	(Note 6)	V_{IND}	-0.7	(VA+) + 0.7	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

6. The maximum over/under voltage is limited by the input extremes.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 5 V ±5%; Inputs: Logic 0 = 0 V, Logic 1 = VA+ = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Output Sample Rate		F_S	8.0	-	50	kHz
MCLK Period	MCLK / LRCK = 256	t_{clkw}	78	-	1953	ns
	MCLK / LRCK = 384		52	-	1302	
	MCLK / LRCK = 512		39	-	976	
MCLK Low	MCLK / LRCK = 256	t_{clkl}	31	-	-	ns
	MCLK / LRCK = 384		20	-	-	
	MCLK / LRCK = 512		15	-	-	
MCLK High	MCLK / LRCK = 256	t_{clkh}	31	-	-	ns
	MCLK / LRCK = 384		20	-	-	
	MCLK / LRCK = 512		15	-	-	
Peak Update Pulse Width		pu_{pulse}	20	-	-	ns
Master Mode						
SCLK Falling to LRCK	(Note 7)	t_{mslr}	-10	-	10	ns
SCLK Falling to SDATA Valid	(Note 7)	t_{sdo}	-10	-	35	ns
SCLK Duty Cycle			-	50	-	%
SCLK Falling to Frame Valid	(Note 7)	t_{sfo}	-10	-	Note 8	ns
LRCK Edge to OVFL Valid		t_{ovfl}	-10	-	30	ns
LRCK Edge to OVFL Edge Delay		t_{ovfl}	-10	-	Note 12	ns
Slave Mode						
LRCK Duty Cycle			25	50	75	%
SCLK Period		t_{sclkw}	Note 9	-	-	ns
SCLK Pulse Width Low	(Note 10)	t_{sclkl}	Note 13	-	-	ns
SCLK Pulse Width High	(Note 11)	t_{sclkh}	50	-	-	ns
SCLK Falling to SDATA Valid	(Note 7)	t_{dss}	-	-	Note 13	ns
LRCK Edge to MSB Valid		t_{lrdss}	-	-	Note 13	ns
SCLK Rising to LRCK Edge Delay	(Note 14)	t_{slr1}	50	-	-	ns
LRCK Edge to Rising SCLK Setup Time	(Note 14)	t_{slr2}	Note 13	-	-	ns
SCLK Falling to Frame Delay		t_{sfo}	-	-	Note 15	ns

Notes:
7. SCLK Rising for Mode 1
8. $\frac{1}{(1024)(F_S)} + 30$ ns
9. $\frac{1}{(96)(F_S)}$
10. Pulse Width High for Mode 1
11. Pulse Width Low for Mode 1
12. $\frac{1}{(512)(F_S)} + 20$ ns
13. $\frac{1}{(512)(F_S)} + 50$ ns
14. SCLK Falling for Mode 1
15. $\frac{1}{(384)(F_S)} + 35$ ns

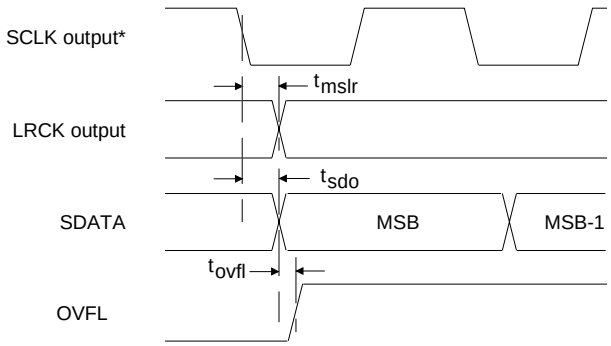


Figure 1. SCLK to SDATA & LRCK - MASTER Mode Format 0 and 1

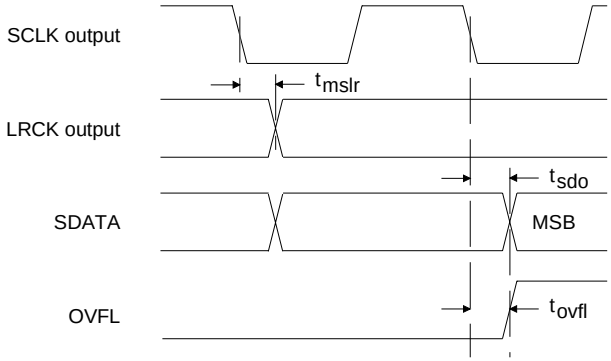


Figure 2. SCLK to SDATA & LRCK - MASTER Mode Format 2

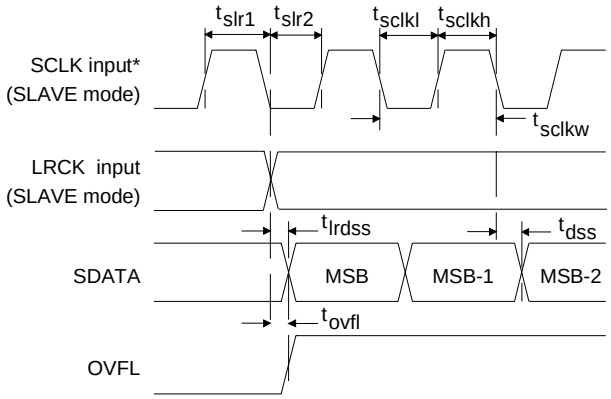


Figure 3. SCLK to LRCK & SDATA - SLAVE Mode Format 0 & 1

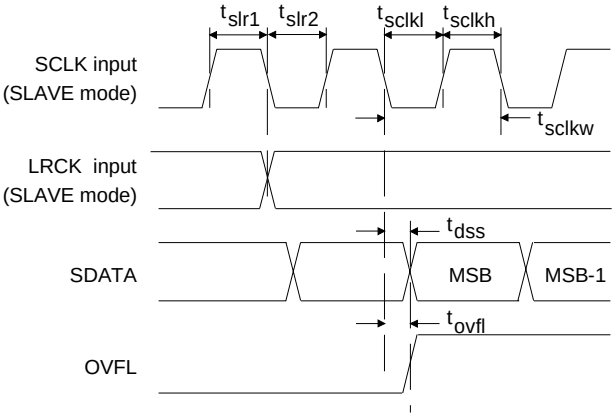


Figure 4. SCLK to LRCK & SDATA - SLAVE Mode Format 2

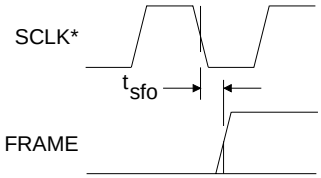


Figure 5. SCLK to Frame Delay

* SCLK is inverted in Format 1

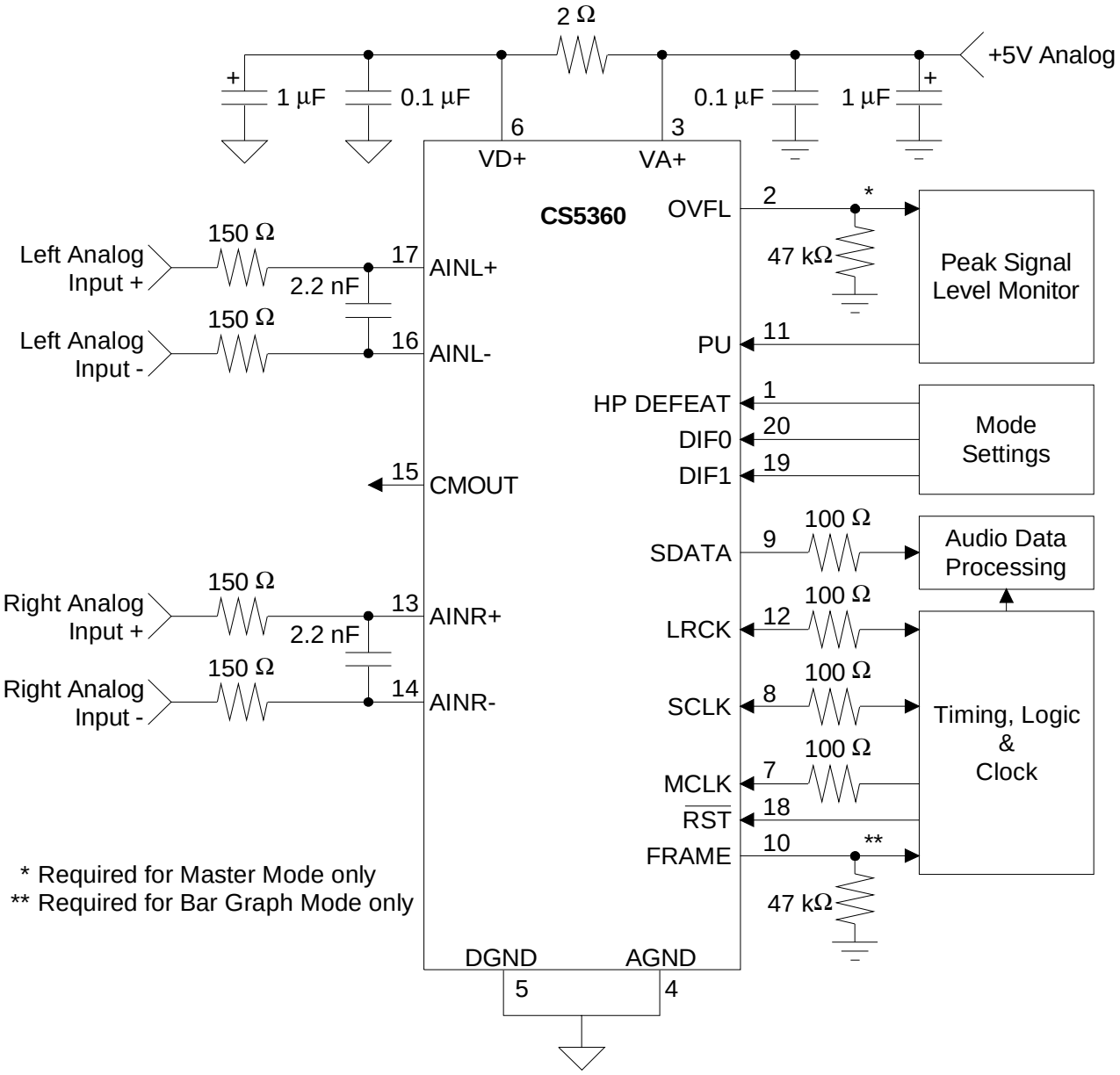


Figure 6. Typical Connection Diagram

2. SYSTEM DESIGN

The CS5360 is a 24-bit, 2-channel analog-to-digital converter designed for digital audio applications. This device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at 128 times the output sample rate (Fs). The resulting serial bit streams are digitally filtered, yielding a pair of 24-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and does not require external sample-and-hold amplifiers or a voltage reference. Very few external components are required to support this ADC. Normal power supply decoupling components and a resistor and capacitor on each input for anti-aliasing are the only external components required, as shown in Figure 6.

An on-chip voltage reference provides for a differential input signal range of 2.0 Vrms. Output data is available in serial form, coded as 2's complement, 24-bit numbers. Typical power consumption is 325 mW which can be reduced to 1.0 mW by using the power-down feature.

2.1 Master Clock

The master clock (MCLK) is the clock source for the delta-sigma modulator and digital filters. In Master Mode, the frequency of this clock must be 256x Fs. In SlaveMode, the master clock must be either 256x, 384x or 512x Fs. Table 1 shows some common master clock frequencies.

LRCK (kHz)	MCLK (MHz)		
	256 X	384 X	512 X
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

3. SERIAL DATA INTERFACE

The CS5360 supports three serial data formats, including I^2S, selected via the digital interface format pins DIF0 and DIF1. The digital interface format determines the relationship between the serial data, left/right clock and serial clock. Table 2 lists the three formats and their associated figure number. The serial data interface is accomplished via the serial data output, SDATA, serial data clock, SCLK, and the left/right clock, LRCK.

DIF1	DIF0	FORMAT	FIGURE
0	0	0	8
0	1	1	9
1	0	2	10
1	1	power-down	-

Table 2. Digital Input Formats

3.1 Serial Data

The serial data block consists of 24 bits of audio data presented in 2's-complement format with the MSB-first followed by 8 Peak Signal Level, PSL, bits as shown in Figure 7. The data is clocked from SDATA by the serial clock and the channel is determined by the Left/Right clock.

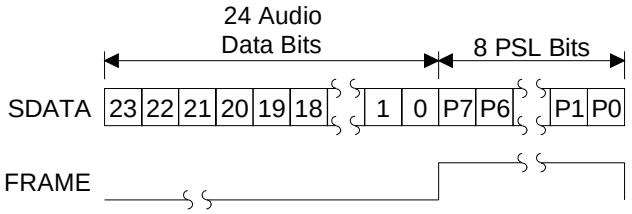
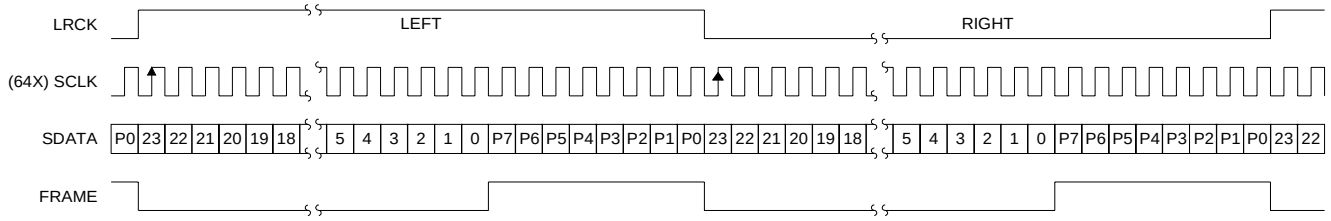


Figure 7. Data Block and Frame

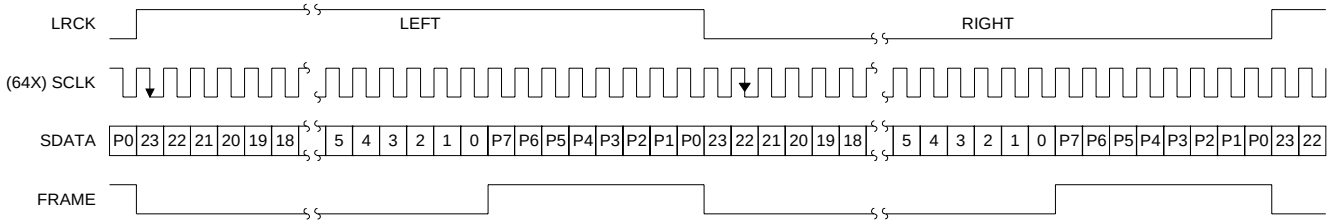
3.2 Serial Clock

The serial clock shifts the digital audio data from the internal data registers via the SDATA pin. SCLK is an output in Master Mode. Internal dividers will divide the master clock by 4 to generate a serial clock which is 64x Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48x and 96x Fs. However, the serial clock must be a minimum of 64x Fs to access the Peak Signal Level bits.



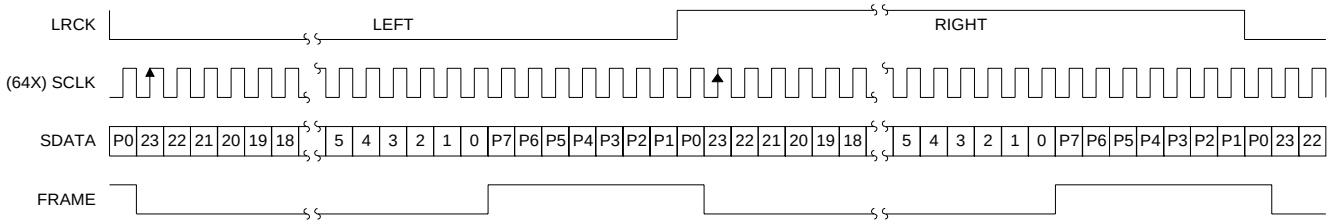
MASTER	SLAVE
24-Bit Left Justified Data	24-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x, 384x, or 512x Fs

Figure 8. Serial Data Format 0



MASTER	SLAVE
l Data	24-Bit Left Justified Data
ıg Edge of 64x SCLK	Data Valid on Falling Edge of SCLK
6x Fs	MCLK equal to 256x, 384x, or 512x Fs

Figure 9. Serial Data Format 1



MASTER	SLAVE
I^2S 24-Bit Left Justified Data	I^2S 24-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x Fs	MCLK equal to 256x, 384x, or 512x Fs

Figure 10. Serial Data Format 2

3.3 Left / Right Clock

The Left/Right clock determines which channel, left or right, is to be output on SDATA. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to the output sample rate, Fs.

3.4 Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the Master Clock. Internal dividers will divide MCLK by 4 to generate a SCLK which is 64x Fs and by 256 to generate a LRCK which is equal to Fs. Master mode is only supported with a 256x master clock. The CS5360 is placed in the Master mode with a 47 kΩ pull-down resistor on the OVFL pin.

3.5 Slave Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLK and be equal to Fs. The serial clock is typically between 64x and 96x Fs. A 48x Fs serial clock is possible though will not allow access to the Peak Signal Level bits. Master clock frequencies of 256x, 384x and 512x Fs are supported. The ratio of the applied master clock to the left/right clock is automatically detected during power-up and internal dividers are set to generate the appropriate internal clocks.

3.6 Analog Connections

Figure 6 shows the analog input connections. The analog inputs are presented to the modulators via the AINR+/- and AINL+/- pins. Each analog input pin will accept a maximum of 1Vrms centered at +2.2 Volt as shown in Figure 11. Input signals can be AC or DC coupled and the CMOUT output may be used as a reference for DC coupling. However, CMOUT is not buffered, and the maximum current is 10 µA.

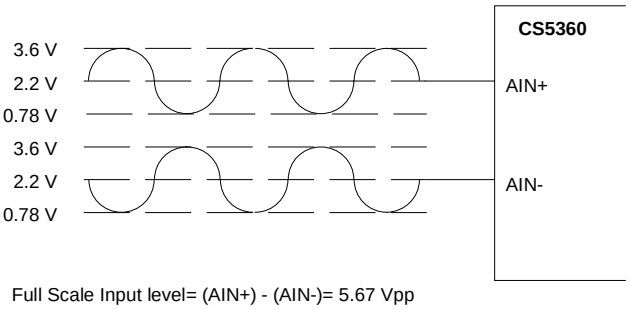


Figure 11. Full Scale Input Levels

The CS5360 samples the analog inputs at 128x Fs, 6.144MHz for a 48kHz sample-rate. The digital filter rejects all noise above 26.3kHz except for frequencies right around 6.144MHz ±21.7kHz (and multiples of 6.144MHz). Most audio signals do not have significant energy at 6.144MHz. Nevertheless, a 150 Ω resistor in series with each analog input and a 2.2 nF capacitor across the inputs will attenuate any noise energy at 6.144MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. NPO and COG capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with the sample rate.

3.7 High Pass Filter

The operational amplifiers in the input circuitry driving the CS5360 may generate a small DC offset into the A/D converter. The CS5360 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. The high pass filter can be disabled with the HP DEFEAT pin.

The high pass filter works by continuously subtracting a measure of the dc offset from the output of the decimation filter. If the HP DEFEAT pin is

taken high during normal operation, the current value of the dc offset register is frozen and this dc offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system calibration by:

1) removing the signal source (or grounding the input signal) at the input to the subsystem containing the CS5360,
2) running the CS5360 with the HP DEFEAT pin low (high pass filter enabled) until the filter settles (approximately 1 second), and
3) taking the HP DEFEAT pin high, disabling the high pass filter and freezing the stored dc offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5360.

The characteristics of the first-order high pass filter are outlined below for an output sample rate of 48 kHz. This filter response scales linearly with sample rate.

Frequency response:	-3 dB @ 0.9 Hz
	-0.01 dB @ 20 Hz
Phase deviation:	2.6 degrees @ 20 Hz
Passband ripple:	None

4. INPUT LEVEL MONITORING

The CS5360 includes independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels, prior to the digital limiter, and records these values in the Active registers. This information can be transferred to the Output registers by a high to low transition on the Peak Update pin (PU) which will also reset the Active register. The Active register contains the peak signal level since the previous peak update request.

The 8-bit contents of the output registers are available in all interface modes and are present in the data block as shown in Figure 7. The monitoring function can be formatted to indicate either High Resolution Mode or Bar Graph Mode. The monitoring function is determined on power-up by the presence of a 47 kΩ pull-down resistor on FRAME. The addition of a 47 kΩ pull-down resistor on the FRAME pin sets the monitoring function to the Bar Graph mode.

4.1 High Resolution Mode

Bits P7-P0 indicate the peak input level since the previous peak update (or low transition on the Peak Update pin). If the full scale input level is exceeded (Bit P7 high), bits P5-P0 represent the peak value up to 3 dB above full-scale in 1 dB steps. If the ADC input level is less than full-scale, bits P5-P0 represent the peak value from -60 dB to 0 dB of full scale in 1 dB steps. The PSL outputs are accurate to within 0.25 dB. Bit P6 provides a coarse means of determining an ADC input idle condition. Bit P7 indicates an ADC overflow condition, if the ADC input level is greater than full-scale.

P7 - Overrange
0 - Analog input less than full-scale level
1 - Analog input greater than full-scale

P6 - Idle channel
0 - Analog input >-60 dB from full-scale
1 - Analog input <-60 dB from full-scale

P5 to P0 - Peak Signal Level Bits (1 dB steps)

Inputs <0 dB	P5 - P0
0 dB	000000
-1 dB	000001
-2 dB	000010
-60 dB	111100

Inputs >0 dB	P5 - P0
0 dB	000000
+1 dB	000001
+2 dB	000010
+3 dB	000011

Table 3. Peak Signal Level Bits - High Resolution Mode

4.2 Bar Graph Mode

This mode provides a decoded output format which indicates the peak Peak Signal Level in a "Bar Graph" format.

Input Level	P7 - P0
Overflow	11111111
0 dB to -3 dB	01111111
-3 dB to -6 dB	00111111
-6 dB to -10 dB	00011111
-10 dB to -20 dB	00001111
-20 dB to -30 dB	00000111
-30 dB to -40 dB	00000011
-40 dB to -60 dB	00000001
< - 60 dB	00000000

Table 4. P7 to P0 - Peak Signal Level Bits -Bar Graph Mode

4.3 Overflow

Overflow indicates analog input overrange for the Left and Right channels as of the last update request on the Peak Update pin. A value of 1 indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK.

4.4 Initialization

Upon initial power-up, the digital filters and delta-sigma modulators are reset and the internal voltage reference is powered down. The CS5360 will remain in the power-down mode until valid clocks are presented. A valid MCLK is required to exit power-down in Master Mode. However, in Slave Mode, MCLK and LRCK of the proper ratio are required to exit power-down. MCLK occurrences are also counted over one LRCK period to determine the MCLK / LRCK frequency ratio in Slave Mode. Power is then applied to the internal voltage reference, the analog inputs will move to approximately 2.2 V and output clocks will begin (Master Mode only). This process requires 32 periods of LRCK and is followed by the initialization sequence.

4.5 Initialization with High Pass Filter Enabled

28,672 LRCK cycles are required for the initialization sequence with the high pass filter enabled. This time is dominated by the settling time required for the high pass filter.

4.6 Initialization and Internal Calibration with High Pass Filter Disabled

If the HP DEFEAT pin is high (high pass filter disabled) during the initialization sequence, the CS5360 will perform an internal dc calibration by:

1) disconnecting the internal ADC inputs from the input pins,
2) connecting the (differential) ADC inputs to a common reference voltage,
3) running the high pass filter with a fast settling time constant,
4) freezing the dc offset register, and
5) reconnecting the internal ADC inputs to the input pins.

This procedure takes 4,160 cycles of LRCK. Unlike the system calibration procedure described in the High Pass Filter section, a dc calibration performed during start-up will only eliminate offsets internal to the CS5360, and should result in output codes which accurately reflect the differential dc signal at the pins.

4.7 Power-Down

The CS5360 has a power-down mode wherein typical consumption drops to 1.0 mW. This is initiated when a loss of clock is detected (either LRCK or MCLK in Slave Mode or MCLK in Master Mode), $\overline{RST}$ is enabled or DIF0 / DIF1 are at a logic 1. The initialization sequence will begin whenever valid clocks are restored, $\overline{RST}$ is disabled and DIF0 / DIF1 are restored. If the MCLK / LRCK frequency ratio changes during power-down, the CS5360 will adapt to these new operating conditions. However, only the $\overline{RST}$ method of power-down will include the Master/Slave decision in the initialization sequence.

4.8 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5360 requires careful attention to power supply and grounding arrangements to optimize performance. Figure6 shows the recommended power arrangements with VA+ connected to a clean +5volt supply. VD+ should be derived from VA+ through a 2 ohm resistor. VD+ should not be used to power additional digital circuitry. All mode pins which require VD+ should be connected to pin 6 of the CS5360. All mode pins which require DGND should be connected to pin 5 of the CS5360. AGND and DGND, Pins 4 and 5, should be connected together at the CS5360. DGND for the CS5360 should not be confused with the ground for the digital section of the system. The CS5360 should be positioned over the analog ground plane near the digital / analog ground plane split. The analog and digital ground planes must be connected elsewhere in the system. The CS5360 evaluation board, CDB5360, demonstrates this layout technique. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors should be located as near to the CS5360 as possible.

4.9 Digital Filter

Figures 12-15 show the performance of the digital filter included in the CS5360. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with the sample rate.

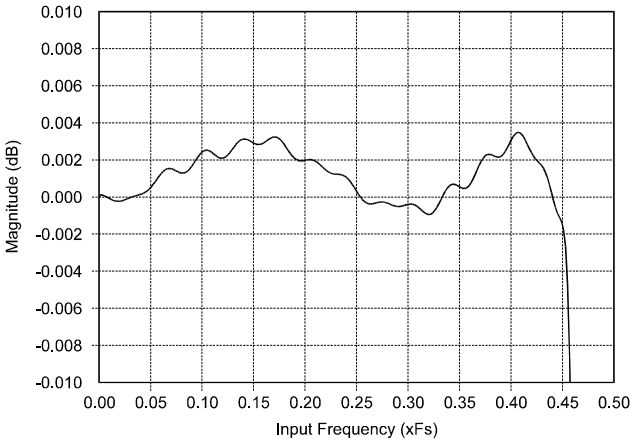


Figure 12. CS5360 Digital Filter Passband Ripple

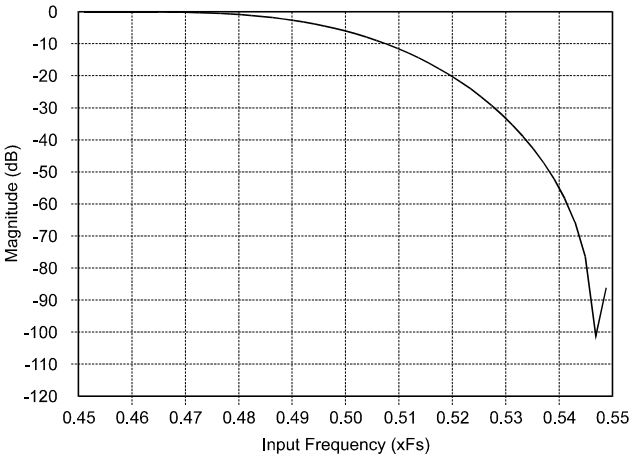
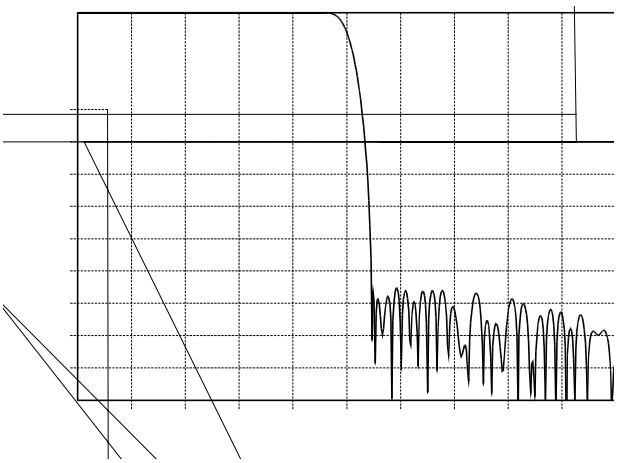
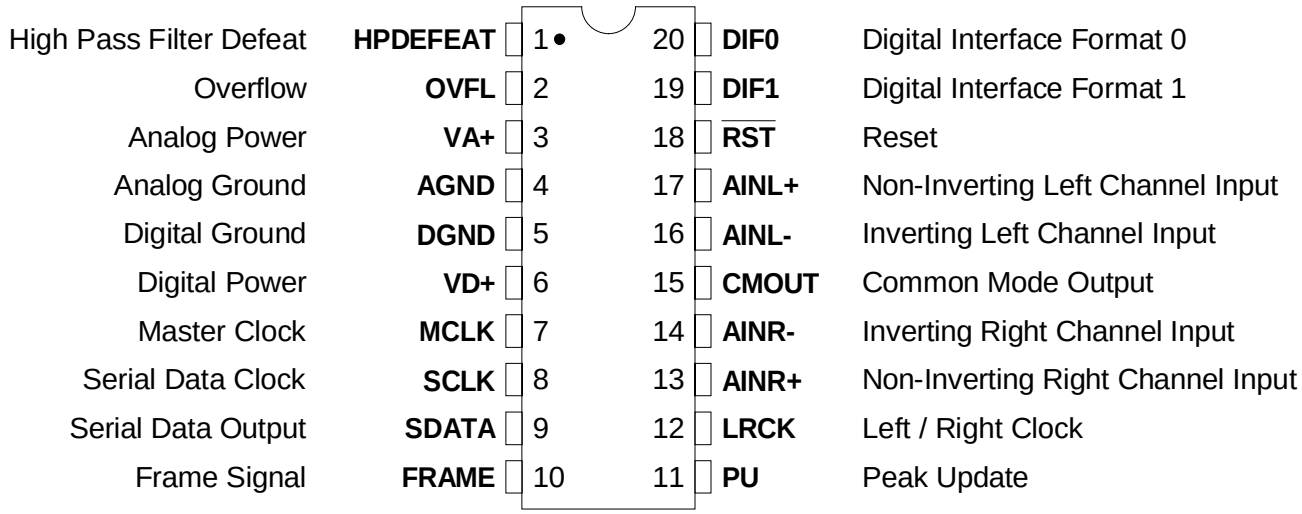


Figure 13. CS5360 Digital Filter Transition Band



5. PIN DESCRIPTIONS



High Pass Filter Defeat - HP DEFEAT

Pin 1, Input

Function

A high logic level on this pin disables the digital high pass filter. A low logic level on this pin enables the high pass filter.

Overflow - $\overline{\text{OVFL}}$

Pin 2, Input

Function

Overflow indicates analog input overrange, for both the Left and Right channels, since the last update request on the PEAK UPDATE (PU) pin. A value of 1 in the register indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK. The registers are updated with a high to low transition on the PEAK UPDATE pin. A 47 kΩ pull-down resistor on this pin will set the CS5360 in Master Mode.

Positive Analog Power - VA+

Pin 3, Input

Function:

Positive analog supply. Nominally +5 volts.

Analog Ground - AGND

Pin 4, Input

Function:

Analog ground reference.

DGND - Digital Ground

Pin 5, Input

Function:

Digital ground reference.

Positive Digital Power - VD+

Pin 6, Input

Function:

Positive digital supply. Nominally +5 volts.

Master Clock - MCLK

Pin 7, Input

Function:

Clock source for the delta-sigma modulator sampling and digital filters. In Master Mode, the frequency of this clock must be 256x the output sample rate, Fs. In Slave Mode, the frequency of this clock must be either 256x, 384x or 512x Fs.

Serial Data Clock - SCLK

Pin 8, Input/Output

Function:

Clocks the individual bits of the serial data out from the SDATA pin. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.In Master Mode, SCLK is an output clock with a frequency of 64x the output sample rate, Fs.In Slave Mode, SCLK is an input.

Serial Data Output - SDATA

Pin 9, Output

Function:

Two's complement MSB-first serial data of 24 bits is output on this pin. Included in the serial data output is the 8-bit Input Signal Level Bits. The data is clocked out via the SCLK clock and the channel is determined by LRCK. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.

Peak Update - PU

Pin 11, Input

Function:

Transfers the Peak Signal Level contents of the Active Registers to the Output Registers on a high to low transition on this pin. This transition will also reset the Active register.

Frame Signal - FRAME

Pin 10, Output

Function:

Frames the Peak Signal Level (PSL) Bits. FRAME goes high coincident with the leading edge of the first PSL bit and falls coincident with the trailing edge of the last PSL bit as shown in Figures 8-10. A 47 kΩ pull-down resistor on this pin will set the Peak Signal Level Monitoring format to "Bar Graph" mode.

Left/Right Clock - LRCK

Pin 12, Input/Output

Function:

LRCK determines which channel, left or right, is to be output on SDATA. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output clock whose frequency is equal to the output sample rate, Fs. In Slave Mode, LRCK is an input clock whose frequency must be equal to Fs.

Differential Right Channel Analog Input - AINR+, AINR-

Pin 13 and Pin 14, Input

Function:

Analog input connections of the right channel differential inputs. Typically 2 Vrms differential (1Vrms for each input pin) for a full-scale analog input signal.

Common Mode Output - CMOUT

Pin 15, Output

Function:

This output, nominally 2.2 V, can be used to bias the analog input circuitry to the common mode voltage of the CS5360. CMOUT is not buffered and the maximum current is 10 µA.

Differential Left Channel Analog Input - AINL+, AINL-

Pin 16 and Pin 17, Input

Function:

Analog input connections of the left channel differential inputs. Typically 2 Vrms differential (1Vrms for each input pin) for a full-scale analog input signal.

Reset - $\overline{\text{RST}}$

Pin 18, Input

Function:

A low logic level on this pin activates Reset.

Digital Interface Format - DIF0, DIF1

Pins 19 and 20, Input

Function:

These two pins select one of 3 digital interface formats or power-down. The format determines the relationship between SCLK, LRCK and SDATA. The formats are detailed in Figures 8-10.

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal at the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

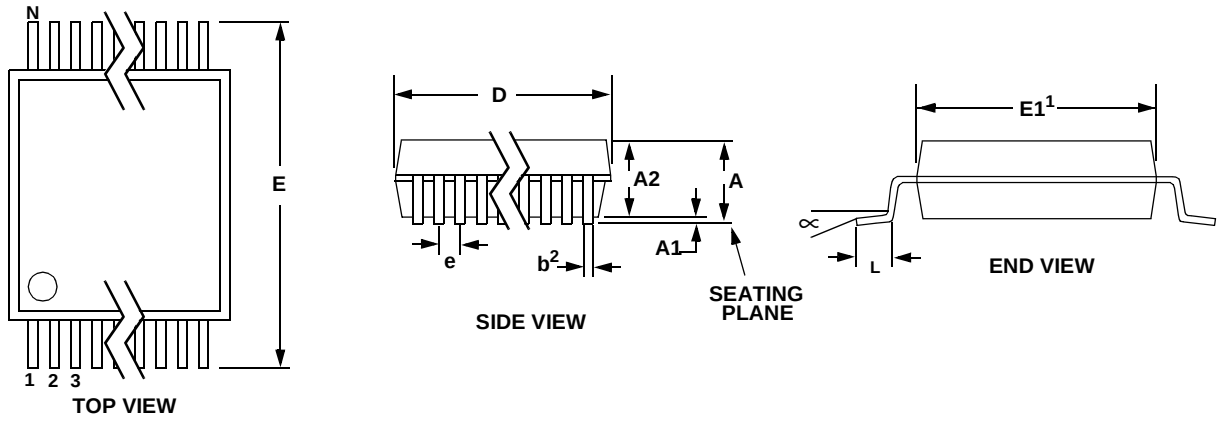
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

7. PACKAGE DIMENSIONS

20 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.272	0.295	6.90	7.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• Notes •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