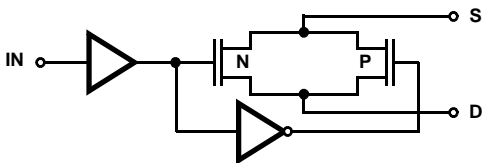


**Dual, SPDT CMOS Analog Switch**

The HI-303 switch is a monolithic device fabricated using CMOS technology and the Intersil dielectric isolation process. This switch features break-before-make switching, low and nearly constant ON resistance over the full analog signal range, and low power dissipation.

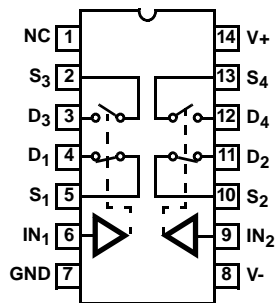
The HI-303 is TTL compatible and has a logic “0” condition with an input less than 0.8V and a logic “1” condition with an input greater than 4V. (See pinouts for switch conditions with a logic “1” input.)

**Functional Diagram**



**Pinout** Switch States Shown For A Logic “1” Input

**HI-303 (PDIP, CERDIP, SOIC)**  
TOP VIEW



LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

**Features**

- Analog Signal Range ( $\pm 15V$  Supplies) . . . . .  $\pm 15V$
- Low Leakage at 25°C . . . . . 40pA
- Low Leakage at 125°C . . . . . 1nA
- Low On Resistance at 25°C . . . . . 35 $\Omega$
- Break-Before-Make Delay . . . . . 60ns
- Charge Injection . . . . . 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power (Typ) . . . . . 1.0mW
- Pb-Free Available (RoHS Compliant)

**Applications**

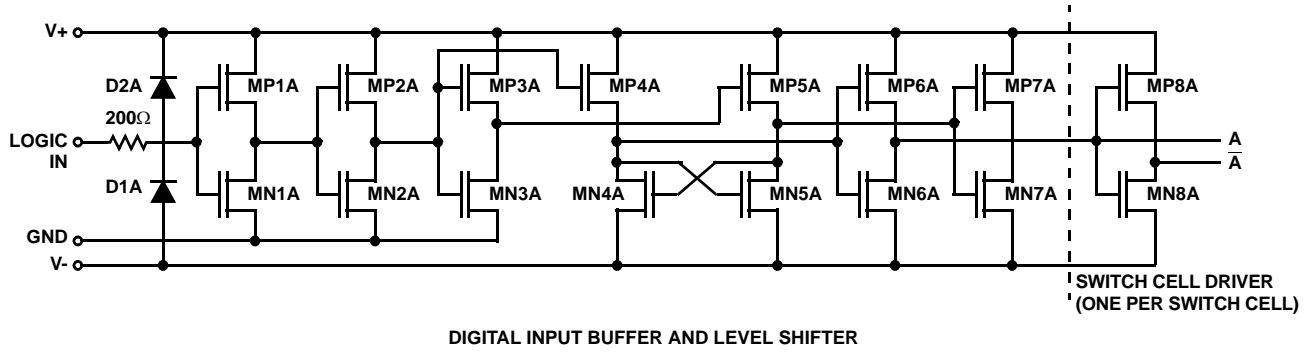
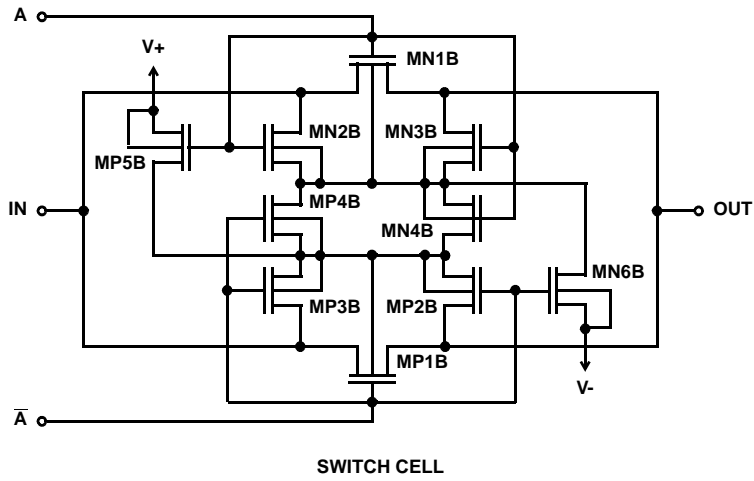
- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0303-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0303-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0303-5	0 to 75	14 Ld PDIP	E14.3
HI3-0303-5Z (See Note)	0 to 75	14 Ld PDIP (Pb-free)	E14.3
HI9P0303-9	-40 to 85	14 Ld SOIC	M14.15
HI9P0303-9Z (See Note)	-40 to 85	14 Ld SOIC (Pb-free)	M14.15

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Schematic Diagrams







Test Circuits and Waveforms (Continued)

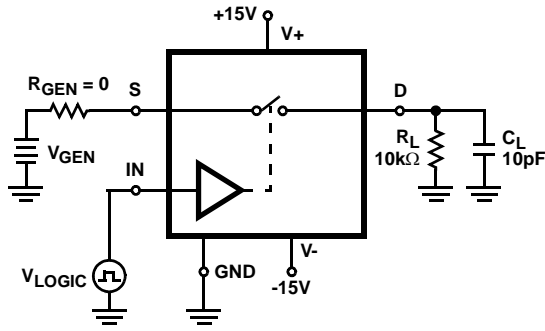


FIGURE 2A. TEST CIRCUIT

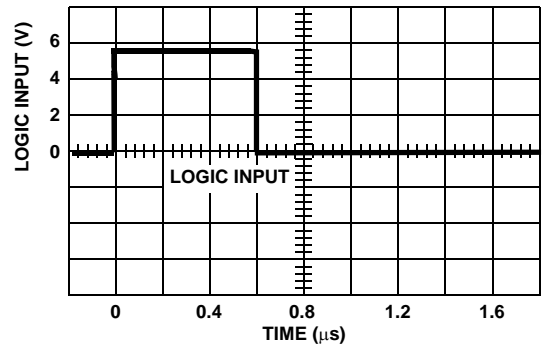


FIGURE 2B. TTL LOGIC INPUT

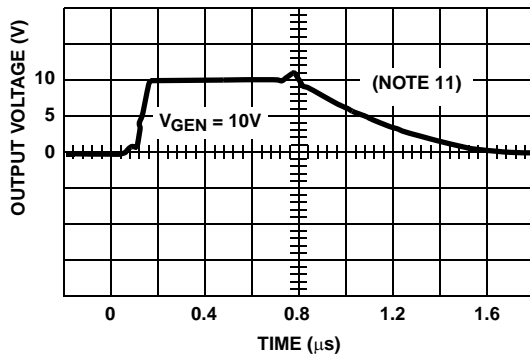


FIGURE 2C.  $V_{ANALOG} = 10V$

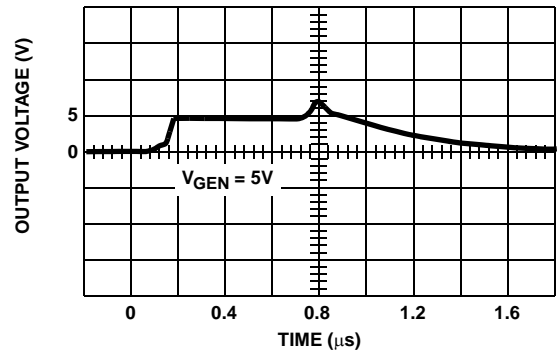


FIGURE 2D.  $V_{ANALOG} = 5V$

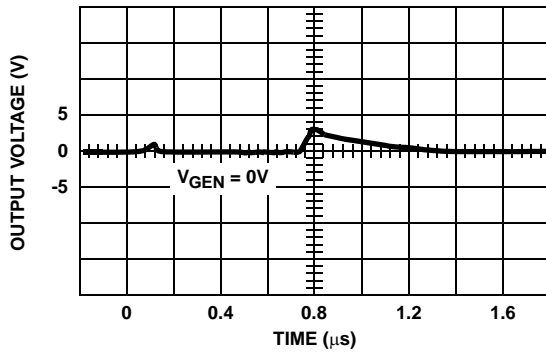


FIGURE 2E.  $V_{ANALOG} = 0V$

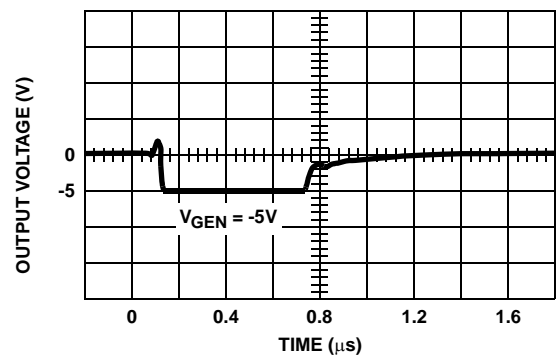


FIGURE 2F.  $V_{ANALOG} = -5V$



Typical Performance Curves (Continued)

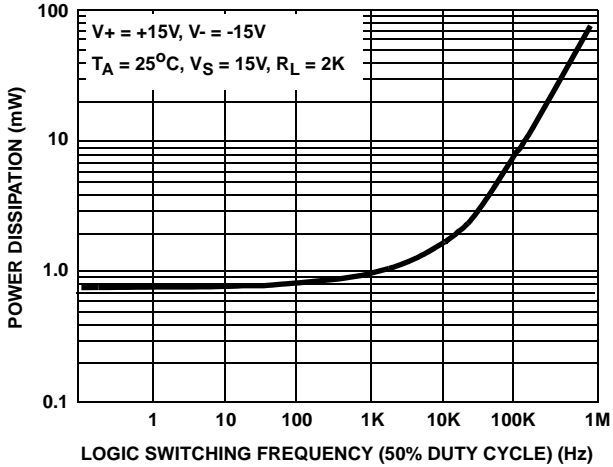


FIGURE 6. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

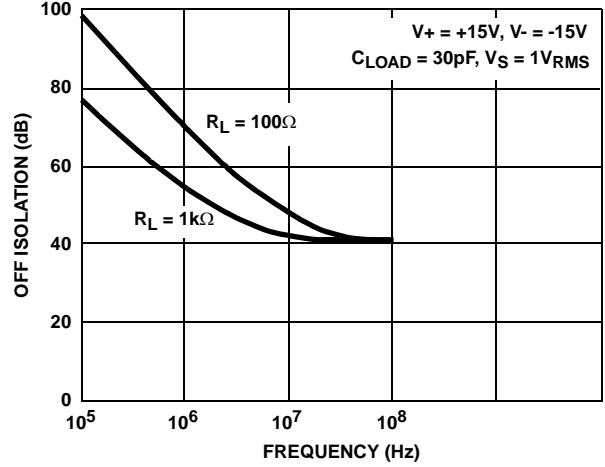


FIGURE 7. OFF ISOLATION vs FREQUENCY

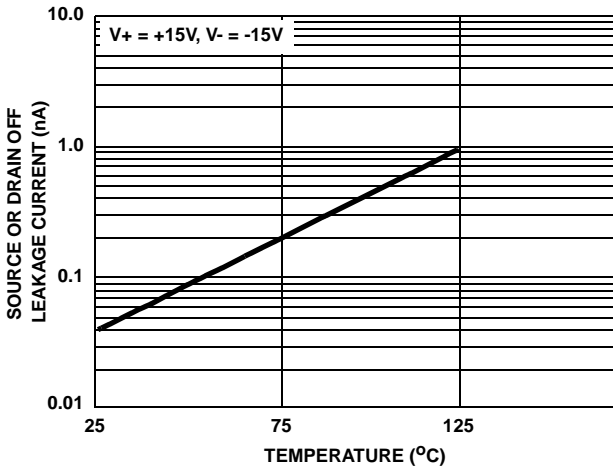


FIGURE 8.  $I_{S(OFF)}$  OR  $I_{D(OFF)}$  vs TEMPERATURE\*

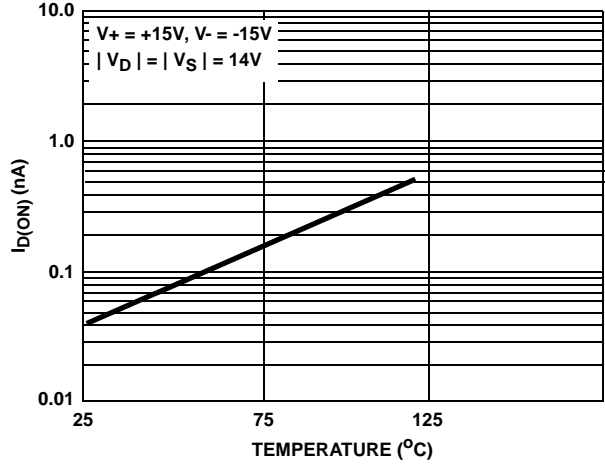


FIGURE 9.  $I_{D(ON)}$  vs TEMPERATURE\*

\* The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

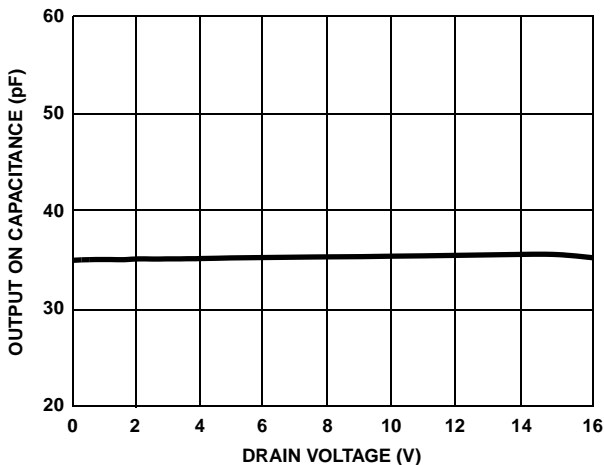


FIGURE 10. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

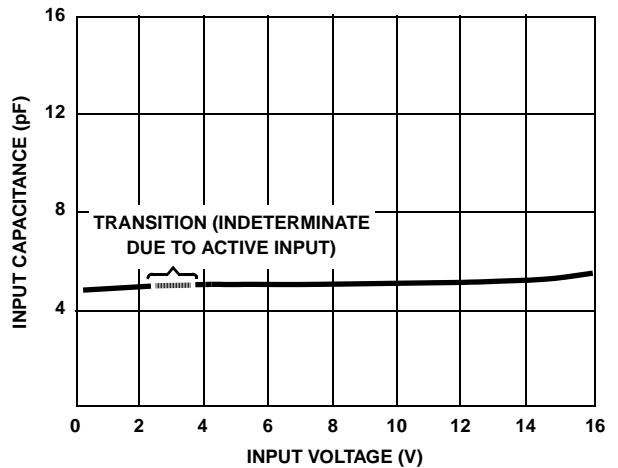


FIGURE 11. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

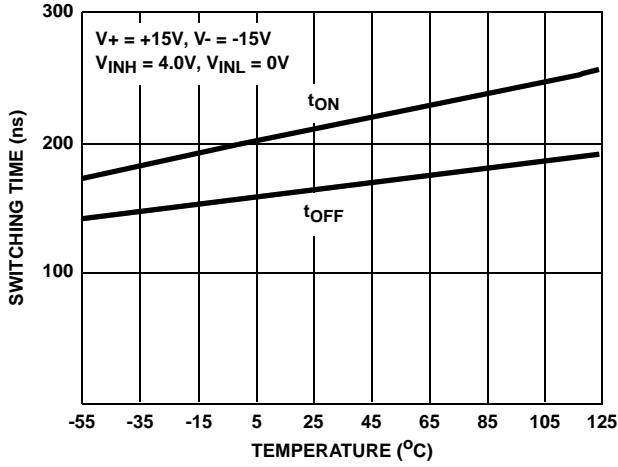


FIGURE 12. SWITCHING TIME vs TEMPERATURE

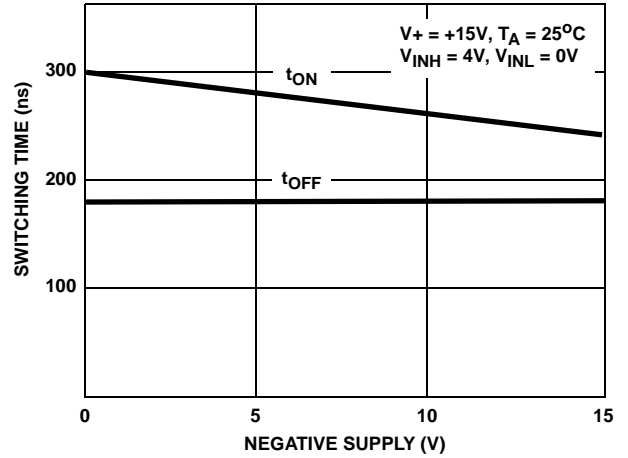


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

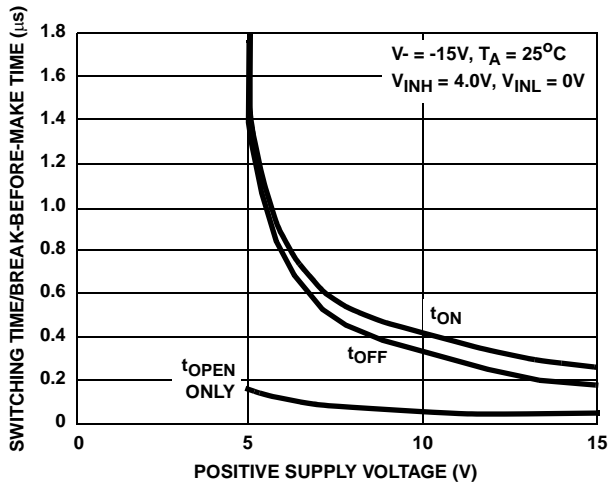


FIGURE 14. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE

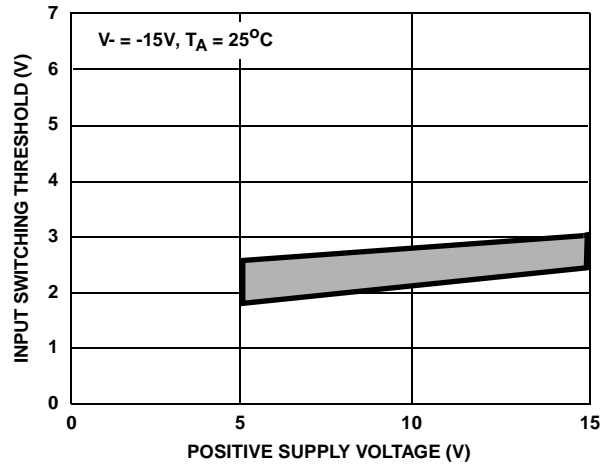
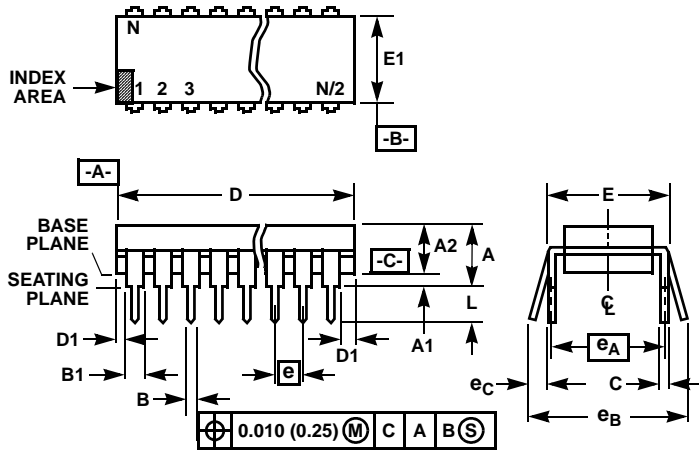


FIGURE 15. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE



Dual-In-Line Plastic Packages (PDIP)



NOTES:

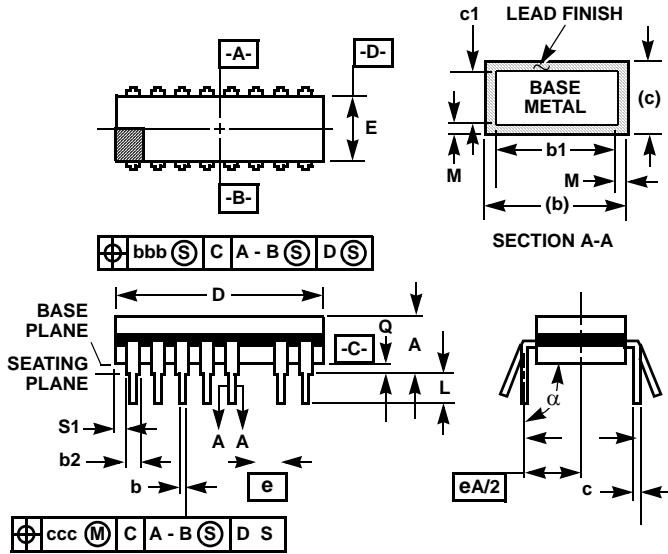
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)  
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

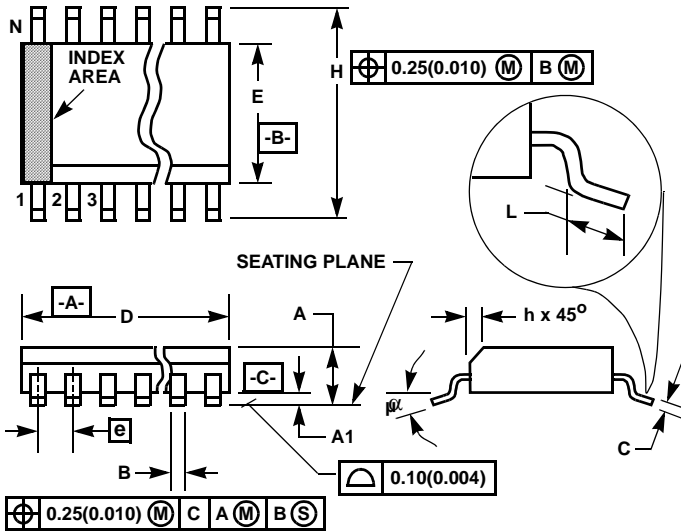
**Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions  $b$  and  $c$  or  $M$  shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions  $b_1$  and  $c_1$  apply to lead base metal only. Dimension  $M$  applies to lead plating and finish thickness.
4. Corner leads (1,  $N$ ,  $N/2$ , and  $N/2+1$ ) may be configured with a partial lead paddle. For this configuration dimension  $b_3$  replaces dimension  $b_2$ .
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension  $Q$  shall be measured from the seating plane to the base plane.
7. Measure dimension  $S_1$  at all four corners.
8.  $N$  is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**Small Outline Plastic Packages (SOIC)**



**M14.15 (JEDEC MS-012-AB ISSUE C)  
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

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