System Motor Driver

BD64547MUV

General Description

This is a system motor driver with integrated 2ch H-bridge driver, 2ch step-down switching regulator (SWREG) with built-in Power MOS, and Reset output.

Features

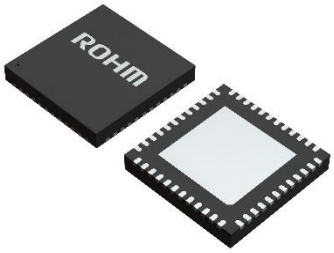
- Low ON-resistance Output H-Bridge Driver (2ch)
- Built-in Regular Current Chopping Function
- Over-current Protection (OCP) in H-Bridge Driver
- 3-line Serial Type Interface
- SWREG (CH1) with Built-in P-ch Power DMOS FET
- High Efficiency SWREG Function
- Soft Start Function in SWREG
- Over-current Protection (OCP) in SWREG
- Output Under Voltage Protection (UVLO) in SWREG
- SWREG Enable Function
- Thermal Shutdown Function (TSD)
- Power ON Reset
- V_{BB} Drop Detection Function
- Ultra-thin Type, High Heat Dissipation Package

Key Specifications

- Input Voltage Range: 9.0 V to 45.0 V
- Motor Rated Output Current: 2.0 A/Phase
- SWREG1 Output Current Range: 0 A to 2.0 A
- SWREG2 Output Current Range: 0 A to 1.4 A
- Operating Temperature Range: -25 °C to +85 °C
- Standby Current: 100 µA (Max)

Package

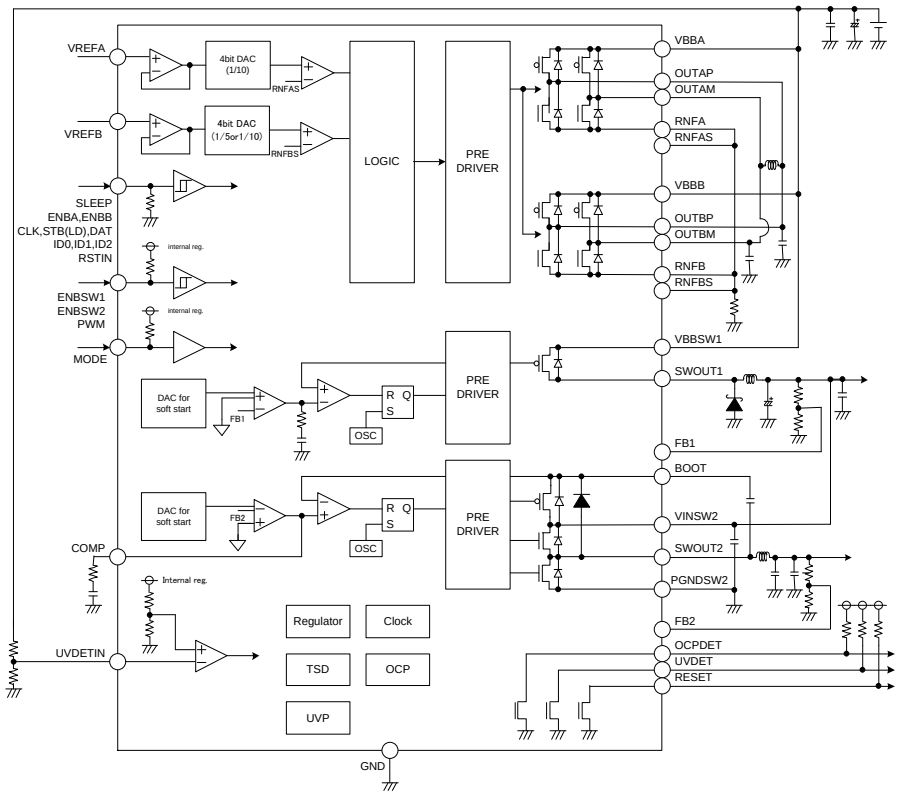
Package	W (Typ) x D (Typ) x H (Max)
VQFN048V7070	7.0 mm x 7.0 mm x 1.0 mm



Applications

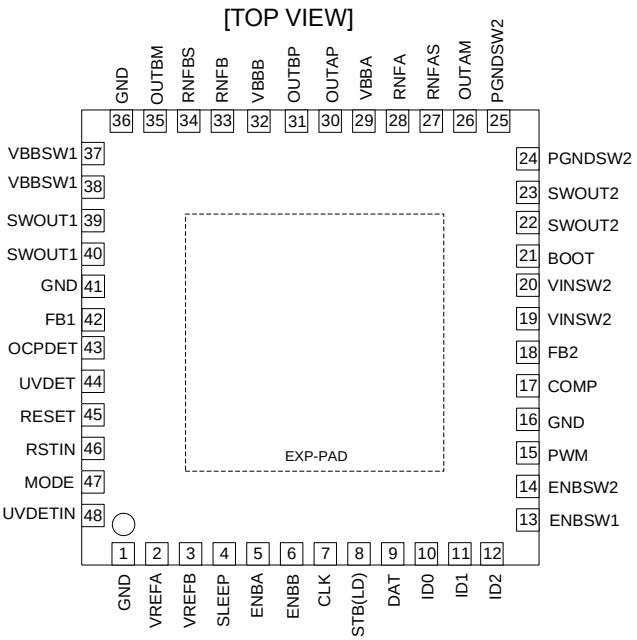
- Inkjet printers
- Photo printers etc.

Typical Application Circuit

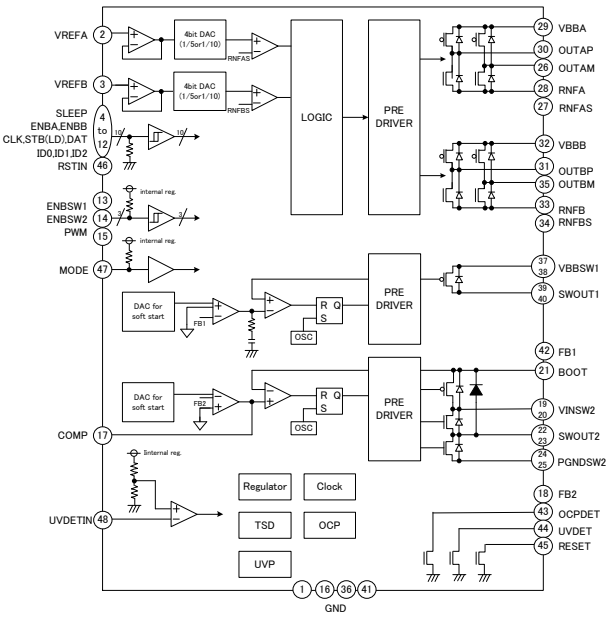


○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



Block Diagram



Pin Description

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	GND	-	Ground	25	PGNDSW2	-	SWREG2 power ground
2	VREFA	I	H-Bridge A output current setting	26	OUTAM	O	H-Bridge A output (-)
3	VREFB	I	H-Bridge B output current setting	27	RNFAS	I	H-Bridge A input pin of current detection
4	SLEEP	I	Sleep mode setting	28	RNFA	O	H-Bridge A current detection
5	ENBA	I	H-Bridge A enable input	29	VBBA	-	H-Bridge A power supply (42 V)
6	ENBB	I	H-Bridge B enable input	30	OUTAP	O	H-Bridge A output (+)
7	CLK	I	Serial CLK input	31	OUTBP	O	H-Bridge B output (+)
8	STB(LD)	I	Serial STB(LD) input	32	VBBB	-	H-Bridge B power supply (42 V)
9	DAT	I	Serial DAT input	33	RNFB	O	H-Bridge B current detection
10	ID0	I	ID 0 setting	34	RNFBS	I	H-Bridge B input pin of current detection
11	ID1	I	ID 1 setting	35	OUTBM	O	H-Bridge B output (-)
12	ID2	I	ID 2 setting	36	GND	-	Ground
13	ENBSW1	I	SWREG1 enable input	37	VBBSW1	-	SWREG1 power supply (42 V)
14	ENBSW2	I	SWREG2 enable input	38	VBBSW1	-	SWREG1 power supply (42 V)
15	PWM	I	SWREG2 PWM compulsion	39	SWOUT1	O	SWREG1 output
16	GND	-	Ground	40	SWOUT1	O	SWREG1 output
17	COMP	I/O	SWREG2 phase compensation	41	GND	-	Ground
18	FB2	I	SWREG2 feedback	42	FB1	I	SWREG1 feedback
19	VINSW2	-	SWREG2 power supply (5 V)	43	OCPDET	O	OCP detection
20	VINSW2	-	SWREG2 power supply (5 V)	44	UVDET	O	V_{BB} drop detection
21	BOOT	I	SWREG2 H-side Nch booster	45	RESET	O	Reset output
22	SWOUT2	O	SWREG2 output	46	RSTIN	I	Reset input
23	SWOUT2	O	SWREG2 output	47	MODE	I	H-Bridge mode setting
24	PGNDSW2	-	SWREG2 power ground	48	UVDETIN	I	UVDET setting
-	EXP-PAD	-	The EXP-PAD is connect to GND.	-	-	-	-

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Limit	Unit
VBB Applied Voltage *(Note 1)(Note 2)*	V_{BB}	-0.4 to +50.0	V
Motor Output Voltage *(Note 3)*	V_{MOUT}	-0.4 to +50.0	V
SWOUT1 Voltage	V_{SWOUT1}	-0.4 to +50.0	V
VINSW2 Applied Voltage *(Note 1)*	V_{INSW2}	-0.4 to +7.0	V
SWOUT2 Voltage	V_{SWOUT2}	-0.4 to +7.0	V
Logic Input Voltage *(Note 4)*	V_{LI}	-0.4 to +5.5	V
Logic Output Voltage *(Note 5)*	V_{LO}	5.5	V
RNF Voltage (DC)	$V_{RNF(DC)}$	0.55	V
RNF Voltage (peak) *(Note 6)*	$V_{RNF(peak)}$	2.5	V
Power Dissipation *(Note 7)*	Pd	4.83	W
Motor Output Current (DC) *(Note 1)*	$I_{OMAXMT(DC)}$	2.0	A/Phase
SWOUT1 Output Current (DC) *(Note 1)*	$I_{OMAXSW1(DC)}$	2.2	A
SWOUT1 Output Current (peak) *(Note 1)(Note 6)*	$I_{OMAXSW1(peak)}$	2.4	A
SWOUT2 Output Current (DC) *(Note 1)*	$I_{OMAXSW2(DC)}$	1.5	A
SWOUT2 Output Current (peak) *(Note 1)(Note 6)*	$I_{OMAXSW2(peak)}$	1.65	A
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Must not exceed Pd and Tj = 150 °C
(Note 2) Supply = VBBA, VBBB, VBBSW1
(Note 3) Motor Output = OUTAP, OUTAM, OUTBP, OUTBM
(Note 4) Logic Input = SLEEP, ENBA, ENBB, CLK, STB(LD), DAT, ID0, ID1, ID2, ENBSW1, ENBSW2, PWM, RSTIN, MODE
(Note 5) Logic Output = OCPDET, UVDET, RESET
(Note 6) peak = 1 µs
(Note 7) When mounted on a 4-layer recommended board (74.2 mm x 74.2 mm x 1.6 mm), reduce by 37.3 mW/°C when Ta ≥ 25 °C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-25	-	+85	°C
VBB Applied Voltage *(Note 8)(Note 9)*	V_{BB}	9.0	-	45.0	V
CLK Max Operating Frequency	f_{CLOCK}	-	40	-	MHz
SWREG1 Output Voltage Setting	V_{OUT1}	3.0	-	13.0	V
SWREG2 Output Voltage Setting	V_{OUT2}	0.8	-	3.6	V
SWREG1 Output Current *(Note 10)*	I_{SW1}	0	-	2.0	A
SWREG2 Output Current *(Note 10)*	I_{SW2}	0	-	1.4	A
VINSW2 Applied Voltage	V_{INSW2}	3.0	-	5.5	V

(Note 8) When V_{BB} is under POR, H-Bridge, SWREG and circuit protection are disabled.
(Note 9) Supply = VBBA, VBBB, VBBSW1
(Note 10) Must not exceed Pd and Tj = 150 °C

Electrical Characteristics (Unless otherwise specified V_{BB} = 42 V, Ta = 25 °C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
[Overall]						
Circuit Current (Standby)*(Note 1)*	I_{BBST}	-	20	100	µA	SLEEP = L, ENBSW1 = H
Circuit Current (Active)*(Note 1)*	I_{BB}	-	8.5	13.0	mA	SLEEP = H, ENBSW1 = L
VINSW2 Current	I_{INSW2}	-	0	10	µA	
POR Threshold Voltage H	V_{PORH}	6	7	8	V	V_{BB} Input timing
POR Hysteresis Voltage	V_{PORHY}	0.5	1.0	1.5	V	
[H-Bridge]						
Output ON-Resistance (H-side)	R_{ONH}	-	0.75	1.05	Ω	I_{OUT} = 1 A
Output ON-Resistance (L-side)	R_{ONL}	-	0.45	0.75	Ω	I_{OUT} = 1 A
Built-in Diode Forward Voltage (H-side)	VF_H	-	1.0	1.3	V	I_{OUT} = 1 A
Built-in Diode Forward Voltage (L-side)	VF_L	-	1.0	1.3	V	I_{OUT} = 1 A
[Current Control]						
VREF Voltage Range	V_{VREF}	0	-	3.7	V	
VREF Input Current	I_{VREF}	-1	0	+1	µA	V_{VREF} = 3.3 V
RNF Input Current	I_{RNF}	5	15	30	µA	
VREF to RNFS Offset Voltage	V_{OFST}*(Note 2)*	-4	0	+4	%	V_{VREF} = 2 V, DAC = 15, MODE = H, M
[Control Logic 1 (DAT, CLK, STB(LD), ENBA, ENBB, SLEEP, RSTIN, ID0, ID1, ID2)]						
H Level Input Voltage 1	V_{IN1H}	2.0	-	-	V	
L Level Input Voltage 1	V_{IN1L}	-	-	0.8	V	
Input Current 1	I_{IN1}	15	33	50	µA	Input Voltage = 3.3 V
[Control Logic 2 (ENBSW1, ENBSW2, PWM)]						
H Level Input Voltage 2	V_{IN2H}	2.0	-	-	V	
L Level Input Voltage 2	V_{IN2L}	-	-	0.8	V	
Input Current 2	I_{IN2}	-18	-9	-3	µA	Input Voltage = 0 V
[Control Logic 3 (MODE)]						
Input Voltage H	V_{IN3H}	4.0	-	-	V	
Input Voltage M	V_{IN3M}	2.0	-	3.0	V	
Input Voltage L	V_{IN3L}	-	-	1.0	V	
Input Current	I_{IN3}	-85	-50	-30	µA	Input Voltage = 0 V
[Switching Regulator 1 Block]						
FB1 Threshold Voltage	V_{FBSW1}	0.99	1.00	1.01	V	
Output ON-Resistance	R_{ONSW1}	-	0.65	0.85	Ω	I_{SWOUT1} = 1 A
FB1 Pin Current	I_{FBSW1}	-0.1	0	+0.1	µA	V_{FB1} = 1 V
FB1 Low Input Voltage	V_{FBUVP1}	0.71	0.75	0.79	V	Common with RESET detection
[Switching Regulator 2 Block]						
FB2 Threshold Voltage	V_{FBSW2}	0.792	0.800	0.808	V	
Output ON-Resistance (H-side)	R_{ONHSW2}	-	0.20	0.26	Ω	I_{SWOUT2} = 1 A
Output ON-Resistance (L-side)	R_{ONLSW2}	-	0.20	0.26	Ω	I_{SWOUT2} = 1 A
FB2 Pin Current	I_{FBSW2}	-0.1	0	+0.1	µA	V_{FB2} = 0.8 V
FB2 Low Input Voltage	V_{FBUVP2}	0.28	0.40	0.52	V	
[RESET, UVDET, OCPDET]						
Low Output Voltage	V_{OD}	-	-	0.2	V	I_{OUT} = 1 mA
RESET Output Delay Time	t_{RST}	40	50	60	ms	
RSTIN Minimum Input Pulse Width	t_{RSTIN}	-	-	13	µs	Refer to P.7 1.4
UVDET Base Voltage	V_{UV}	0.552	0.600	0.648	V	
UVDET Hysteresis Voltage	V_{UVHYS}	-	0.05	-	V	

(Note 1) Total current value of the VBBA, VBBB, VBBSW1 pins.
(Note 2) V_{OFST} = ((V_{VREF} × Current_Ratio / α) – V_{RNFS}) / (V_{VREF} × Current_Ratio / α), α = 5 (MODE = M), 10 (MODE = H)

Recommended Range of External Constants

Characteristics may vary due to factors such as the mounting conditions and the temperature dependence of the external parts. Be certain to evaluate these values with respect to the actual intended application.

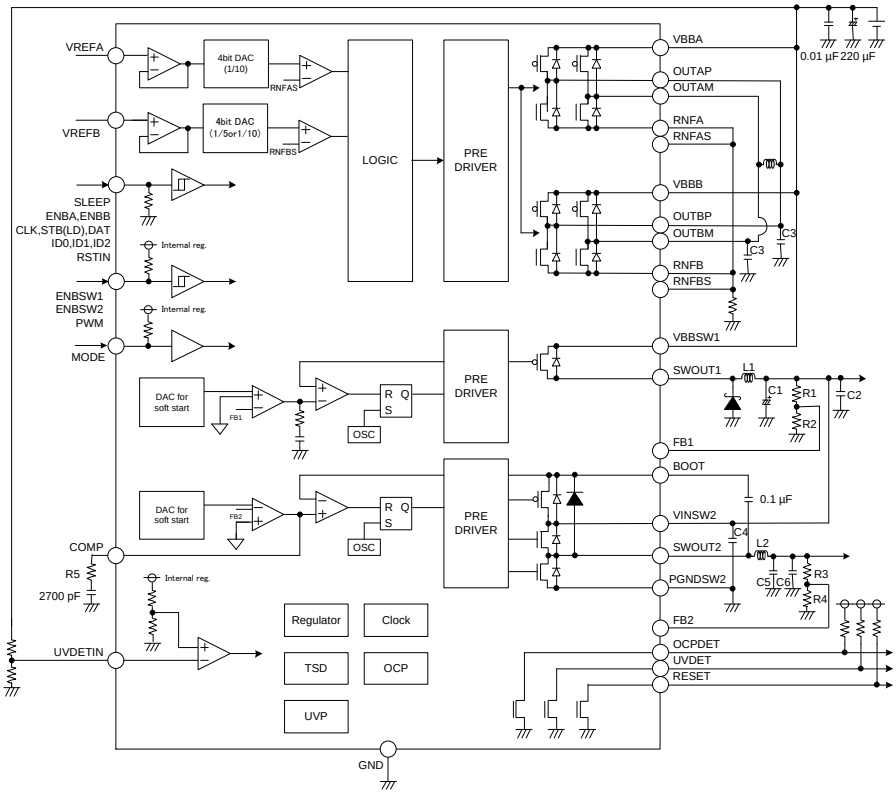


Figure 1. BD64547MUV Recommended Range of External Components Circuit diagram

Parameter	Symbol	Recommended Values			Unit
		Min	Typ	Max	
SWOUT1 (5 V setting)	C_1	220	330	470	µF
SWOUT1 (3.3 V setting)	C_1	220	330	470	µF
SWOUT1	C_2	0	-	22	µF
OUTxx*(Note 1)* (50 V capacity)	C_3	-	-	1000	pF
VINSW2-PGNDSW2	C_4	10	22	40	µF
SWOUT2	C_5 / C_6	-	20 / 20	-	µF
SWOUT1	L_1	33	47	68	µH
SWOUT2	L_2	1.5	1.8	2.2	µH
FB1 (5 V setting)	R_1 / R_2	3.3 / 0.82	33 / 8.2	-	kΩ
FB1 (3.3 V setting)	R_1 / R_2	3.0 / 1.3	30 / 13	-	kΩ
FB2 (3.3 V setting)	R_3 / R_4	-	75 / 24	-	kΩ
FB2 (1.8 V setting)	R_3 / R_4	-	30 / 24	-	kΩ
FB2 (1.5 V setting)	R_3 / R_4	1.3 / 1.5	13 / 15	-	kΩ
FB2 (1.125 V setting)	R_3 / R_4	3.3 / 8.2	33 / 82	-	kΩ
COMP (3.3 V setting)	R_5	-	18	-	kΩ
COMP (1.5 V to 1.8 V setting)	R_5	-	9.1	-	kΩ
COMP (1.125 V setting)	R_5	-	8.2	-	kΩ

(Note 1) xx = AP, AM, BP, BM

Pin Processing • Condition List

1 Pin Connections when H-Bridge is Not in Use

The pin processing shown in the table below is recommended.

	ENBx*(Note 1)*	VREFx*(Note 1)*	RNFx*(Note 1)* RNFxS*(Note 1)*	OUTxP*(Note 1)* OUTxM*(Note 1)*
Ach	OPEN or GND	GND	GND	OPEN
Bch	OPEN or GND	GND	GND	OPEN

(Note 1) x = A, B

The overcurrent protection may fail if VREFx and RNFx / RNFxS are left OPEN.
(However, there is no problem even if Voltage is applied to the VREFx pin only when ENBx is Low and output is open with no serial input.)

2 Pin Connections when SWREG is Not in Use

The pin processing shown in the table below is recommended.

	ENBSWx*(Note 2)*	FBx*(Note 2)*	SWOUTx*(Note 2)*	COMP	BOOT	VINSW2
1ch	OPEN	GND	OPEN	-	-	-
2ch	OPEN	GND	OPEN	OPEN	OPEN	OPEN

(Note 2) x = 1, 2

3 Condition of the MODE pin

MODE	Pin State
H	OPEN
M	100 kΩ Pull Down
L	GND (Don't use)

(use a Pull Down resistor of 100 kΩ with ±5 % accuracy or tolerance.)

4 Active Condition of Logic Input Pins

Logic input pins	Active condition	Non-active condition (OPEN case)
DAT, CLK, STB(LD), ENBA, ENBB, SLEEP, RSTIN, ID0, ID1, ID2	H (2.0 V or more)	L (0.8 V or less)
ENBSW1, ENBSW2, PWM	L (0.8 V or less)	H (2.0 V or more)

5 Condition of the SLEEP pin

Logic input pins	Data accept mode	Power save mode
SLEEP	H (2.0 V or more)	L (0.8 V or less)

When SLEEP = L, ENBSW1 = H and ENBSW2 = H, the condition is stand-by. The IC switches to power save mode. In this case, RESET output (P.7), Thermal shutdown (P.24), over-current (P.24) and output under voltage protection turn OFF.

Explanation of Block Operation

BD64547MUV is composed of four blocks namely; H-Bridge Driver, SWREG1, SWREG2, and Protection Function block as shown in Figure 2.

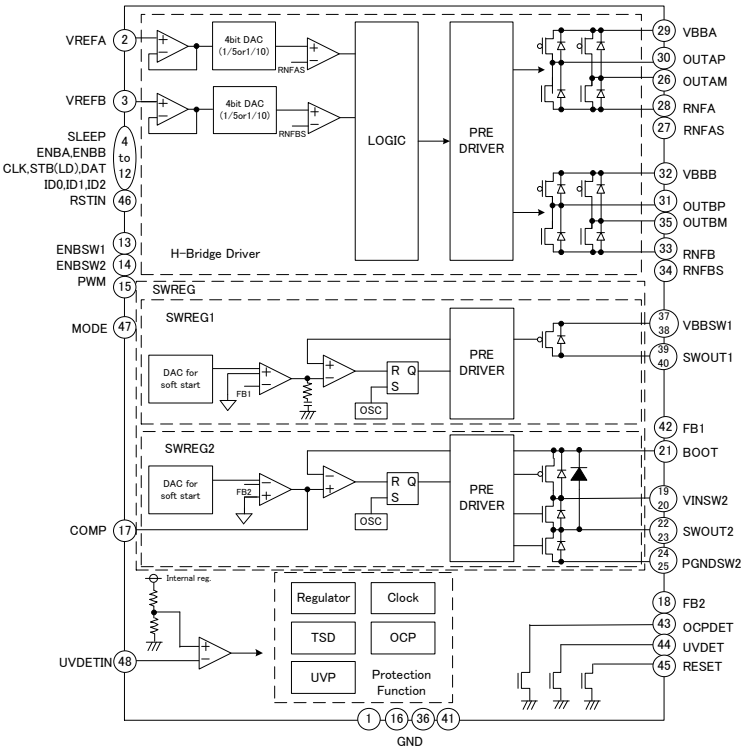


Figure 2. Explanation of Circuit Operation

1 Overall

1.1 Power supply (V_{BB}) input

Input power supply 300 µs or more at 0 V to V_{PORH} (7 V (Typ))

1.2 Control Logic Input

Control logic input for DAT, CLK, STB(LD), ENBA, ENBB, SLEEP, RSTIN, ID0, ID1, ID2, ENBSW1, ENBSW2, PWM is implemented with a Schmitt trigger, with hysteresis.

Design values		
Min	Typ	Max
200 mV	300 mV	400 mV

1.3 Power-On RESET Function

A Power-On RESET circuit is built-in for V_{BB}.

When V_{BB} rises to V_{PORH} level (7.0 V (Typ)) or higher at the time of power ON, SWREG1 activates by a soft start. After soft start, the state of the serial port RESET is cleared. In addition, hysteresis is established at the time of power-down to turn all outputs OFF with V_{PORH}-V_{PORHY} (1.0 V (Typ)) and reset the serial ports.

1.4 Reset Timing, V_{BB} Drop Detection Function

After detecting Power-On RESET release, FB1 ≥ 0.75 V (Typ) and RSTIN = L, RESET output becomes H level after 50 ms (Typ). Meanwhile UVDET output only depends on V_{BB}. It becomes L level with any voltage by external resistance. In addition, inputting H pulse (over 10 µs (Typ), 13 µs (Max)) into the RSTIN pin makes RESET output L level.

RESET output table is shown below (Values at the table are all typical. V_{BB} has hysteresis).

V_{BB}	FB1	RSTIN	RESET Output
Under 7.0 V	Don't Care	Don't Care	Unstable (IC internal circuit stops)
7.0 V or more	Under 0.75 V	H	L
	0.75 V or more	H	L
	Under 0.75 V	L	L
	0.75 V or more	L	H (50 ms after detection)

Explanation of Block Operation – continued

2 H-Bridge

2.1 Power Save Mode

When the SLEEP = L, H-Bridge will cause the circuit to enter standby state, with only SWREG1 and SWREG2 active. Serial ports are reset in power save mode.

SLEEP pin	Mode
L	Power Save Mode
H	Normal (active) Mode

Be sure driver outputs are in the OFF state when switching modes with the SLEEP pin.

2.2 ID Setting

Setting the identification code of the device with the ID0, ID1 and ID2 pins.
ID pin is always monitored.

ID2	ID1	ID0	Identification code (D20, D19, D18)
L	L	L	Driven by Serial interface 2
L	L	H	1 (001)
L	H	L	2 (010)
L	H	H	3 (011)
H	L	L	4 (100)
H	L	H	5 (101)
H	H	L	6 (110)
H	H	H	7 (111)
Don’t care	Don’t care	Don’t care	All IC reply (000)

Identification code 1, 3, 5, 7 is triggered in the falling edge of CLK only, identification code 2, 4, 6 and serial interface 2 is triggered in the rising edge of CLK only.

2.3 MODE Setting

The MODE pin changes the drive mode of H-Bridge as follows.

MODE	Pin state	H-Bridge-A	H-Bridge-B
H	OPEN or 5 V	DC motor ×2 or Stepping motor (VREF voltage splitting ratio α = 10)	
M	100 kΩ pull down	DC motor ×2 or Stepping motor (VREF voltage splitting ratio α = 5)	
L	GND	Don’t use	

2 H-Bridge — continued

2.4 Serial Interface 1

21-bit, 3-linear type serial interface (DAT, CLK, STB(LD)) is provided to set the operation and the value of current limit. DAT logic for each channel is sent to the internal shift register on the edge of CLK signal according to the identification code in the L area of STB(LD) signal.
The data of the shift register appoints a device code in D20, D19, and D18.
Identification codes 1, 3, 5, 7 is triggered on the falling edge of CLK, and in the case of (D20, D19, D18) = (000), identification codes 2, 4, 6 is triggered on the rising edge of CLK. According to address data of D17, D16, D15, D14, word setting write the data on an appropriate address of the internal memory of 3 x 14 bit at the rising edge of the STB(LD) signal.
The input order of serial data is from D20 to D0. After SLEEP changes from L to H, serial data inputs are only valid after 10 µs.

Serial port write timing is described in the figure below, and the respective minimum timing values are specified as follows:

A	:	DAT Setup Time	·····	7.5 ns
B	:	DAT Hold Time	·····	5 ns
C	:	CLK High Pulse Width	·····	25 ns
D	:	CLK Low Pulse Width	·····	25 ns

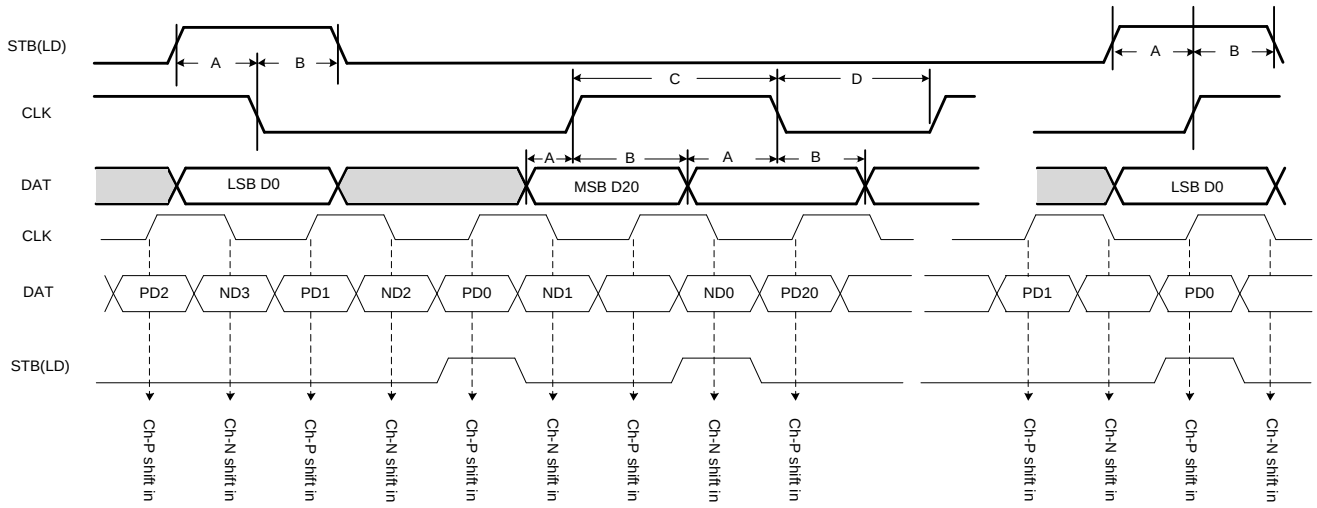


Figure 3. Serial Port Write Timing of Serial Interface 1

2 H-Bridge — continued

2.5 Serial Data Allotment (Serial Interface 1)

Address Data

	WORD A	Initial DAT
D0	Watch Dog Timer LSB	0
D1	Watch Dog Timer MSB	0
D2	-	-
D3	-	-
D4	-	-
D5	-	-
D6	-	-
D7	-	-
D8	-	-
D9	-	-
D10	-	-
D11	-	-
D12	-	-
D13	-	-
D14	Word Select 0 = 1	1
D15	Word Select 1 = 1	1
D16	Word Select 2 = 1	1
D17	Word Select 3 = 1	1
D18	-	-
D19	-	-
D20	-	-

D17 Word Select 3	D16 Word Select 2	D15 Word Select 1	D14 Word Select 0	Word Select
1	1	1	1	WORD A
0	0	0	0	WORD B
0	0	0	1	WORD C
0	0	1	0	WORD D
0	0	1	1	Rohm Reserved
0	1	0	0	WORD E
0	1	0	1	WORD F
0	1	1	0	WORD G
0	1	1	1	WORD H

Rohm Reserved denotes a special mode-setting port for inspection at shipment.
If the Word Select 3, 2, 1, and 0 are set to “0,0,1,1” by mistake, it may cause malfunctions. Therefore, be careful NOT to implement this setting.

2.5 Serial Data Allotment (Serial Interface 1) — continued

	WORD B (H-Bridge-A Specific)	Initial DAT	WORD C (H-Bridge-B Specific)	Initial DAT	WORD D H-Bridge-A-B General	Initial DAT
D0	Blank Time LSB	0	Blank Time LSB	0	Internal PWM Mode for H-Bridge-B	0
D1	Blank Time MSB	0	Blank Time MSB	0	External PWM Mode for H-Bridge-B	0
D2	Off Time LSB	0	Off Time LSB	0	Phase for H-Bridge-B	0
D3	Off Time Bit1	0	Off Time Bit1	0	DAC LSB for H-Bridge-B	0
D4	Off Time Bit2	0	Off Time Bit2	0	DAC Bit1 for H-Bridge-B	0
D5	Off Time Bit3	0	Off Time Bit3	0	DAC Bit2 for H-Bridge-B	0
D6	Off Time MSB	1	Off Time MSB	1	DAC MSB for H-Bridge-B	0
D7	Fast Decay Time LSB	0	Fast Decay Time LSB	0	Internal PWM Mode for H-Bridge-A	0
D8	Fast Decay Time Bit1	0	Fast Decay Time Bit1	0	External PWM Mode for H-Bridge-A	0
D9	Fast Decay Time Bit2	0	Fast Decay Time Bit2	0	Phase for H-Bridge-A	0
D10	Fast Decay Time MSB	0	Fast Decay Time MSB	0	DAC LSB for H-Bridge-A	0
D11	Sync. Rect. Control	0	Sync. Rect. Control	0	DAC Bit1 for H-Bridge-A	0
D12	Sync. Rect. Enable	0	Sync. Rect. Enable	0	DAC Bit2 for H-Bridge-A	0
D13	Don’t care	-	Don’t care	-	DAC MSB for H-Bridge-A	0
D14	Word Select 0 = 0	0	Word Select 0 = 1	1	Word Select 0 = 0	0
D15	Word Select 1 = 0	0	Word Select 1 = 0	0	Word Select 1 = 1	1
D16	Word Select 2 = 0	0	Word Select 2 = 0	0	Word Select 2 = 0	0
D17	Word Select 3 = 0	0	Word Select 3 = 0	0	Word Select 3 = 0	0
D18	ID Bit0	-	ID Bit0	-	ID Bit0	-
D19	ID Bit1	-	ID Bit1	-	ID Bit1	-
D20	ID Bit2	-	ID Bit2	-	ID Bit2	-

2.5 Serial Data Allotment (Serial Interface 1) — continued

	WORD E (H-Bridge-A Specific)	Initial DAT	WORD F (H-Bridge-B Specific)	Initial DAT
D0	EN A PWM Cycle Time LSB	0	EN B PWM Cycle Time LSB	0
D1	EN A PWM Cycle Time Bit1	0	EN B PWM Cycle Time Bit1	0
D2	EN A PWM Cycle Time Bit2	0	EN B PWM Cycle Time Bit2	0
D3	EN A PWM Cycle Time Bit3	0	EN B PWM Cycle Time Bit3	0
D4	EN A PWM Cycle Time Bit4	0	EN B PWM Cycle Time Bit4	0
D5	EN A PWM Cycle Time Bit5	0	EN B PWM Cycle Time Bit5	0
D6	EN A PWM Cycle Time Bit6	0	EN B PWM Cycle Time Bit6	0
D7	EN A PWM Cycle Time Bit7	0	EN B PWM Cycle Time Bit7	0
D8	EN A PWM Cycle Time Bit8	0	EN B PWM Cycle Time Bit8	0
D9	EN A PWM Cycle Time Bit9	0	EN B PWM Cycle Time Bit9	0
D10	EN A PWM Cycle Time Bit10	0	EN B PWM Cycle Time Bit10	0
D11	EN A PWM Cycle Time Bit11	0	EN B PWM Cycle Time Bit11	0
D12	EN A PWM Cycle Time MSB	0	EN B PWM Cycle Time MSB	0
D13	Don’t care	-	Don’t care	-
D14	Word Select 0 = 0	0	Word Select 0 = 1	1
D15	Word Select 1 = 0	0	Word Select 1 = 0	0
D16	Word Select 2 = 1	1	Word Select 2 = 1	1
D17	Word Select 3 = 0	0	Word Select 3 = 0	0
D18	ID Bit0	-	ID Bit0	-
D19	ID Bit1	-	ID Bit1	-
D20	ID Bit2	-	ID Bit2	-

	WORD G (H-Bridge-A Specific)	Initial DAT	WORD H (H-Bridge-B Specific)	Initial DAT
D0	EN A PWM On Time LSB	0	EN B PWM On Time LSB	0
D1	EN A PWM On Time Bit1	0	EN B PWM On Time Bit1	0
D2	EN A PWM On Time Bit2	0	EN B PWM On Time Bit2	0
D3	EN A PWM On Time Bit3	0	EN B PWM On Time Bit3	0
D4	EN A PWM On Time Bit4	0	EN B PWM On Time Bit4	0
D5	EN A PWM On Time Bit5	0	EN B PWM On Time Bit5	0
D6	EN A PWM On Time Bit6	0	EN B PWM On Time Bit6	0
D7	EN A PWM On Time Bit7	0	EN B PWM On Time Bit7	0
D8	EN A PWM On Time Bit8	0	EN B PWM On Time Bit8	0
D9	EN A PWM On Time Bit9	0	EN B PWM On Time Bit9	0
D10	EN A PWM On Time Bit10	0	EN B PWM On Time Bit10	0
D11	EN A PWM On Time Bit11	0	EN B PWM On Time Bit11	0
D12	EN A PWM On Time MSB	0	EN B PWM On Time MSB	0
D13	Phase for H-Bridge-A	0	Phase for H-Bridge-B	0
D14	Word Select 0 = 0	0	Word Select 0 = 1	1
D15	Word Select 1 = 1	1	Word Select 1 = 1	1
D16	Word Select 2 = 1	1	Word Select 2 = 1	1
D17	Word Select 3 = 0	0	Word Select 3 = 0	0
D18	ID Bit0	-	ID Bit0	-
D19	ID Bit1	-	ID Bit1	-
D20	ID Bit2	-	ID Bit2	-

2 H-Bridge — continued

2.6 Serial Interface 2

16-bit, 3-line type serial interface (CLK, DAT, STB(LD)) is provided to set the operation and the value of current limit. DAT logic for each channel is sent to the internal shift register on the rising edge of the CLK pin in the L area of the STB(LD) pin.
According to address data of D15 and D14, shift register data write the data on an appropriate address of the internal memory of 3 x 14 bit at the rising edge of the STB(LD) pin.
The input order of serial data is from D15 to D0. After SLEEP changes from L to H, serial data inputs are only valid after 10 µs.

Serial port write timing is described in the figure below, and the respective minimum timing values are specified as follows:

A	:	DAT Setup Time	·····	15 ns
B	:	DAT Hold Time	·····	10 ns
C	:	Setup STB(LD) to CLK Rising Edge	·····	50 ns
D	:	CLK High Pulse Width	·····	50 ns
E	:	CLK Low Pulse Width	·····	50 ns
F	:	Setup CLK Rising Edge to STB(LD)	·····	50 ns
G	:	STB(LD) Pulse Width	·····	50 ns

Address data

D15	D14	Word Select
0	0	WORD0
0	1	WORD1
1	0	WORD2
1	1	Rohm Reserved

Rohm Reserved is a special mode setting port for factory inspection, etc.
Please be careful not to set it as it may cause malfunction if it is set incorrectly.

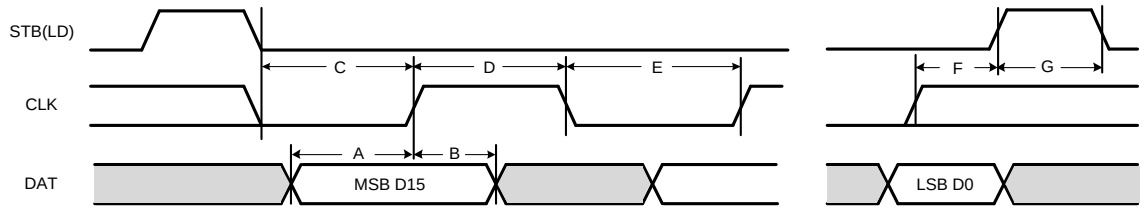


Figure 4. Serial Port Write Timing of Serial Interface 2

2 H-Bridge — continued

2.7 Serial Data Allotment (Serial Interface 2)

	WORD0 (H-Bridge-A Specific)	Initial DAT	WORD1 (H-Bridge-B Specific)	Initial DAT	WORD2 H-Bridge-A-B General	Initial DAT
D0	Blank Time LSB	0	Blank Time LSB	0	Internal PWM Mode for H-Bridge-B	0
D1	Blank Time MSB	0	Blank Time MSB	0	External PWM Mode for H-Bridge-B	0
D2	Off Time LSB	0	Off Time LSB	0	Phase for H-Bridge-B	0
D3	Off Time Bit1	0	Off Time Bit1	0	DAC LSB for H-Bridge-B	0
D4	Off Time Bit2	0	Off Time Bit2	0	DAC Bit1 for H-Bridge-B	0
D5	Off Time Bit3	0	Off Time Bit3	0	DAC Bit2 for H-Bridge-B	0
D6	Off Time MSB	1	Off Time MSB	1	DAC MSB for H-Bridge-B	0
D7	Fast Decay Time LSB	0	Fast Decay Time LSB	0	Internal PWM Mode for H-Bridge-A	0
D8	Fast Decay Time Bit1	0	Fast Decay Time Bit1	0	External PWM Mode for H-Bridge-A	0
D9	Fast Decay Time Bit2	0	Fast Decay Time Bit2	0	Phase for H-Bridge-A	0
D10	Fast Decay Time MSB	0	Fast Decay Time MSB	0	DAC LSB for H-Bridge-A	0
D11	Sync. Rect. Control	0	Sync. Rect. Control	0	DAC Bit1 for H-Bridge-A	0
D12	Sync. Rect. Enable	0	Sync. Rect. Enable	0	DAC Bit2 for H-Bridge-A	0
D13	Don’t care	-	Don’t care	-	DAC MSB for H-Bridge-A	0
D14	Word Select 0 = 0	-	Word Select 0 = 1	-	Word Select 0 = 0	-
D15	Word Select 1 = 0	-	Word Select 1 = 0	-	Word Select 1 = 1	-

2 H-Bridge — continued

2.8 Explanation of Serial Port · H-Bridge Operation

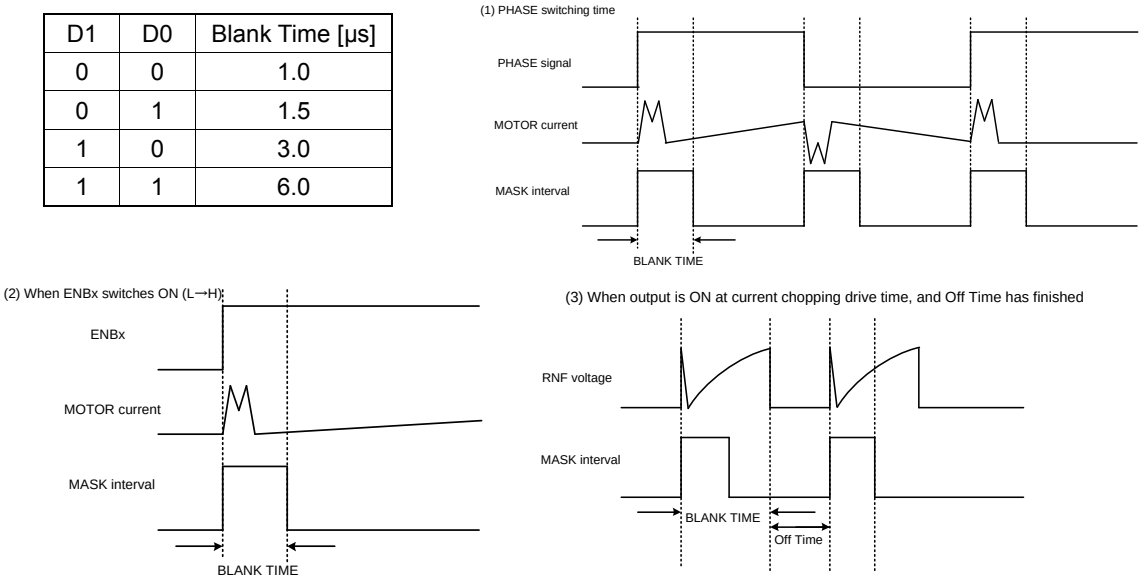
H-Bridge is in ACTIVE mode when the logic of the SLEEP pin is H level and in DECAY mode when it is L level. All serial input time settings are determined by the internal clock (40 MHz (Typ) ±15 % (Ta = 25 °C)) and have the same degree of variation and temperature dependence as the clock.

2.8.1 Blank Time D0 to D1: WORD0 / WORD1

The current-limit comparator monitors the RNFxS*(Note 1)* pin voltage and sets the current limit. However, the RNFxS pin voltage is not detected during the switch to BLANK TIME to avoid misdetection due to noise spikes that occurs at the time of the switching.

(1) PHASE switching time
(2) When ENBx*(Note 1)* switches ON (L → H)
(3) When output is ON at current chopping drive time, and Off Time has finished

D1	D0	Blank Time [µs]
0	0	1.0
0	1	1.5
1	0	3.0
1	1	6.0



(Note 1) x = A, B

Figure 5. Blank Time

2.8.2 Off Time D2 to D6: WORD0 / WORD1

Off Time is set by the following equation:

$$t_{OFF} = (1 + N) \times 8 \times 0.25 - 0.25 \ \text{[µs]}$$

t_{OFF} : is the Off Time.
N : is set by the serial bit: 0 to 31.

For example, if N = 0, the Off Time setting is as follows:

$$t_{OFF} = (1 + 0) \times 8 \times 0.25 - 0.25 = 1.75 \ \text{[µs]}$$

2.8.3 Fast Decay Time D7 to D10: WORD0 / WORD1

Fast Decay Time is set by the following equation:

$$t_{FD} = (1 + N) \times 8 \times 0.25 - 0.25 \ \text{[µs]}$$

t_{FD} : is the Fast Decay Time.
N : is set by the serial bit: 0 to 15.

For example, if N = 0, the Fast Decay Time setting is as follows:

$$t_{FD} = (1 + 0) \times 8 \times 0.25 - 0.25 = 1.75 \ \text{[µs]}$$

2.8 Explanation of Serial Port · H-Bridge Operation — continued

2.8.4 Sync. Rect. Control D11: WORD0 / WORD1

At Fast Decay Mode Synchronous rectification,
make settings related to reverse energization of the motor current.

D11	Sync. Rect. Cont.	Function
0	ACTIVE	Detects motor current at 0 A, switches synchronous rectification OFF and prevents reverse energization.
1	PASSIVE	Permits reverse energization; switches synchronous rectification OFF when current reaches the I_{TRIP}.

$$I_{TRIP} = VREF \times DACvalue(Current\_Ratio)/(\alpha \times Rsense) \text{ [A]}$$

I_{TRIP} : is the motor current limit, established by the formula above.
$VREF$: Is the output current value setting voltage.
α : is the VREF voltage division ratio.
(MODE = H: α = 10, MODE = M: α = 5)
$Rsense$: is the Current detection resistance value.
$DACvalue(Current\_Ratio)$: is refer to table below.

2.8.5 DAC value (Current_Ratio) D3 to D6 / D10 to D13: WORD2

MSB D6 / D13	Bit2 D5 / D12	Bit1 D4 / D11	LSB D3 / D10	Current_Ratio [%]
1	1	1	1	100.00
1	1	1	0	98.08
1	1	0	1	95.69
1	1	0	0	92.39
1	0	1	1	88.19
1	0	1	0	83.15
1	0	0	1	77.30
1	0	0	0	70.71
0	1	1	1	63.44
0	1	1	0	55.56
0	1	0	1	47.14
0	1	0	0	38.27
0	0	1	1	29.03
0	0	1	0	19.51
0	0	0	1	9.80
0	0	0	0	Disable

2.8.6 Sync. Rect. Enable D12: WORD0 / WORD1

In current decay mode, D12 value enables or disables synchronous rectification.

D12	Sync. Rect. En.	Function
0	Disabled	No synchronous rectification
1	Enabled	Synchronous rectification implemented

2.8 Explanation of Serial Port · H-Bridge Operation — continued

2.8.7 Internal PWM Mode D0 / D7: WORD2

In current decay mode, this data sets the motor current regeneration method.
Mixed Decay setting: During Off Time, the Fast Decay Time is set for Fast regeneration mode.
For the rest of the time, it is set to Slow regeneration mode. In this scheme, if Fast Decay Time is longer than Off Time, Fast regeneration becomes the only operative mode.
When Sync. Rect. Control = Active and 0 A is detected in Fast regeneration mode, the regeneration mode will switch to Slow, once all outputs are OFF and the Fast Decay Time period has finished.

D0 / D7	Mode
0	Mixed
1	Slow

2.8.8 External PWM Mode D1 / D8: WORD2

Sets the motor current regeneration mode when ENBx*(Note 1)* = L.
Motor current regeneration is triggered by the falling edge of the ENBx pin logic.
Therefore, this mode is not synchronized with the clock.

D1 / D8	Mode
0	Fast
1	Slow

(Note 1) x = A, B

2.8.9 Phase D2 / D9: WORD2

Sets the motor drive rotational direction.

D2 / D9	Direction	OUTxP*(Note 2)*	OUTxM*(Note 2)*
0	Reverse	L	H
1	Forward	H	L

There is a Phase bit in WORD D, WORD G, WORD H, and last updated WORD is reflected.
For example, when Phase D2: WORD D ”0”, Phase D13: WORD G ”0”, Phase D13: WORD G ”1”, Phase setting is forward detection. And when Phase D2: WORD D ”0”, Phase D13: WORD H ”0”, Phase D2: WORD D ”1”, Phase setting is forward detection.
(Note 2) x = A, B

2.8.10 PWM Cycle Time D0 to D12: WORD E / WORD F

PWM Cycle Time setting. PWM Cycle Time is accomplished using the equation:

$$t_{PWM} = N \times 25n \text{ [s]}$$

t_{PWM} : is the PWM Cycle Time.
N : is set by the serial bit: 0 to 8191.

For example, if N = 4000,

$$t_{PWM} = 4000 \times 25n = 100 \text{ [µs]}$$

When N = 0 is set, external enable becomes active. On the other hand, internal PWM becomes active when N > 0 is set.

2.8 Explanation of Serial Port · H-Bridge Operation — continued

2.8.11 PWM ON Time D0 to D12: WORD G / WORD H

PWM ON Time setting. PWM ON Time is accomplished using the equation:

$$t_{ON} = N \times 25n \text{ [s]}$$

t_{ON} : is the PWM ON Time.
N : is set by the serial bit: 0 to 8191.

For example, when N = 1000,

$$t_{ON} = 1000 \times 25n = 25 \text{ [µs]}$$

(The frequency of the internal clock becomes 30 MHz (Min) or more)

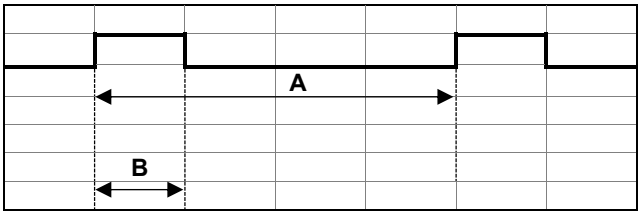


Figure 6. Relationship Diagram of PWM Cycle Time and PWM ON Time

A: PWM Cycle Time
B: PWM ON Time
Section B is ON section. The end of section A is OFF section from the end of section B (Slow Decay or Fast Decay).

Example)
PWM ON Time: when N = 1000, 1000 x 25 ns = 25 µs
PWM Cycle Time: when N = 4000, 4000 x 25 ns = 100 µs
Therefore, PWM period is 100 µs (section A), ON Time is 25 µs (section B), OFF Time is 75 µs (section B to section A).

2.8.12 Watch Dog Timer D0 / D1: WORD A

A counter improves when setting value to a start register. When setting the time, this IC turn OFF motor output. The A side and the B side can be set individually.

(Usage example)
1. Set the A side time at 180 s
2. Initiate the A side start register and start timer count.
3. A side motor drives.
4. When the motor stops, it clears the start register and the timer count is reset.

In case step 4 did not function in the sequence mentioned above (with a field anomaly relaxation method overrun and a bug) and the start register is not cleared for more than 180 s, turn OFF motor driver output. In addition, if you set it to 180 s again within 180 s after setting it to 180 s, the count is restarted from there.

D1	D0	Time (s)		
		Min	Typ	Max
0	0	Infinity (default)	Infinity (default)	Infinity (default)
0	1	50	60	70
1	0	150	180	210
1	1	250	300	350

2 H-Bridge — continued

2.9 Current Decay Mode

For the PWM constant current drive of this IC, the current decay modes (FAST DECAY / SLOW DECAY) can be set freely. The state of output transistor and the route of motor's regenerative current during current decay for each DECAY mode are as follows.

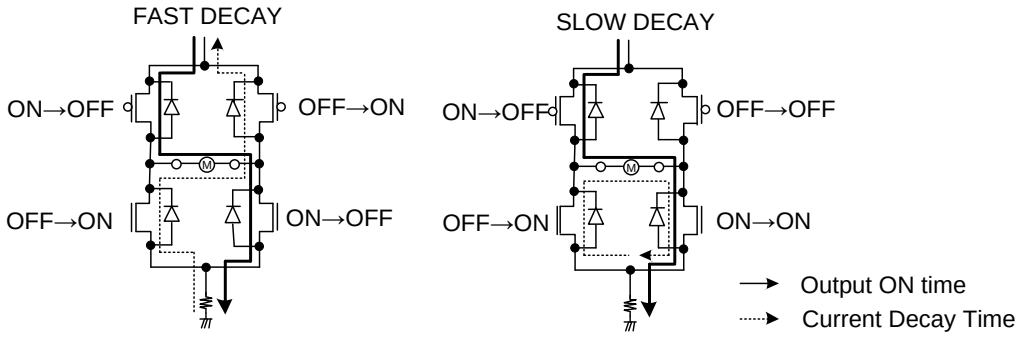


Figure 7. Route of Regenerated Current during Current Decay

The merits of each DECAY mode are as follows:

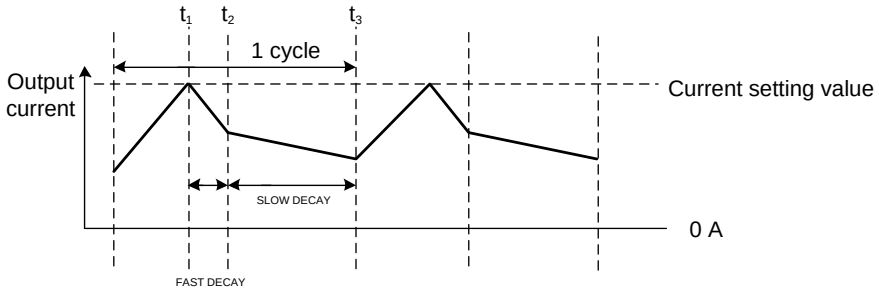
2.9.1 SLOW DECAY

When the current decay, the voltage between motor coils is small and the regenerative current decreases slowly. Current ripple also decreases, which improves motor torque. At the same time, the output current increases due to the deterioration of current control characteristic in the small current region; it is also easily affected by motor's BEMF at the time of high pulse rate drive. Therefore, change of current limit value cannot be followed, current waveform distorts and motor vibration increases. It is most suitable to FULL STEP and low pulse rate drive.

2.9.2 FAST DECAY

Because of sudden decrease of regenerative current, distortion of current waveform related to high pulse rate drive can be reduced. However, because the output current's ripple gets larger, the average current decreases, so (1) motor torque decreases (increasing the current limit value can cope with the problem, but it is necessary to take the rated output current into consideration), (2) motor's loss gets larger causing heat radiation to also increase. If there are no problems of (1) and (2), it is most suitable to the modes that are of high pulse rate drive.

There is the Mixed Decay mode that can improve the problem related to Slow Decay mode and Fast Decay mode. Due to switching between Fast Decay and Slow Decay, the current control characteristic can be improved without making the current ripple larger during current decay.
This IC can change the time ratio of Slow Decay and Fast Decay during Mixed Decay, so the optimal control state for every motor can be achieved. During Mixed Decay, the first half X % (between t_1 and t_2) of the discharge interval in the chopping cycle is Fast Decay time, and the remaining interval is Slow Decay time (between t_2 and t_3).



Motor output current (DC): to 2.0 A/Phase
Motor output current (peak): to 6.0 A/Phase

Figure 8. Mixed Decay Diagram

Explanation of Block Operation – continued

3 SWREG

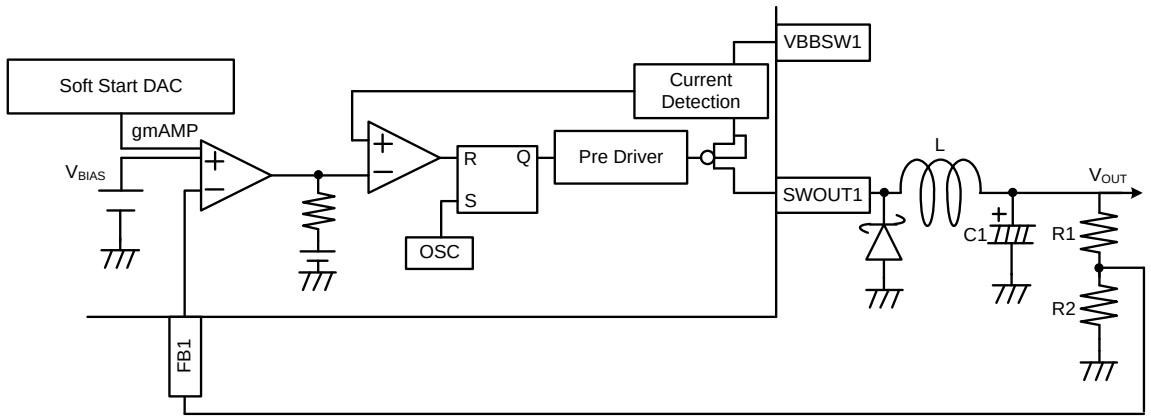


Figure 9. SWREG1 Block Diagram (SWREG2: Synchronous rectification and VBBSW1 → VINSW2)

3.1 Basic Operation

This IC incorporates 2ch of switching regulator circuit that repeats ON/OFF, synchronized with an internal clock (SWCLK), 1ch SWREG operates by 250 kHz (Typ) ±15 % and 2ch SWREG operates by 1 MHz (Typ) ±20 %.

Startup output voltage SWOUT1 begins switching and the V_{OUT1} slowly ramps up with a soft start at V_{BB} power-on ($V_{BB} > V_{PORH}$) and ENBSW1 = L. And startup output voltage SWOUT2 begins switching and the V_{OUT2} slowly ramps up with a soft start at V_{BB} power-on ($V_{BB} > V_{PORH}$) and ENBSW2 = L . When ENBSW1 = H and ENBSW2 = H, the IC doesn't work.
Input power supply 300 µs or more at 0 V to V_{PORH} (7 V (Typ))

Output voltage is determined with external resistance by using the following equation:

$$V_{OUT} = V_{BIAS} \times \{(R_1 + R_2)/R_2\} \text{ [V]}$$

V_{OUT} is the output voltage.
V_{BIAS} is the FB1 voltage.
R_1, R_2 is the external resistance.

Note that the external LC filter constant should be set to optimize output ripple voltage (V_{RIP}). This is accomplished using the equation below:

$$V_{RIP} = I_{RIP} \times \{(ESR + 1)/f_{SW}/C_{OUT}/8\} \text{ [V]}$$

V_{RIP} : is the output ripple voltage.
I_{RIP} : is the output ripple current.
ESR : is the equivalent series resistance.
f_{SW} : is the switching frequency.
C_{OUT} : is the output capacitance.

$$I_{RIP} = V_{OUT}/L \times V_{BBSW} - V_{OUT}/V_{BBSW} \times 1/f_{SW} \text{ [A]}$$

L : is the inductance.
V_{BBSW} : is the applied voltage.

3.2 Skip Mode Operation

In certain run modes, such as when output load is low, gmAMP output (COMP) voltage exceeds the current detection level at the SWCLK rising edge, output will not switch ON.

3.3 MAX DUTY

In certain run modes, such as when output load is high, if the COMP voltage level does not reach the current detection level, output MAX DUTY (90 %) will force the output OFF.

3 SWREG — continued

3.4 Operation Timing

Operation timing under light, normal and heavy loads are respectively described in the charts below.

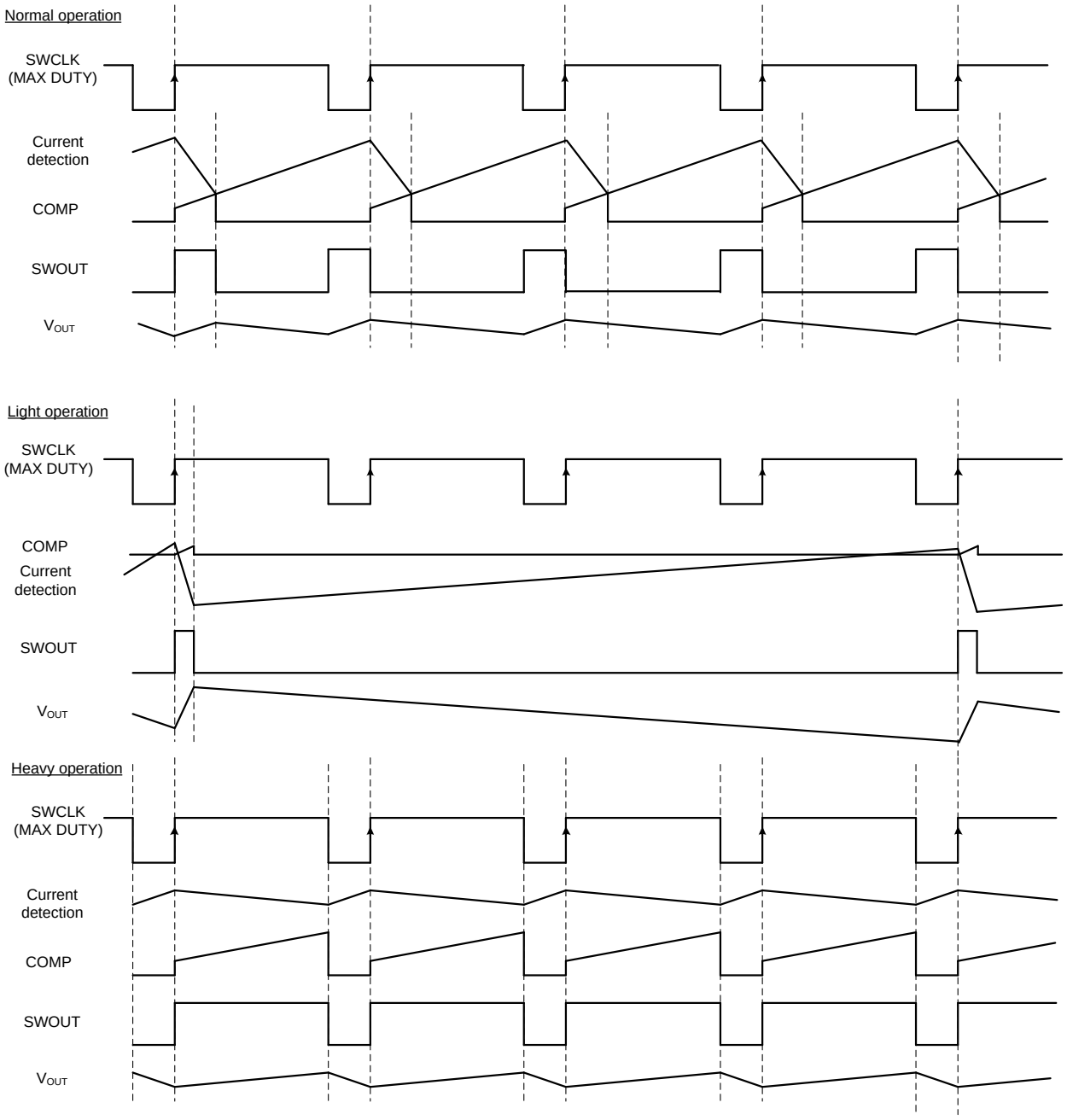


Figure 10. Operation Timing of Light Loads, Normal Loads and Heavy Loads

3 SWREG — continued

3.5 SWREG1 Soft Start (at power-on, with ENBSW1 = L)

At the time of power-on, V_{OUT1} ramps up slowly with a soft start.
The rising edge of SWREG1 is synchronized with the timing when ENBSW1 = L and POR release.

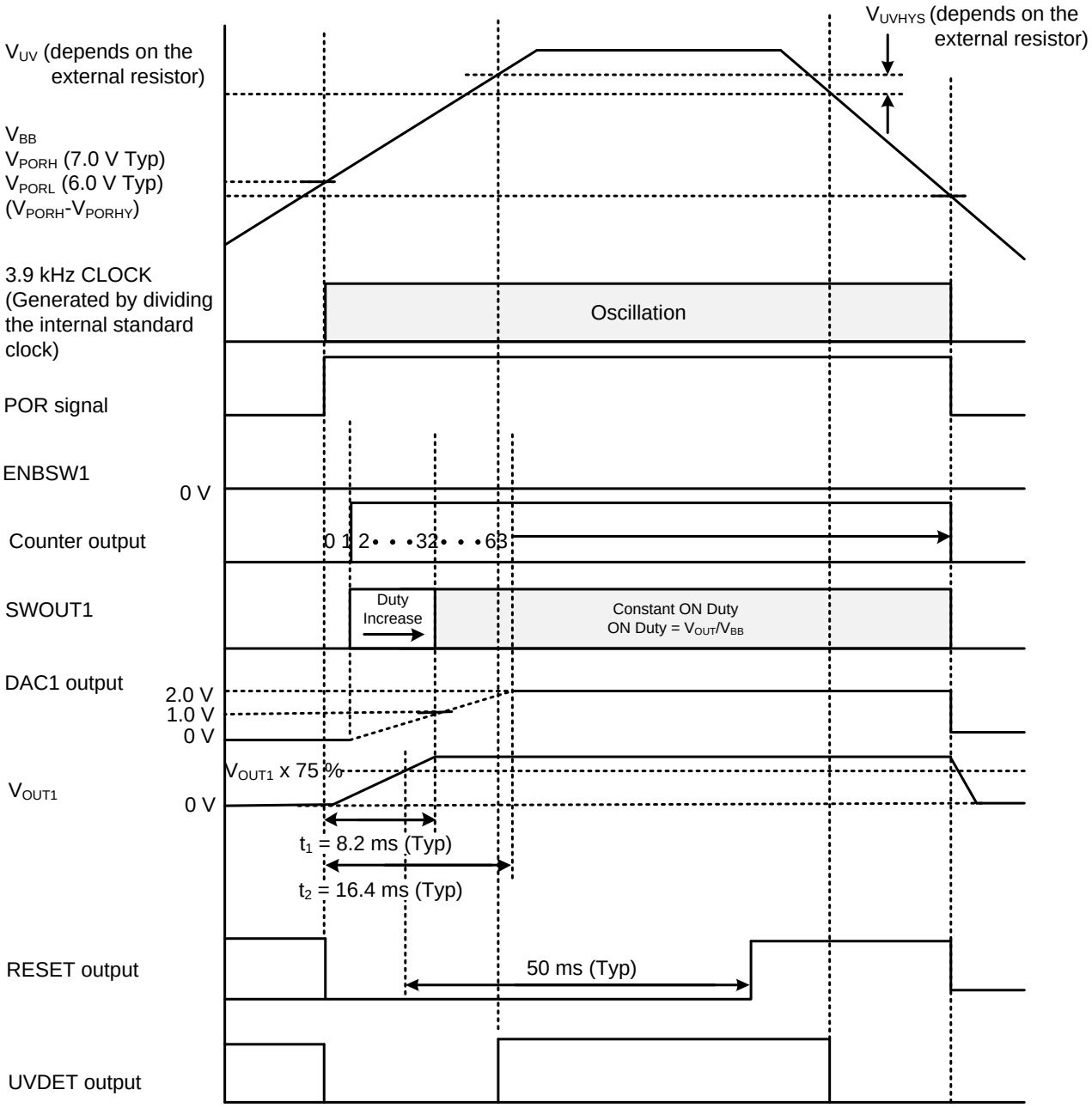


Figure 11. SWREG1 Soft Start Operation Timing Diagram

This soft start method is realized by linearly changing the negative side voltage of the gmAMP by using DAC.
Soft start time t1 is constant, regardless of V_{BB}.

Parameter	Specification			Unit
	Min	Typ	Max	
Soft start time (t_1)	6.97	8.20	9.43	ms
Count finish time (t_2)	13.94	16.40	18.86	ms

3 SWREG — continued

3.6 SWREG2 Operation

SWREG2 is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in Pulse Width Modulation (PWM) mode for heavier load, while it utilizes SLLM™ (Simple Light Load Mode) control for lighter load to improve efficiency.

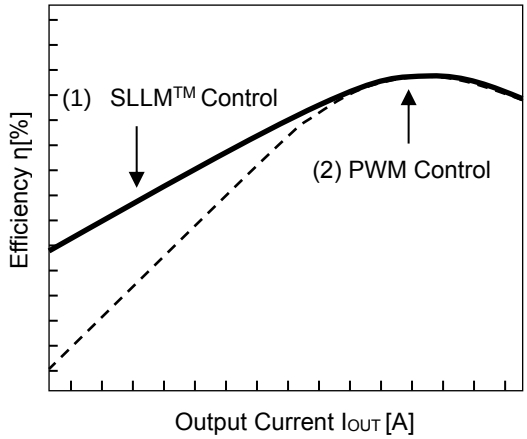


Figure 12. Efficiency characteristics (SLLM™ Control and PWM Control)

3.6.1 Basic Function

SWREG2 works forcibly with fixed frequency PWM mode when the PWM pin is H. SLLM™ control is enabled, SLLM™ control and fixed frequency PWM mode becomes active automatically when the PWM pin is L.

When the logic of the PWM pin is switched during SWREG2 operation, the output voltage may decrease. Therefore, fix the logic of the PWM pin to H (2.0 V or more) or L (0.8 V or less) before starting up the SWREG2(Note 1), and do not change during operation.

(Note 1) Before start up means the ENBSW2 = H state or before UVLO release of SWREG2.

3.6.2 Enable Control

The SWREG2 shutdown can be controlled by the voltage applied to the ENBSW2 Pin. When ENBSW2 = L, the internal circuit is activated and the SWREG2 starts up. To shutdown control with the ENBSW2 Pin, the shutdown interval (H level interval of ENSW2) must be set to 100 μs or longer.

3.7 Reference efficiency (It does not do the all quantity measurement.)

Channel	Efficiency (Typ)	Unit	Conditions	Notes
SWREG1	87	%	V_{BBSW1} = 12 V, V_{OUT1} = 5.0 V, I_{OUT1} = 50 mA	DS126C2 B953AS-680M(TOKO) RB050L-60TE25(ROHM)
	85	%	V_{BBSW1} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 50 mA	DS126C2 B953AS-680M(TOKO) RB050L-60TE25(ROHM)
SWREG2	88	%	V_{INSW2} = 3.3 V, V_{OUT2} = 1.1 V, I_{OUT2} = 50 mA	NRS6045T1R8NMGK (TAIYO YUDEN)
	86	%	V_{INSW2} = 3.3 V, V_{OUT2} = 1.5 V, I_{OUT2} = 50 mA	NRS5040T1R5NMGJ (TAIYO YUDEN)

Explanation of Block Operation – continued

4 Protection Functions

4.1 Protection Circuits Function

Overall	Overheating protection
H-Bridge drive circuit	Over-current protection
SWREG circuit	Over-current protection, output low voltage protection

4.1.1 Overheating protection

Turns OFF all output functions in response to junction temperature rise.
Output is restored when the system powers on again.

Thermal shutdown temperature	Hysteresis	Restart
175 °C (Typ)	None	-

4.1.2 Over-current protection (H-Bridge)

Detects current flowing to H-Bridge output, turns OFF all H-Bridge outputs at the end of Mask time. Output is restored at the SLEEP pin = H → L → H.

Set current	Mask time	Restart
3.5 A (Typ)	3 µs (Typ)	SLEEP

4.1.3 Over-current protection (H-Bridge) detect function

The OCPDET output detects that the over-current protection of the H-Bridge has worked and becomes L level at the timing of turnning OFF all H-Bridge outputs.

4.1.4 Over-current protection (SWREG1)

Detects current flowing to SWREG1 output. After Mask time, SWREG1 is turned OFF between 256 µs to 512 µs (Typ) at the timing of detection.
When protection operation is complete, normal operation resumes.

Channel	Set current	Mask time	Restart
SWREG1	5.0 A (Typ)	0.15 µs (Typ)	-

4.1.5 Over-current protection (SWREG2)

It becomes activated by confining current flowing through the upper part MOSFET of SWREG2 to every 1 cycle of the switching frequency.

Channel	Set current
SWREG2	5.0 A (Typ)

4.1.6 Output low voltage protection (SWREG1)

Monitors the FB1 pin voltage of the SWREG1 circuit.
If the FB1 pin voltage is less than 0.75 V (Typ), only SWREG1 is turned OFF after mask time. Output is restored at the ENBSW1 pin = L → H → L.

Set voltage	Mask time	Restart
< 0.75 V (Typ)	10 µs (Typ)	ENBSW1

Note that output under-voltage protection does not work until the soft start count is complete (16.4 ms (Typ)).

4.1.7 Output low voltage protection (SWREG2)

Monitors the FB2 pin voltage of the SWREG2 circuit.
It activates when the FB2 pin voltage is less than 0.4 V (Typ).
SWREG2 is turned OFF when the state continues for 1 ms (Typ).

Set voltage	Mask time	Output low voltage protection operation	Restart
< 0.4 V (Typ)	1 ms (Typ)	ON	ENBSW2 reboot
> 0.4 V (Typ)	-	OFF	-

4 Protection Functions — continued

4.2 Over-current protection circuit operation current

Function Block		Design value		
		Min	Typ	Max
H-Bridge	Operation current	2.5 A	3.5 A	4.5 A
	Mask time	2.4 µs	3 µs	3.6 µs
SWREG1	Operation current	2.3 A	5.0 A	6.9 A
SWREG2	Operation current	2.05 A	5.00 A	6.90 A

The over-current protection circuit's only aim is to prevent the destruction of the IC from irregular situations such as motor output shorts, and is not meant to be used as protection or surety for the set. Therefore, sets should not be designed to take into account this circuit's functions. After the OCP activates, if the return by power reactivation or the reset by the SLEEP pin in an abnormal state, the OCP operation may be repeated in the order of latch → recovery → latch, which may cause heat generation or deterioration of the IC. Please note that. If the L value of the wiring is large, such as the wiring is long when the motor outputs are shorted VCC or GND or other outputs, the output pin voltage jumps after an overcurrent flows, and if it exceeds the absolute maximum rating, it may be destroyed. Also, when current which is over the output current rating and under the OCP detection current flows, the IC may heat up to over Tjmax = 150 °C and can deteriorate, so current which exceeds the output rating should not be applied. This value is design level and is not the guaranteed value that is measured by total inspection.

4.3 Timing of output low voltage protection (SWREG1)

When the switching regulator output current is large enough to reach a detection threshold 5.0 A (Typ), the output is shut OFF for a period of 256 µs to 512 µs (Typ). Then, output is restored to the normal ON state by the timing of the next ON switching cycle. Repeated large current outflows will cause this operation to implement continuously, which in turn will gradually lower the output voltage. Consequently, when it detects that the voltage at the FB pin (output voltage feedback pin) has fallen below 0.75 V (Typ), it latches the output OFF after a mask time of 10 µs (Typ). At this time, all outputs except the switching regulator are turned off at the same time.

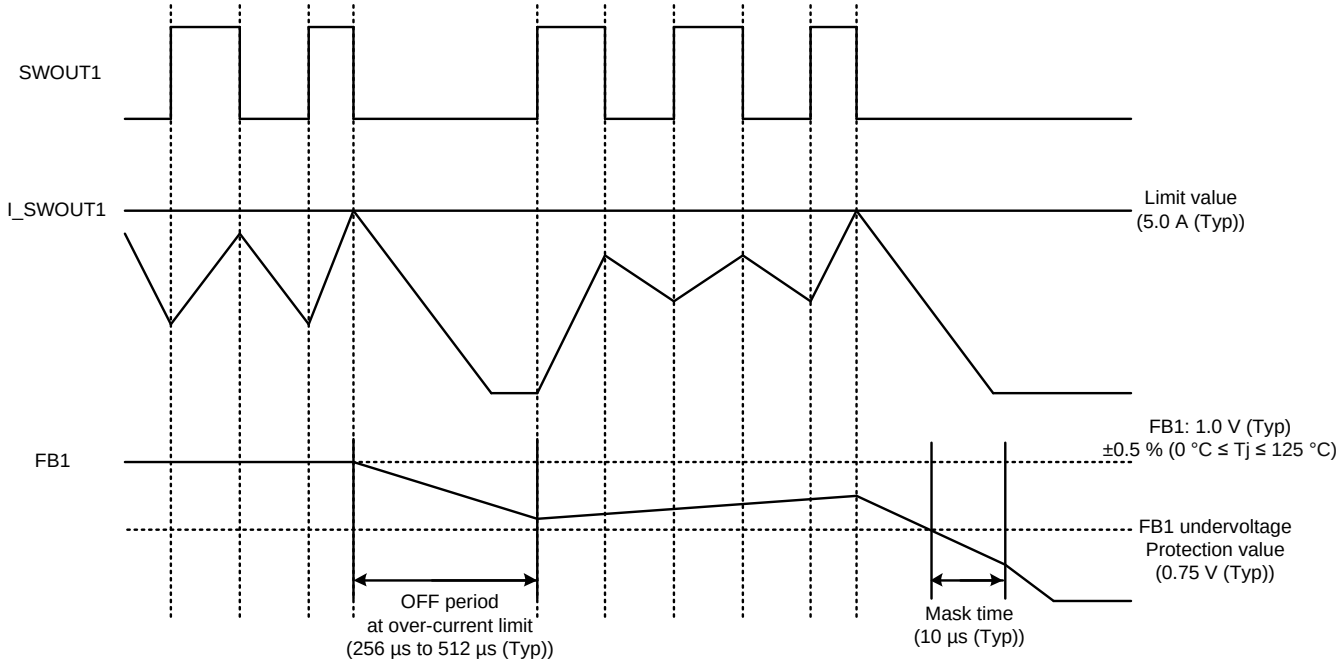


Figure 13. Timing of SWREG1 Protection Operation Diagram

FB1 under-voltage protection will not operate during the soft start period (t_2), If abnormal FB1 voltage is produced during a soft start, the IC will not shut OFF until the soft start is complete.

4 Protection Functions — continued

4.4 Soft Start (at power-on, with ENBSW2 = L)

At the time of power-on, V_{OUT2} ramps up slowly with a soft start.
The rising edge of SWREG2 is synchronized with the timing when ENBSW2 = L and POR release of V_{BB}.

4.5 Operation Timing of malfunction protection circuit at output low voltage protection (SWREG2)

This IC has a built-in malfunction protection circuit at low voltage (Under Voltage Lock Out: UVLO circuit) to prevent false operation such as the output during power supply under voltage. When the applied voltage to the VINSW2 pin goes under 2.45 V (Typ), the output is set to OFF state. This switching voltage has a 0.2 V (Typ) hysteresis to prevent false operation by noise etc. This value is design level and is not the guaranteed value that is measured by total inspection.

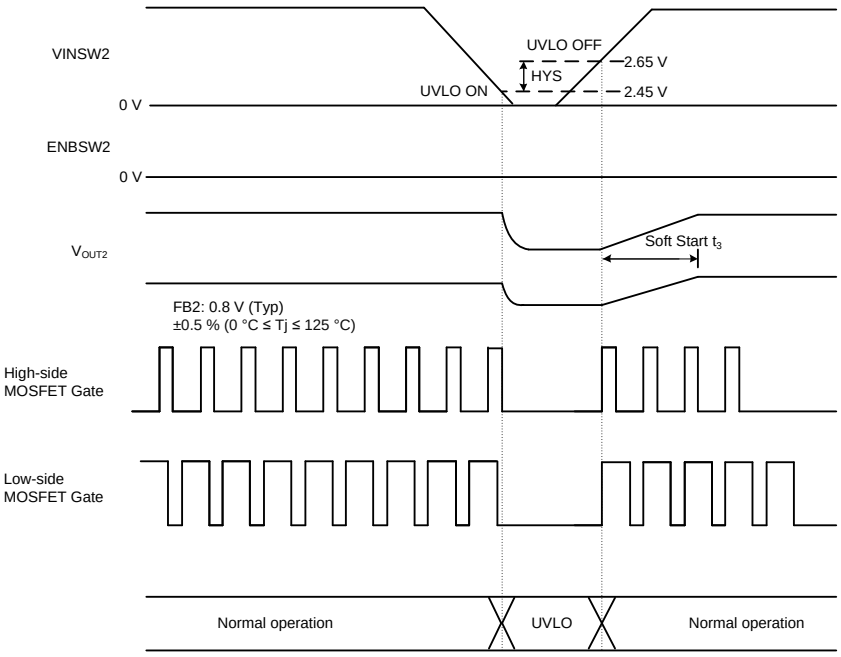


Figure 14. SWREG2 Protection Operate Timing and Soft Start Timing

Parameter	Specification			Unit
	Min	Typ	Max	
Soft Start Sime (t_3)	0.8	1.0	1.2	ms

Precautions of Board Layout

Consider the following key points when designing board layout:

1 Key points and precautions concerning the H-Bridge

1.1 VBBA, VBBB / H-Bridge Power supply Pin

Motor's drive current is flowing in it, so the wire is thick and short and has low impedance.
V_{BBx}*(Note 1)* may have big fluctuations due to motor back EMF, PWM switching noise, etc., so you must arrange the bypass capacitor of about over 220 µF as close to the pin as possible and adjust V_{BBx} is stable. Increase the capacitance if needed, especially when a large current is used or motors that have great back electromotive force are used.
In addition, for the purpose of reducing the power supply's impedance in wide frequency bandwidth, parallel connection of multi-layered ceramic capacitor of 0.01 µF to 0.1 µF etc. is recommended. Extreme care must be used to make sure that V_{BBx} does not exceed the rating even for a moment.
VBBA and VBBB are shorted inside IC, so be sure to short externally VBBA and VBBB when using. If used without shorting, malfunction or destruction may occur because of concentration of current routes etc. Moreover, in the power supply pin, there is a built-in clamp component for preventing of electrostatic destruction. If steep pulse or voltage of surge exceeding the maximum absolute rating is applied, this clamp component operates. As a result, there is danger of destruction, so make sure that the maximum absolute rating is not exceeded. It is effective to mount a Zener diode about the maximum absolute rating. Also, a diode for preventing electrostatic destruction is inserted between the VBBx pin and GND pin, as a result there is the danger of IC destruction if reverse voltage is applied between the VBBx pin and GND pin, so be careful.
(Note 1) x = A, B

1.2 OUTAP, OUTAM, OUTBP, OUTBM / H-Bridge output Pin

Motor's drive current is flowing in it, so the wire is thick and short and has low impedance. It is also effective to add a Schottky diode if output has big positive or negative fluctuations when large current is used, etc., for example, if counter electromotive voltage, etc. is big. Moreover, in the output pin, there is a built-in clamp component for preventing electrostatic destruction. If a steep pulse or voltage surge exceeding the maximum absolute rating is applied, this clamp component operates, but there is still the danger of destruction, so make sure that the maximum absolute rating is not exceeded.

1.3 RNFA, RNFB / H-Bridge Connection Pin of resistor for detecting of output current

Connect the resistor for current detection between this pin and GND. In view of the power consumption of the current-detecting resistor, determine the resistor that $W = I_{OUT}^2 \times R$ [W] does not exceed the power dissipation of the resistor. In addition, wire has low impedance and does not have impedance in common with other GND patterns because motor's drive current flows in the pattern through the RNFx*(Note 2)* pin to current-detecting resistor to GND. Do not exceed the rating because there is the possibility of circuit malfunction, etc. if the RNFx voltage has exceeded the maximum rating (0.55 V). Moreover, be careful because if the RNFx pin is shorted to GND, large current flows without normal PWM constant current control, then there is the danger that OCP or TSD will operate. If the RNFx pin is open, there is the possibility of such malfunction as output current does not flow either, so do not leave it open.
(Note 2) x = A, B

2 Key points and precautions concerning the switching regulator

2.1 VBBSW1, SWOUT1 / SWREG1 power supply pins, SWREG1 output

SWOUT1 is a high-voltage line and a possible source of switching noise. For that reason, the thickest, shortest, lowest-impedance wire possible should be used in the pattern design. Meanwhile, to reduce the switching current noise, the following loop should be kept as short as possible: bypass capacitor → VBBSW1 → SWOUT1 → Schottky diode → GND.
To lessen the impact of coupling capacitance noise, position the FB1 feedback resistor away from the SWOUT1 pattern and components.

2.2 VINSW2, SWOUT2 / SWREG2 power supply pins, SWREG2 output

SWOUT2 is a high-voltage line and a possible source of switching noise. For that reason, the thickest, shortest, lowest-impedance wire possible should be used in the pattern design. Meanwhile, to reduce the switching current noise, the following loop should be kept as short as possible: bypass capacitor → VINSW2 → SWOUT2 → GND.
To lessen the impact of coupling capacitance noise, position the FB2 feedback resistor away from the SWOUT2 pattern and components.

3 Other key points and precautions

3.1 GND, PGNDSW / Ground Pin

In order to reduce noise caused by the switching current and to stabilize the internal reference voltage of the IC, keep the wiring impedance from this pin as low as possible. The design should enable the lowest electrical potential in any operating state. In addition, be sure this wiring does not share common impedance with other GND patterns.

Reference Data

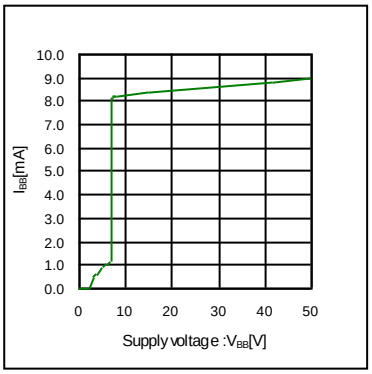


Figure 15. VBB Current1 (Ta = 25 °C)
(SLEEP = H: Active Mode)

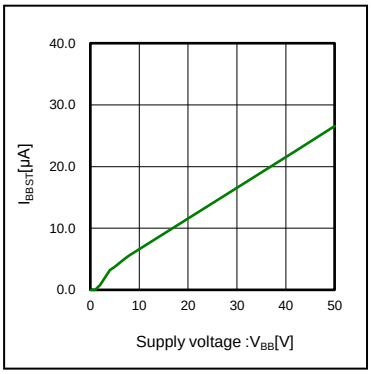


Figure 16. VBB Current2 (Ta = 25 °C)
(SLEEP = L: Sleep Mode)

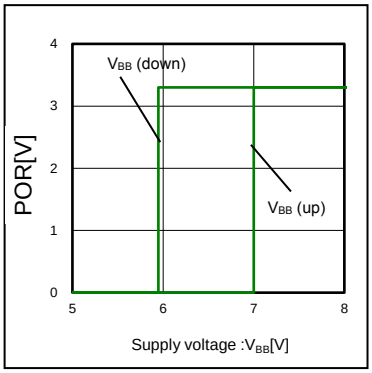


Figure 17. POR Threshold
Voltage (Ta = 25 °C)

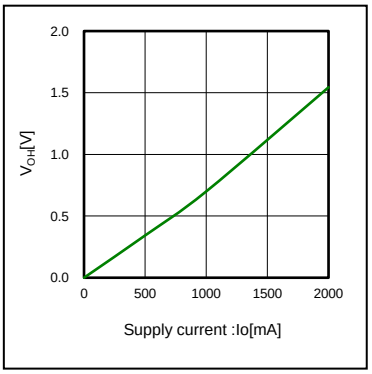


Figure 18. OUTA Output Voltage
H (source side, Ta = 25 °C)

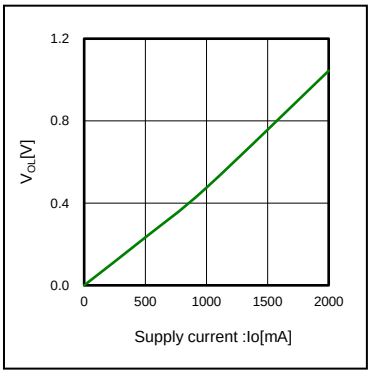


Figure 19. OUTA Output Voltage
L (sink side, Ta = 25 °C)

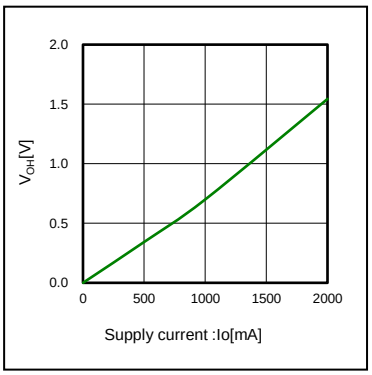


Figure 20. OUTB Output Voltage
H (source side, Ta = 25 °C)

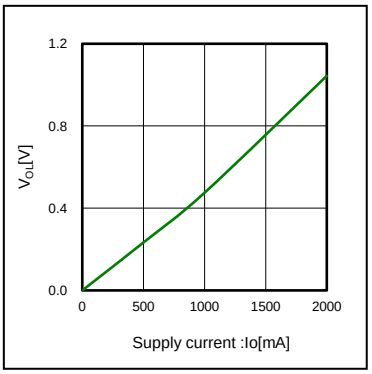


Figure 21. OUTB Output Voltage
L (sink side, Ta = 25 °C)

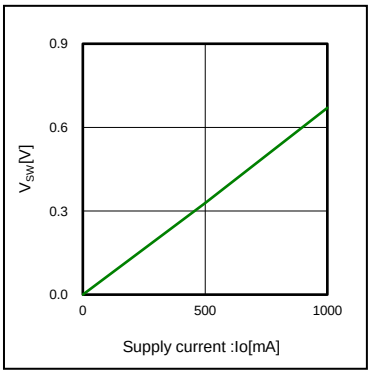


Figure 22. SWREG1 Output
Voltage H (Ta = 25 °C)

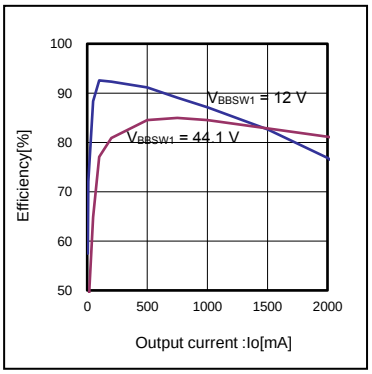


Figure 23. SWREG1 Efficiency-1
(5.0 V setting, Ta = 25 °C)

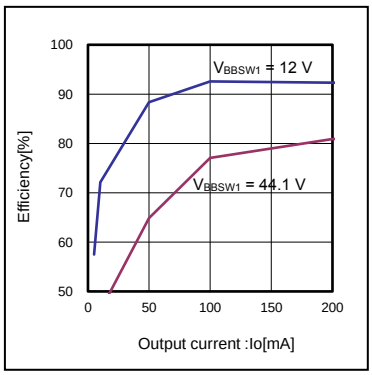


Figure 24. SWREG1 Efficiency-2
(5.0 V setting, Ta = 25 °C)

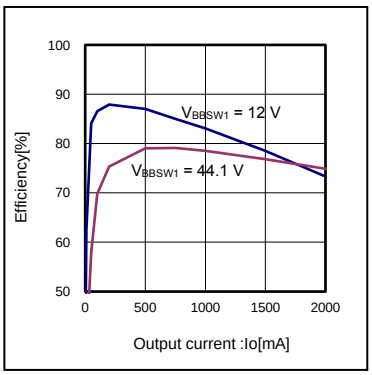


Figure 25. SWREG1 Efficiency-1
(3.3 V setting, Ta = 25 °C)

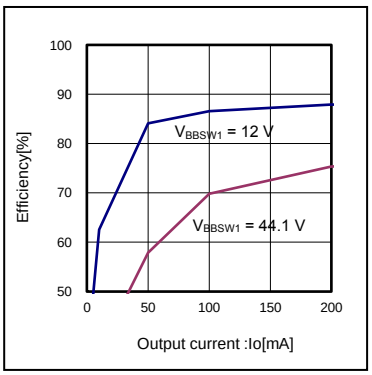


Figure 26. SWREG1 Efficiency-2
(3.3 V setting, Ta = 25 °C)

Reference Data - continued

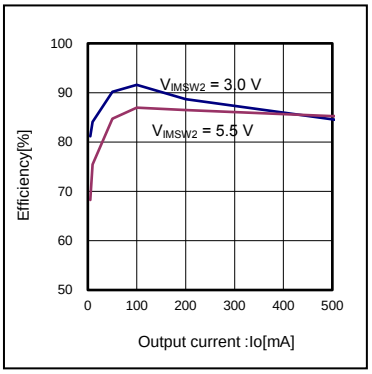


Figure 27. SWREG2 Efficiency
SLLM-1 (1.5 V setting, Ta = 25 °C)

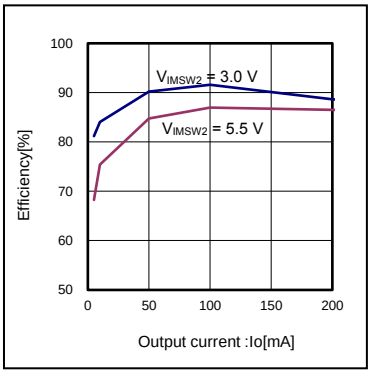


Figure 28. SWREG2 Efficiency
SLLM-2 (1.5 V setting, Ta = 25 °C)

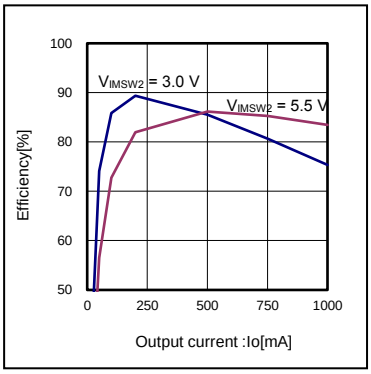


Figure 29. SWREG2 Efficiency
PWM-1 (1.5 V setting, Ta = 25°C)

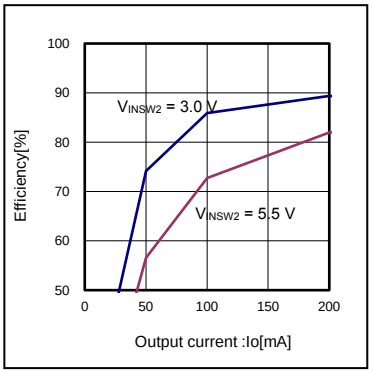


Figure 30. SWREG2 Efficiency
PWM-2 (1.5 V setting, Ta = 25 °C)

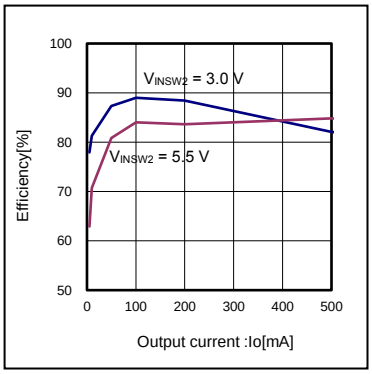


Figure 31. SWREG2 Efficiency
SLLM-1 (1.125 V setting, Ta = 25 °C)

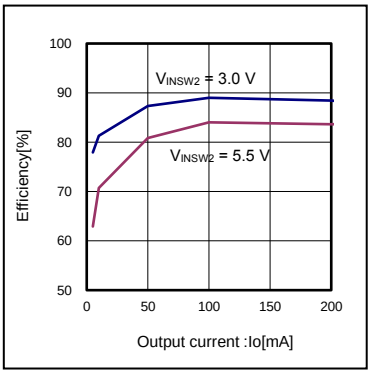


Figure 32. SWREG2 Efficiency
SLLM-2 (1.125 V setting, Ta = 25 °C)

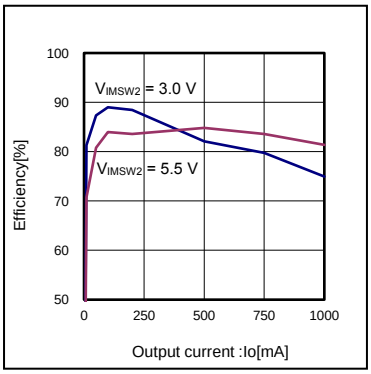


Figure 33. SWREG2 Efficiency
PWM1 (1.125 V setting, Ta = 25 °C)

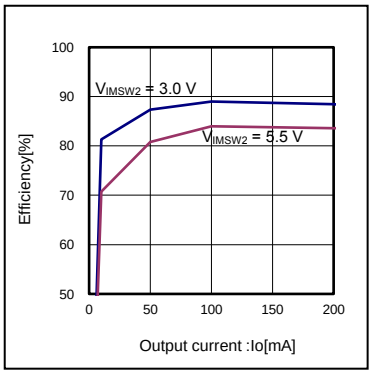


Figure 34. SWREG2 Efficiency
PWM2 (1.125 V setting, Ta = 25 °C)

SWREG1: RCH110BENP-470(SUMIDA), EC30QSA065(Nihon inter)
SWREG2: NRS5024T1R5NMGJ(TAIYO YUDEN)

Power Dissipation

VQFN048V7070 is designed with a heat sink metal on the backside of IC to perform heat dissipation treatment using through hole from backside. Before use, be sure to connect to the GND plane on the board with solder and make the GND pattern as wide as possible to secure a sufficient heat dissipation area. Note that the power dissipation described below may not be assured when not connecting by solder. The back metal is shorted with the backside of the IC chip that is a GND potential. There is a possibility for malfunction or destruction if it is shorted with any potential other than GND, which should be avoided. Please note that it has been assumed that this product will be used in the condition of this back metal performed heat dissipation treatment for increasing heat dissipation efficiency.

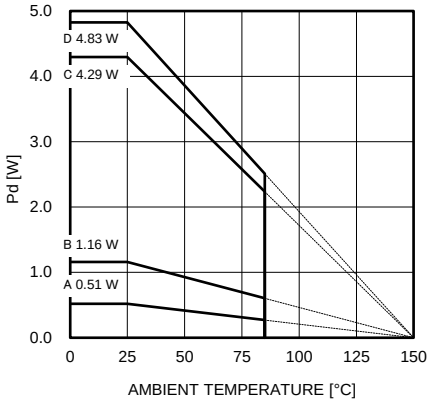


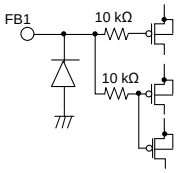
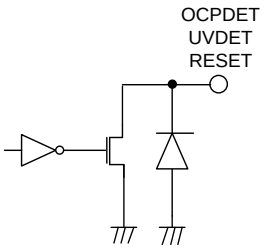
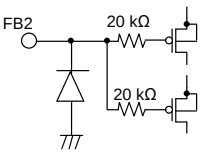
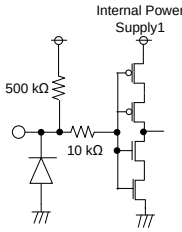
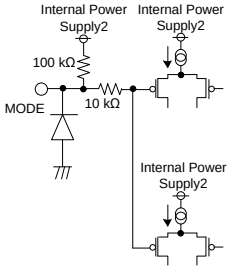
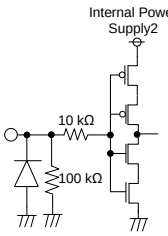
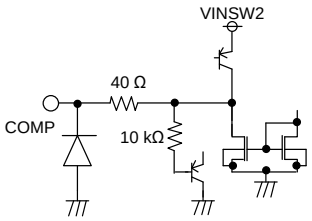
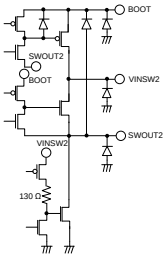
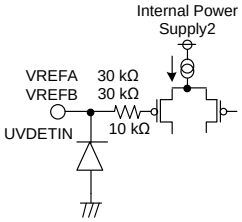
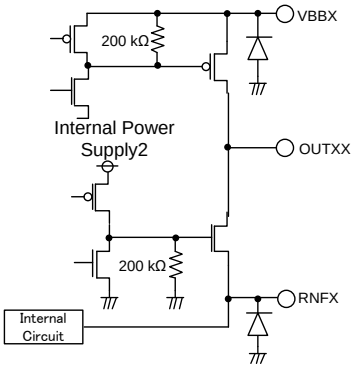
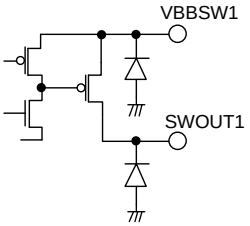
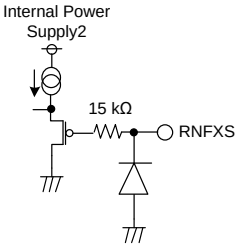
Figure 35. Thermal Derating Curve
(VQFN048V7070)

Package thermal resistor

Board	θ_{JA} [°C/W]
Board A	240.4
Board B	107.8
Board C	29.1
Board D	25.9

PCB size: 74.2 mm x 74.2 mm x 1.6 mmt
(): Copper foil pattern area size
Board A: Package only
Board B: 1 layer PCB (1 layer: 34.09 mm^2)
Board C: 4 layer PCB (1, 4 layer: 34.09 mm^2. 2, 3 layer: 5505 mm^2)
Board D: 4 layer PCB (all layers: 5505 mm^2)
Values in derating curve and packaged thermal resistor are tested values

I/O Equivalent Circuit

No.	Pin Name	Equivalent Circuit	No.	Pin Name	Equivalent Circuit
42	FB1		43	OCPDET	
18	FB2		44	UVDET	
			45	RESET	
13	ENBSW1		47	MODE	
14	ENBSW2				
15	PWM				
9	DAT		17	COMP	
7	CLK				
8	STB(LD)				
4	SLEEP				
5	ENBA				
6	ENBB				
46	RSTIN				
10	ID0				
11	ID1				
12	ID2				
21	BOOT		2	VREFA	
19 20	VINSW2		3	VREFB	
22 23	SWOUT2		48	UVDETIN	
29	VBBA		37 38	VBBSW1	
32	VBBB				
30	OUTAP		39 40	SWOUT1	
26	OUTAM				
31	OUTBP		27	RNFAS	
35	OUTBM				
28	RNFA		34	RNFBS	
33	RNFB				

Operational Notes

1 Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2 Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3 Ground Voltage
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4 Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5 Recommended Operating Conditions
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6 Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7 Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8 Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9 Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10 Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

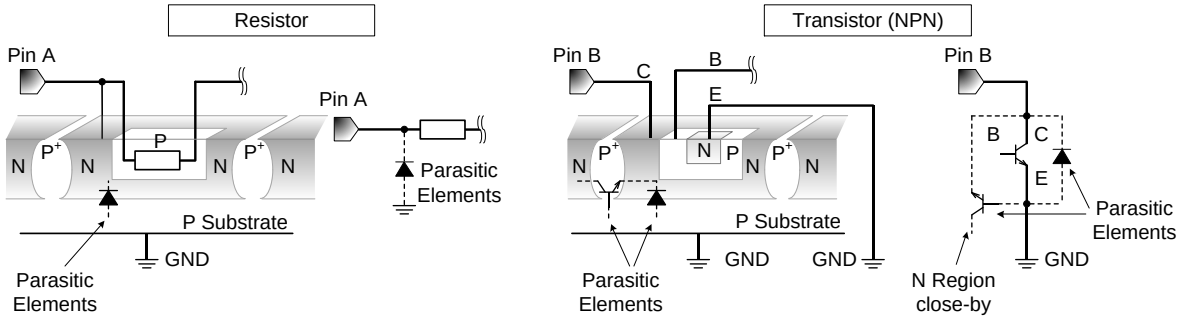


Figure 36. Example of Monolithic IC Structure

11 Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12 Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13 Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Technical information (Exempt from guarantee)

1 About logic input pins for control
Response time from rising edge of CLK signal is 20 µs.

2 In case RESET function is used when SWREG is unused
Divide the power supply (V_{BB}) by resistor voltage divider, and input into the FB1 pin.
In doing so, using RESET function becomes possible.
In this case, it is necessary to make ENBSW1 L level.
Because this function is only assumed when designing, evaluate and confirm it.

3 Internal power supply 1
Internal power supply 1 applies 4.4 V (Typ) ±10 % dispersion.

4 Internal power supply 2
Internal power supply 2 applies 5 V (Typ) ±10 % dispersion.

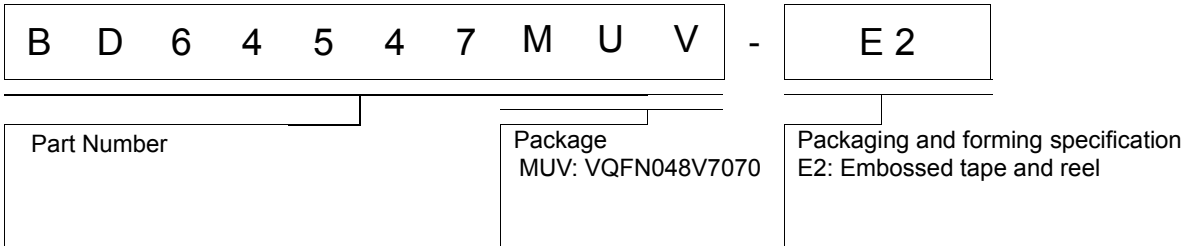
5 VREF to RNFS offset voltage (Refer P.4)
DAC = 3, accuracy ±10 %
DAC = 15, accuracy ±4 %

6 ON-Resistance (H-Bridge)
Listed value is only for I_{OUT} = 1 A, but the value is equal about I_{OUT} = 0.5 A.

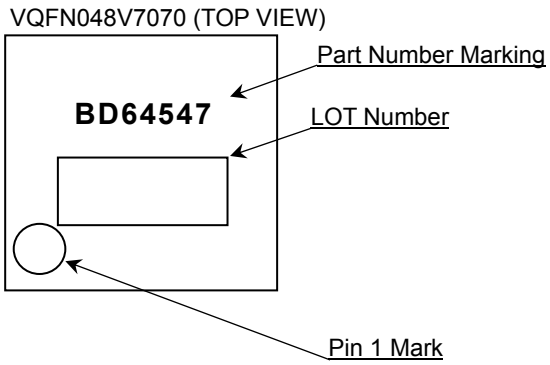
7 Thermal Shutdown Circuit (TSD)
The overheat protection works in 175 °C (Typ), but the overheat protection temperature cannot be less than 150 °C even if it varies with each IC.

8 Adjacent Pins short
When VBBx*(Note 1)* and RNFx*(Note 1)* short-circuits, the IC may destroy it.
(Note 1) x = A, B

Ordering Information

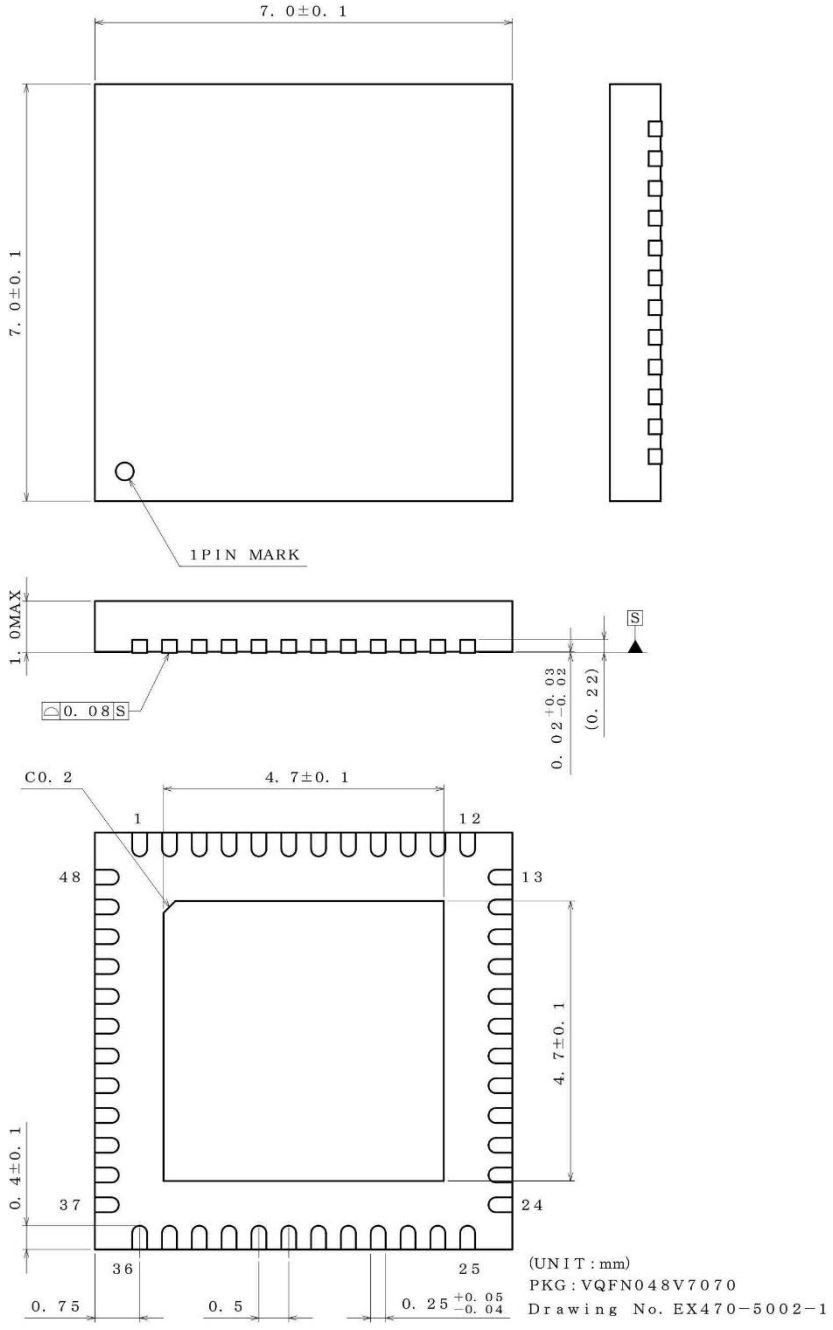


Marking Diagram



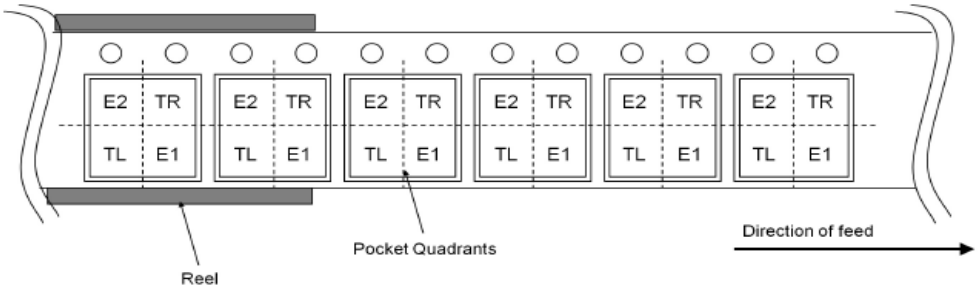
Physical Dimension, Tape and Reel Information

Package Name	VQFN048V7070



< Tape and Reel Information >

Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
-	001	No Release
18.Jan.2018	002	New Release
28.Aug.2018	003	P6, P.7 In the table describing the processing of the MODE terminal, change the setting of "MODE=L" to "Don't use". P.10, P.12, P.14 Delete description of Large Mode. Accordingly, the total number of pages was reduced from 36 to 35 pages. P.22 RESET OUT truth table changed. P.24 Change to the description in Protection Functions - continued.
27.Dec.2019	004	P.7 to P.26 Changed index P.7 (3), (4) Changed place from P.23 P.23 (1) Added explanation
15.Jan.2020	005	P.31 Changed I/O Equivalence Circuit
16.Nov.2020	006	Updated according to the latest format.

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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