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## MAX40110/MAX40111

## 15MHz, Low-Noise, Precision Operational Amplifiers

### General Description

The MAX40110/MAX40111 offer a unique combination of high speed, precision, low noise, and low-voltage operation, making them ideally suited for a large number of signal processing functions including filtering and amplification of signals in portable and industrial equipment.

The MAX40110/MAX40111s' rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 14-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump. The input offset voltage is as low as 30 $\mu$ V due to the auto-calibration performed on power-up. The devices also include a fast-power-on shutdown mode for further power savings.

The MAX40110/MAX40111 operate from a supply range of 1.8V to 5.5V over the -40°C to +125°C extended operating temperature range and consume only 750 $\mu$ A (typ) supply current. The MAX40110 is offered in an ultra-thin 6- $\mu$ DFN package, and the MAX40111 is available in a tiny 6-bump wafer-level-package (WLP) with a 0.4mm pitch.

The MAX40110/MAX40111 are an extension of the MAX44259/60/61/63 and MAX44290 families with a reduced power up time of less than 1ms.

### Applications

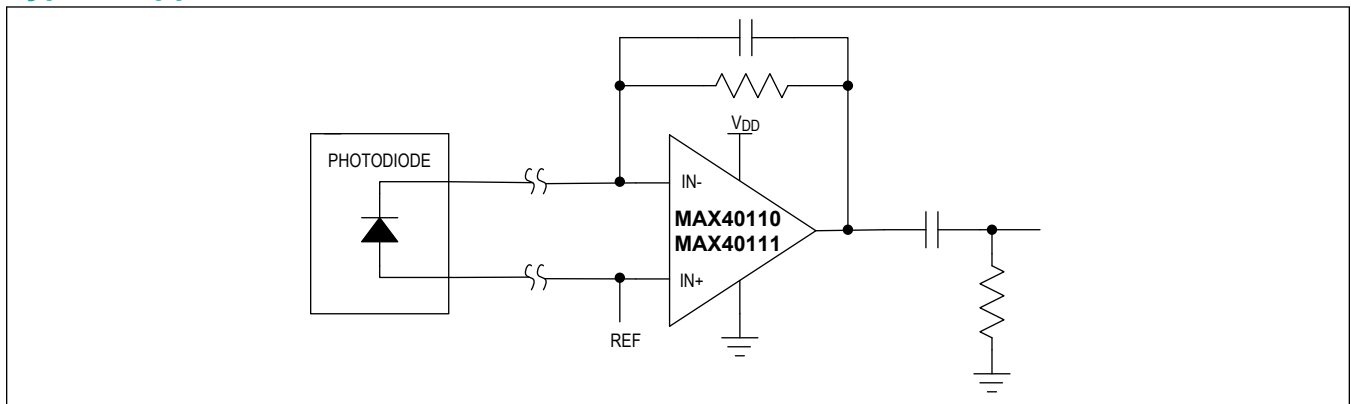
- Wearable Devices
- Home Medical (Blood Glucose, Weight Scale, Blood Pressure, EKG)
- Industrial IOT (Pressure, Flow, Level, Temperature, Proximity)
- Optical Sensors
- SAR ADC Driver

### Benefits and Features

- Fast Power-up Time of less than 1ms
- Supply Voltage Range: 1.7V to 5.5V
- Low 140 $\mu$ V (Max) Input Offset Voltage with Power-On Auto-Cal at +25°C
- 15MHz GBW
- Low 12.7nV/ $\sqrt{\text{Hz}}$  Input Voltage-Noise Density
- 750 $\mu$ A Quiescent Current
- Rail-to-Rail Inputs and Outputs
- Internal EMI Rejection
- <1pA Low Input Bias Current
- Power-Saving Shutdown Mode
- Available in a Tiny 6-bump WLP and a Thin 6- $\mu$ DFN Package

*Ordering Information appears at end of data sheet.*

### Typical Application Circuit



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**Absolute Maximum Ratings**

V <sub>DD</sub> to GND.....	-0.3V to +6V	Continuous Power Dissipation (WLP (Derate 10.51mW/°C above +70°C)) .....	840.8mW
SHDN .....	-0.3V to +6V	Operating Temperature Range .....	-40°C to +125°C
IN+, IN- Maximum Voltage .....	Self Limiting*	Junction Temperature .....	+150°C
OUT to GND .....	-0.3 to (V <sub>DD</sub> + 0.3V)	Storage Temperature Range .....	-65°C to +150°C
Output Short-Circuit Duration to V <sub>DD</sub> or GND .....	Continuous	Lead Temperature (soldering, 10s).....	+300°C
Continuous Current into Any Input/Output Pin .....	±10mA	Soldering Temperature (reflow) .....	+260°C
Differential Input Voltage .....	±6V		
Continuous Power Dissipation (µDFN (Derate 2.1mW/°C above +70°C)).....	170mW		

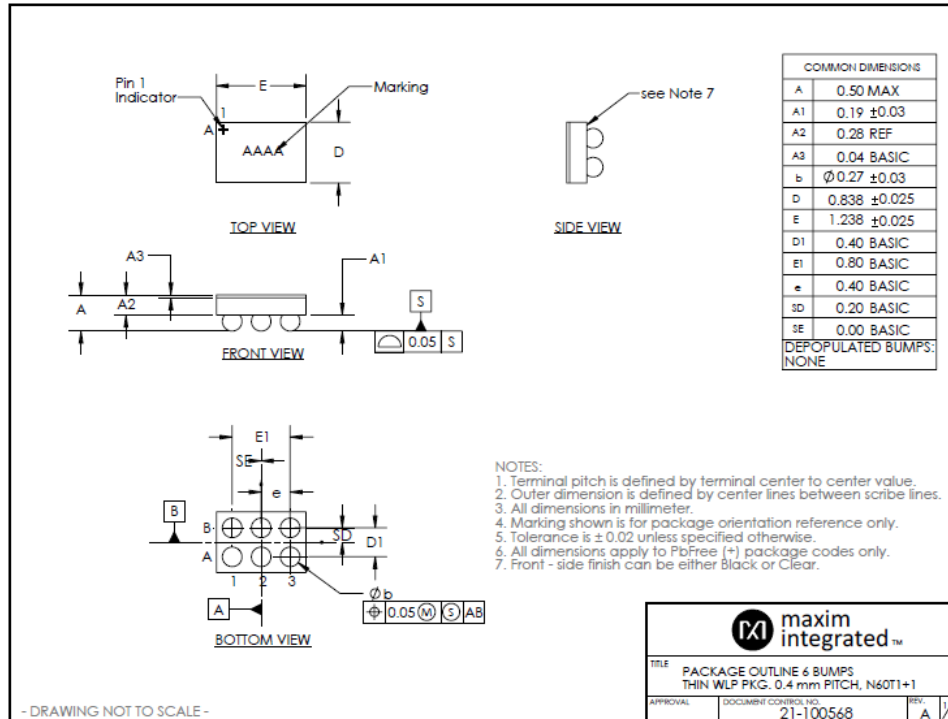
**Note:** \*Not to exceed +6V.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Package Information**

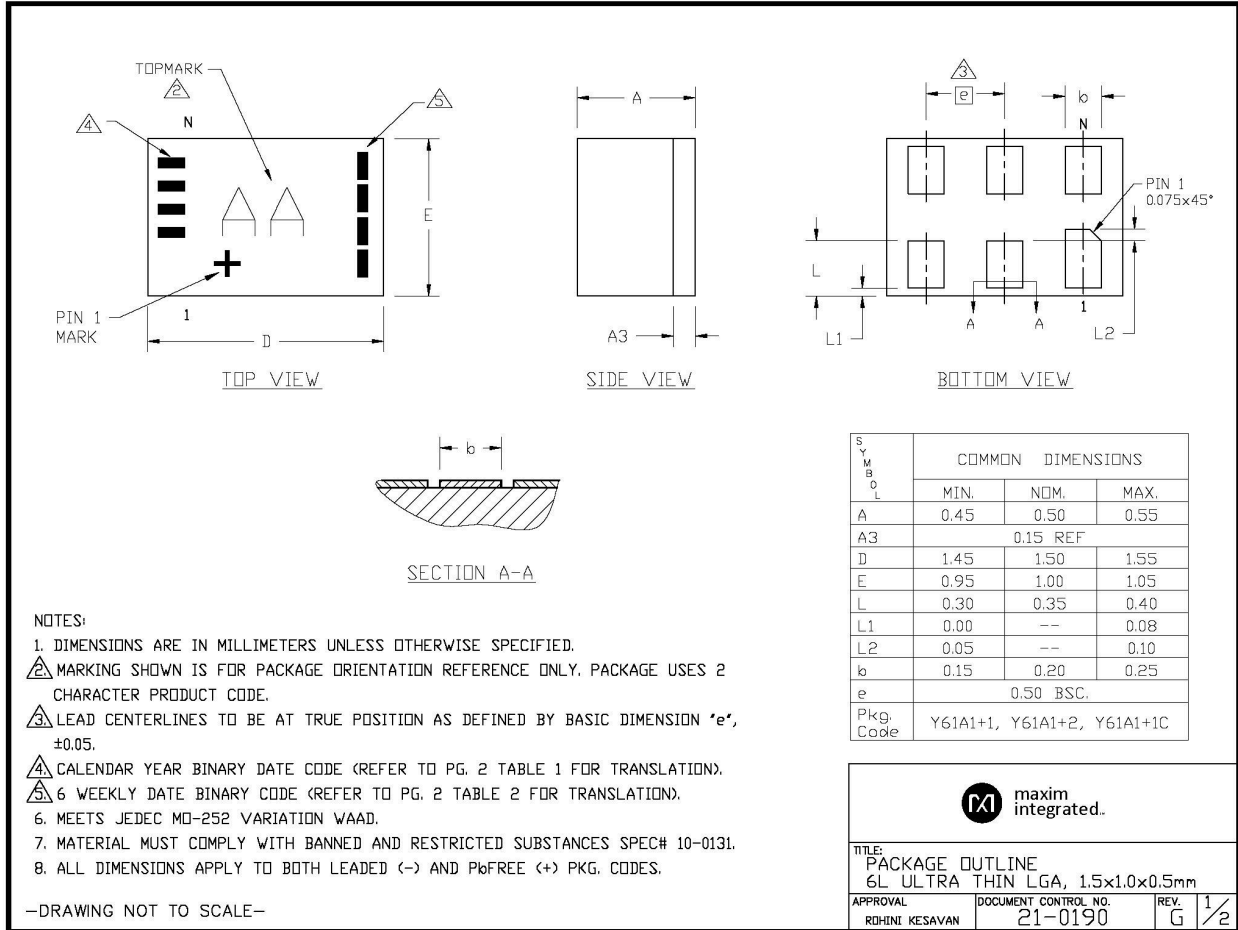
**WLP**

Package Code	N60T1+1
Outline Number	<a href="#">21-100568</a>
Land Pattern Number	Refer to Application Note 1891
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	95.15°C/W
Junction to Case (θ <sub>JC</sub> )	N/A



**6 Thin μDFN (Ultra-Thin LGA)**

Package Code	Y61A1+1
Outline Number	<a href="#">21-0190</a>
Land Pattern Number	<a href="#">90-0233</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	470°C/W
Junction to Case ( $\theta_{JC}$ )	120°C/W



**TABLE 1** Translation Table for Calendar Year Code

Calendar Year	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
	■	■	□	■	□	□	□	■	□	□	■	□	■	■	■
	□	■	■	■	□	□	■	□	□	■	□	■	□	■	■
	■	□	■	■	□	■	□	□	■	□	□	■	■	□	■
	■	■	■	■	■	□	□	□	■	■	■	□	□	□	□


Legend: ■ Marked with bar □ Blank space - no bar required

**TABLE 2** Translation Table for Payweek Binary Coding

Payweek	06-11	12-17	18-23	24-29	30-35	36-41	42-47	48-51	52-05
	□	□	□	■	□	□	■	□	■
	□	□	■	□	□	■	□	■	□
	□	■	□	□	■	□	□	■	■
	■	□	□	□	■	■	■	□	□

Legend: ■ Marked with bar □ Blank space - no bar required



TITLE:  
PACKAGE OUTLINE  
6L ULTRA THIN LGA, 1.5x1.0x0.5mm

APPROVAL: RDHINI KESAVAN    DOCUMENT CONTROL NO. 21-0190    REV. G    2/2

-DRAWING NOT TO SCALE-

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### Electrical Characteristics

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $+25^{\circ}C$ . (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC SPECIFICATIONS</b>						
Input Common-Mode Range	$V_{CM}$	Guaranteed by CMRR test	-0.1		$V_{DD} + 0.1$	V
Common-Mode Rejection Ratio	CMRR	$-0.1V \leq V_{CM} \leq V_{DD} + 0.1V$	75	90		dB
Input Offset Voltage	$V_{OS}$	$T_A = +25^{\circ}C$ (Note 2)		30	140	$\mu V$
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (Note 3)			190	
		$-40^{\circ}C \leq T_A \leq +125^{\circ}C$ (Note 4)			600	

**Electrical Characteristics (continued)**

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $+25^\circ C$ . (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage Drift	TC $V_{OS}$	(Note 5)		1	6	$\mu V/^\circ C$
Input Bias Current	$I_B$	$-40^\circ C \leq T_A \leq +85^\circ C$ (Note 5)		1	12	pA
		$-40^\circ C \leq T_A \leq +125^\circ C$ (Note 5)			200	
Input Offset Current	$I_{OS}$	$-40^\circ C \leq T_A \leq +85^\circ C$ (Note 5)		1	12	pA
		$-40^\circ C \leq T_A \leq +125^\circ C$ (Note 5)			200	
Open-Loop Gain	$A_{OL}$	$0.4V \leq V_{OUT} \leq (V_{DD} - 0.4V)$	$R_{LOAD} = 10k\Omega$ to $V_{DD}/2$	100	115	dB
			$R_{LOAD} = 600\Omega$ to $V_{DD}/2$	91	100	
Output Voltage Swing High	$V_{OH}$	$V_{DD} - V_{OUT}$	$R_{LOAD} = 10k\Omega$ to $V_{DD}/2$		10	mV
			$R_{LOAD} = 600\Omega$ to $V_{DD}/2$		40	
Output Voltage Swing Low	$V_{OL}$	$V_{OUT}$	$R_{LOAD} = 10k\Omega$ to $V_{DD}/2$		20	mV
			$R_{LOAD} = 600\Omega$ to $V_{DD}/2$		50	
Short Circuit Current	$I_{SC}$	To $V_{DD}$ or GND		50		mA
<b>AC SPECIFICATIONS</b>						
Input Voltage Noise Density	$e_N$	$f = 10kHz$		12.7		$nV/\sqrt{Hz}$
Input Voltage Noise		0.1Hz to 10Hz		10		$\mu V_{P-P}$
Input Current Noise Density	$I_N$	$f = 10kHz$		1.2		$fA/\sqrt{Hz}$
Input Capacitance	$C_{IN}$			2.5		pF
Gain Bandwidth Product	GBW			15		MHz
Slew Rate	SR	$A_V = 1V/V$ , $V_{OUT} = 2V_{P-P}$ , 10% to 90%		7		$V/\mu s$
Capacitive Loading Stability		No sustained oscillation		300		pF
Total Harmonic Distortion + Noise	THD+N	$V_{OUT} = 2V_{P-P}$ , $A_V = 1V/V$ , $R_{LOAD} = 10k\Omega$ , $f = 10kHz$		-105		dB
Settling Time		$V_{OUT} = 2V_{P-P}$ , $A_V = 1V/V$ , $C_{LOAD} = 30pF$ , settle to 0.01%,		1.7		$\mu s$
Output Transient Recovery Time		$\Delta V_{OUT} = 0.2V$ , $V_{DD} = 3.3V$ , $A_V = 1V/V$ , $R_S = 20\Omega$ , $C_{LOAD} = 1nF$		1		$\mu s$
<b>POWER SUPPLY</b>						
Supply Voltage	$V_{DD}$	Guaranteed by PSRR	1.8		5.5	V
		$T_A = 0^\circ C$ to $+70^\circ C$	1.7		5.5	
Power-Supply Rejection Ratio	PSRR	$V_{CM} = V_{DD}/2$	78	95		dB
Supply Current	$I_{DD}$			750	1,200	$\mu A$
Shutdown Supply Current	$I_{SHDN}$				1	$\mu A$



**Electrical Characteristics (continued)**

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $+25^\circ C$ . (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Up Time	$t_{ON}$	Includes power-on $V_{OS}$ self-calibration	$V_{DD} = 0V$ to $3V$ step, $AV = 1V/V$ (Note 5)		0.6	1	ms
Shutdown Turn-On Time	$t_{SHDN}$	$-40^\circ C < T_A < +125^\circ C$ (Note 5)			15	29	$\mu s$
<b>LOGIC INPUT DC CHARACTERISTICS (<math>\overline{SHDN}</math>)</b>							
Input Low Level	$V_{IL}$					0.5	V
Input High Level	$V_{IH}$			1.3			V
Shutdown Input Bias Current	$I_{IL} / I_{IH}$					1	$\mu A$

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ C$ . All temperature limits are guaranteed by design.

**Note 2:** At  $T_A = +25^\circ C$ , on power-up and after calibration.

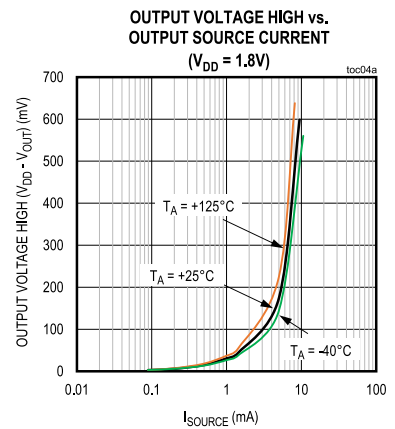
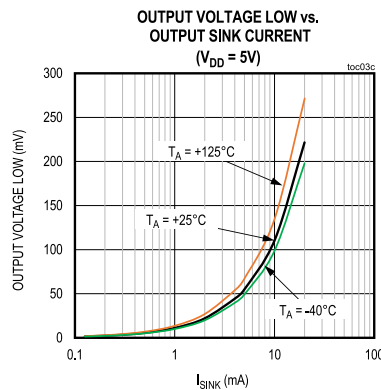
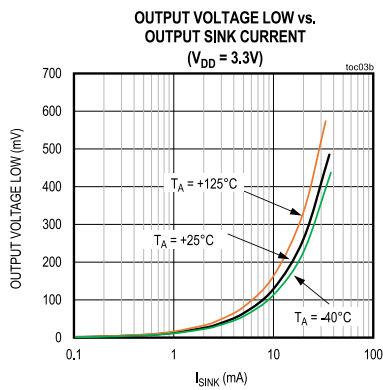
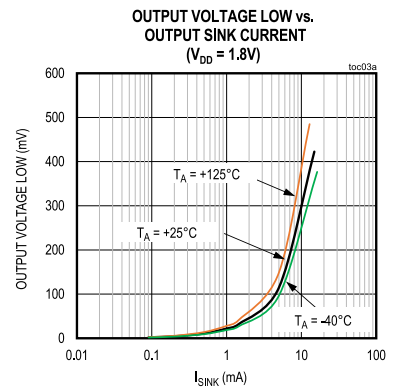
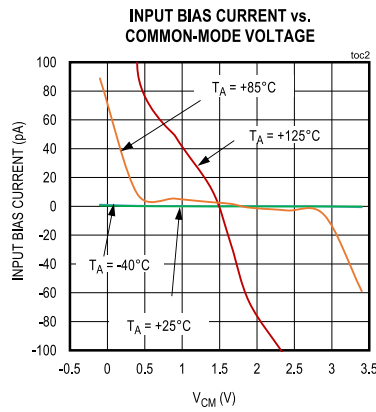
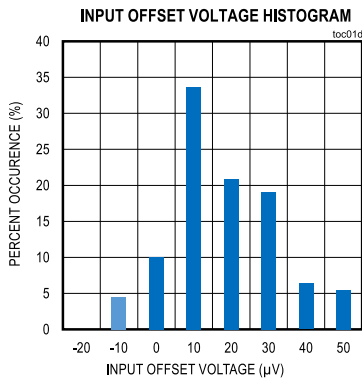
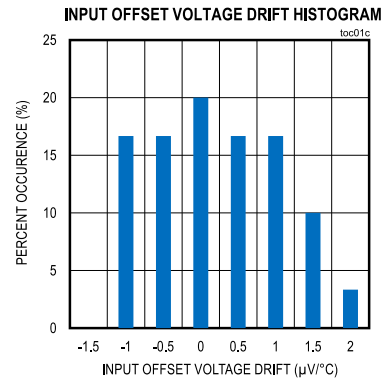
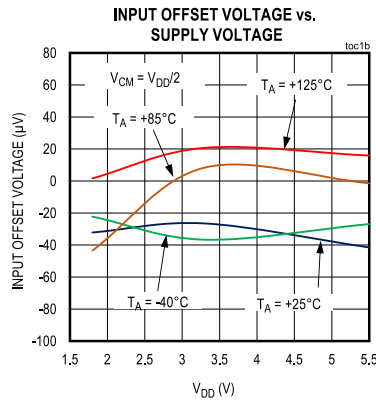
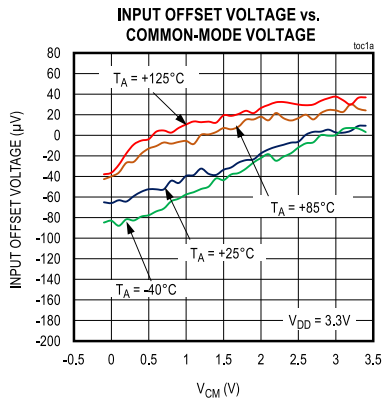
**Note 3:** For any temperature values between  $-40^\circ C$  to  $+125^\circ C$ , on power-up and after calibration.

**Note 4:** For any temperature values between  $-40^\circ C$  to  $+125^\circ C$ , it indicates the maximum drift from the initially calibrated value at power-up.

**Note 5:** Not production tested, guaranteed by design and bench characterization.

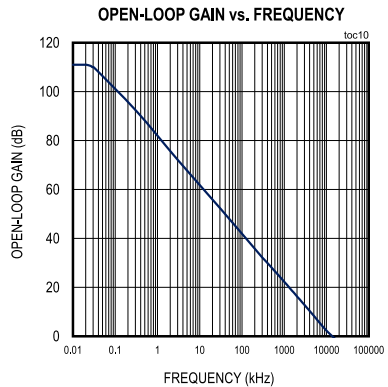
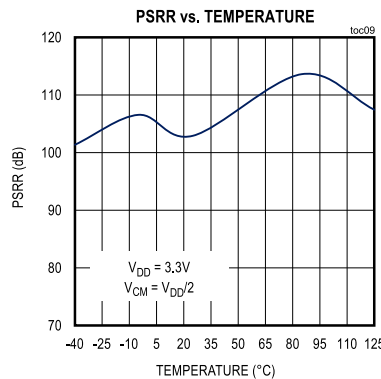
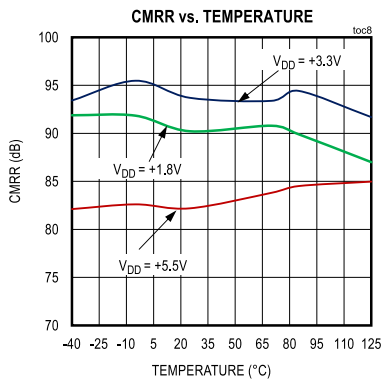
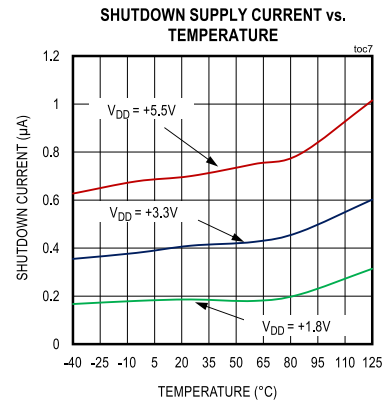
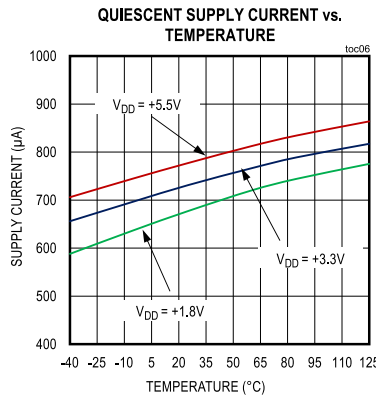
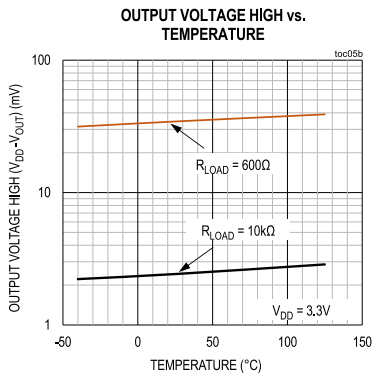
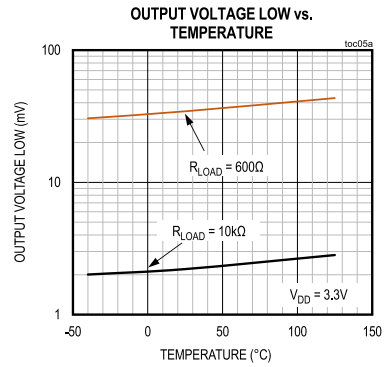
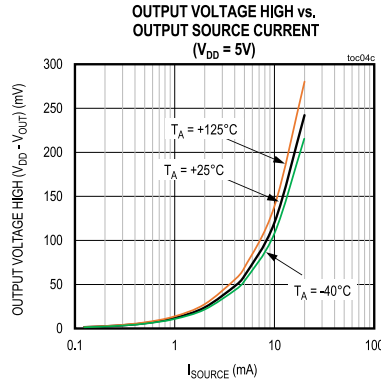
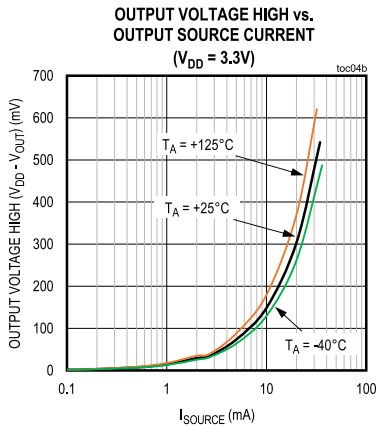
Typical Operating Characteristics

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $\sqrt{SHDN} = V_{DD}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



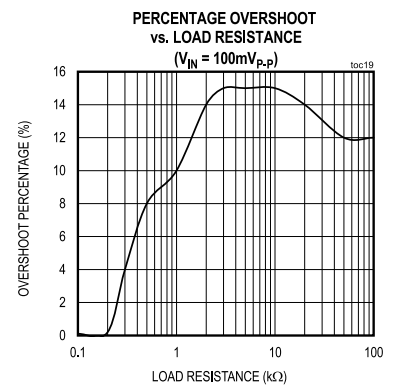
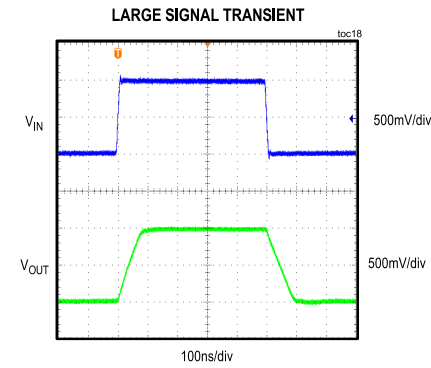
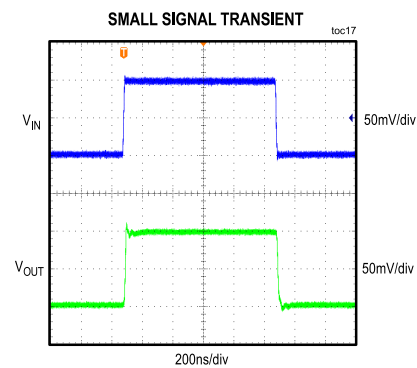
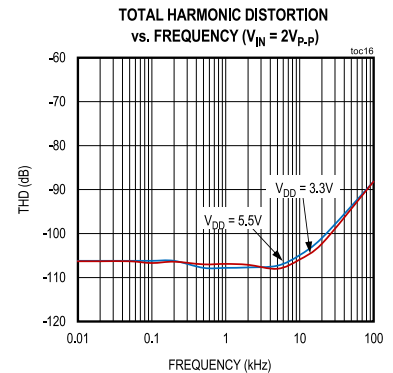
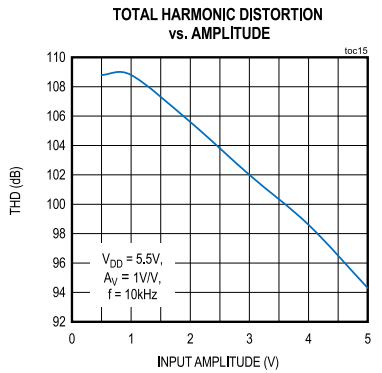
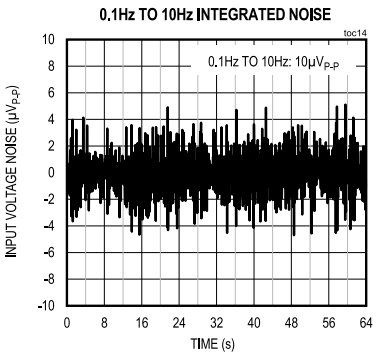
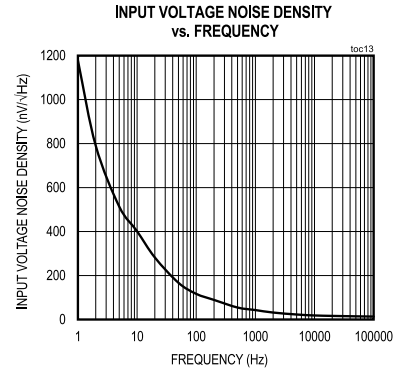
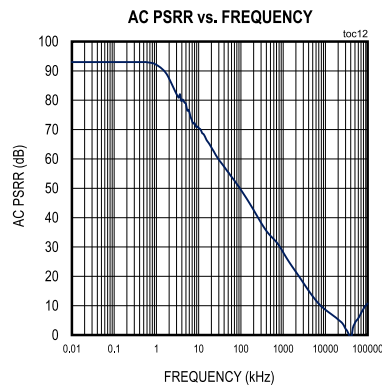
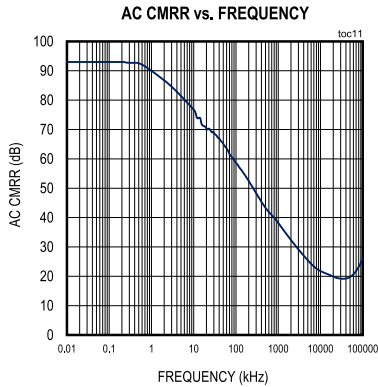
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



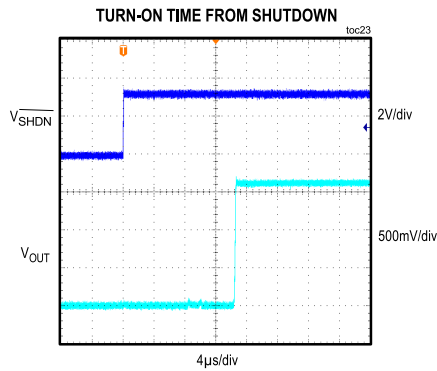
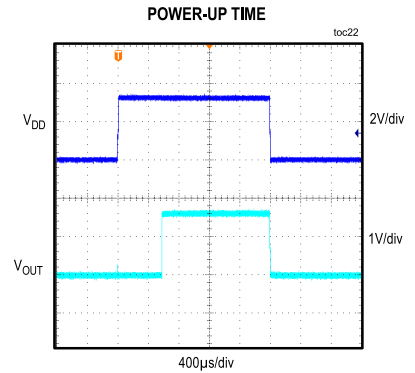
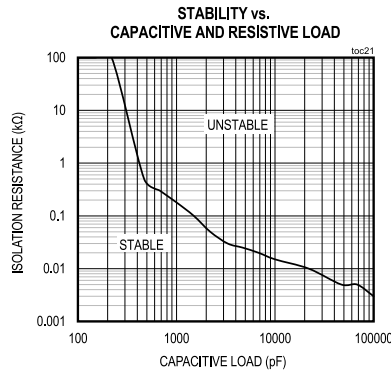
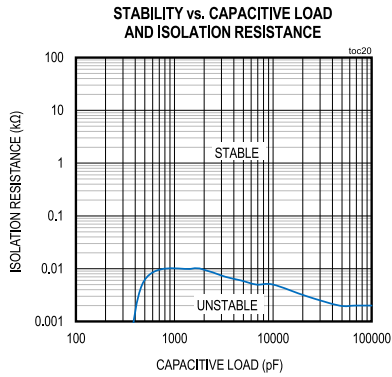
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $V_{SHDN} = V_{DD}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



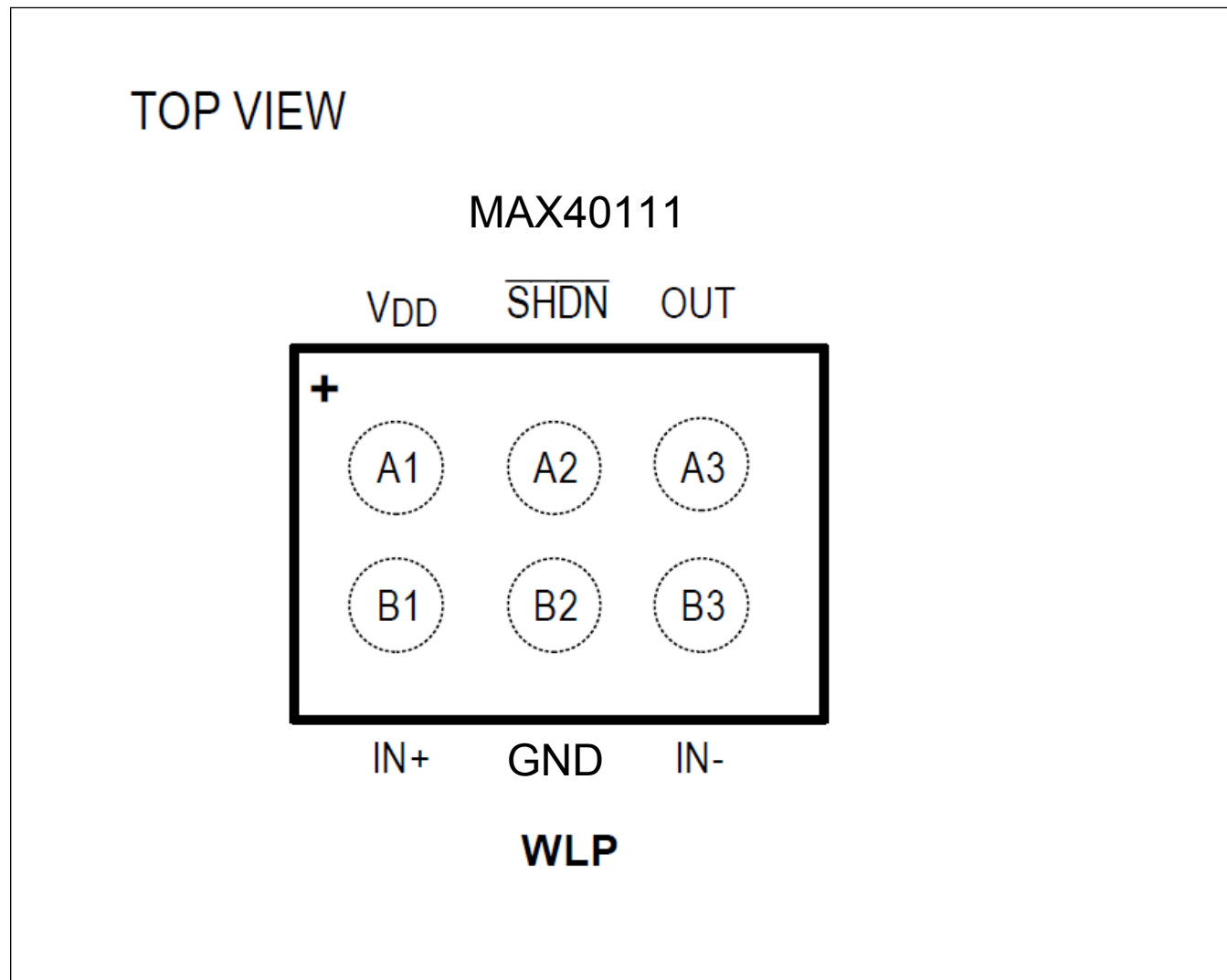
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $GND = 0$ ,  $V_{CM} = V_{DD}/2$ ,  $R_{LOAD} = 10k\Omega$  to  $V_{DD}/2$ ,  $\overline{V_{SHDN}} = V_{DD}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

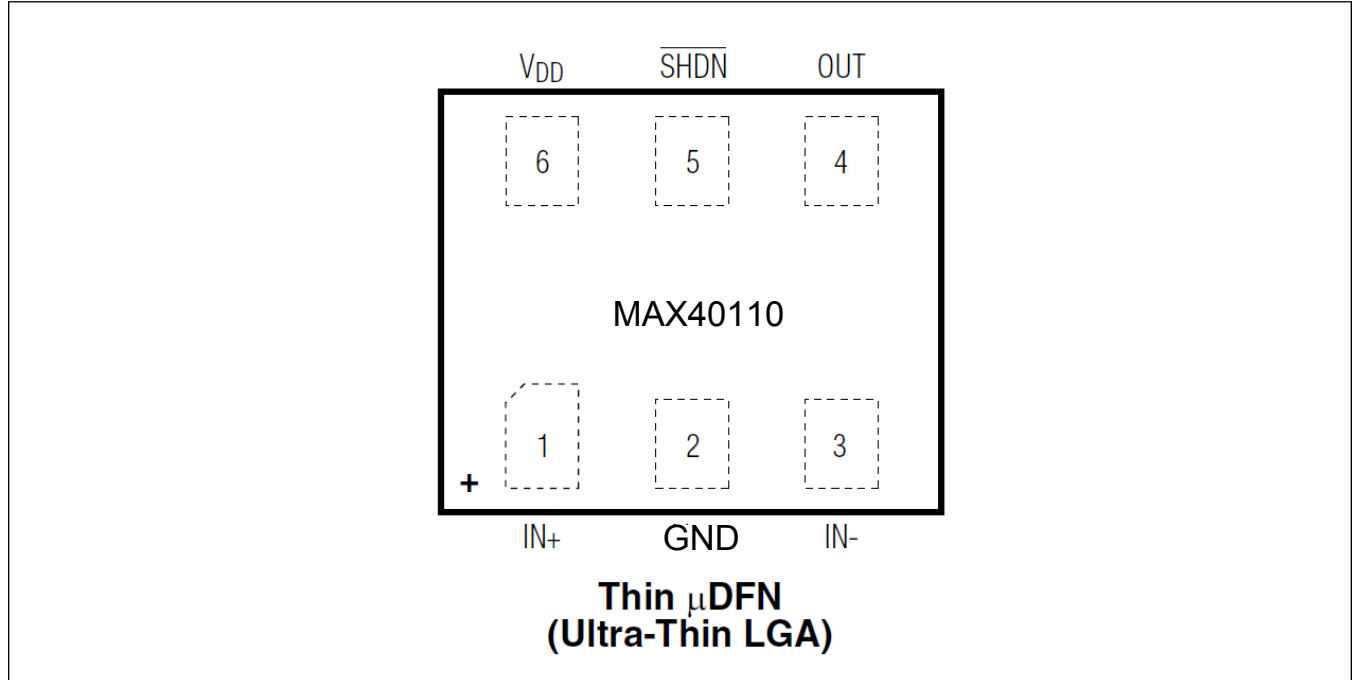


### Pin Configurations

#### WLP



**μDFN**



**Pin Description**

PIN		NAME	FUNCTION
WLP	μDFN		
B1	1	IN+	Noninverting Input
B2	2	GND	Ground
B3	3	IN-	Inverting Input
A3	4	OUT	Output
A2	5	$\overline{\text{SHDN}}$	Active-Low Shutdown Input
A1	6	VDD	Positive Supply Voltage

## Detailed Description

The MAX40110/MAX40111 are high-speed, low-power op-amps ideal for signal processing applications due to the devices' high precision and low-noise CMOS inputs. The devices self-calibrate on power-up to eliminate the effects of temperature and power supply variation.

The MAX40110/MAX40111 have a low-power shutdown mode that greatly reduces quiescent current when not in operation and recovers in 30 $\mu$ s. The MAX40110/MAX40111 feature autocalibration at power-up event and the calibration routine takes 1ms.

## Crossover Distortion

The devices feature a low-noise integrated charge pump that creates an internal voltage rail 1V above  $V_{DD}$ , which powers the input differential pair of PMOS transistors as shown in [Figure 1](#). This unique architecture eliminates crossover distortion common in traditional CMOS input architecture [Figure 2](#), especially when used in a noninverting configuration, such as Sallen-Key filters.

The charge pump operating frequency lies well above the unity-gain frequency of the amplifier. Because of its high frequency operation and ultra-quiet circuitry, the charge pump generates little noise, does not require external components, and is entirely transparent to the user.

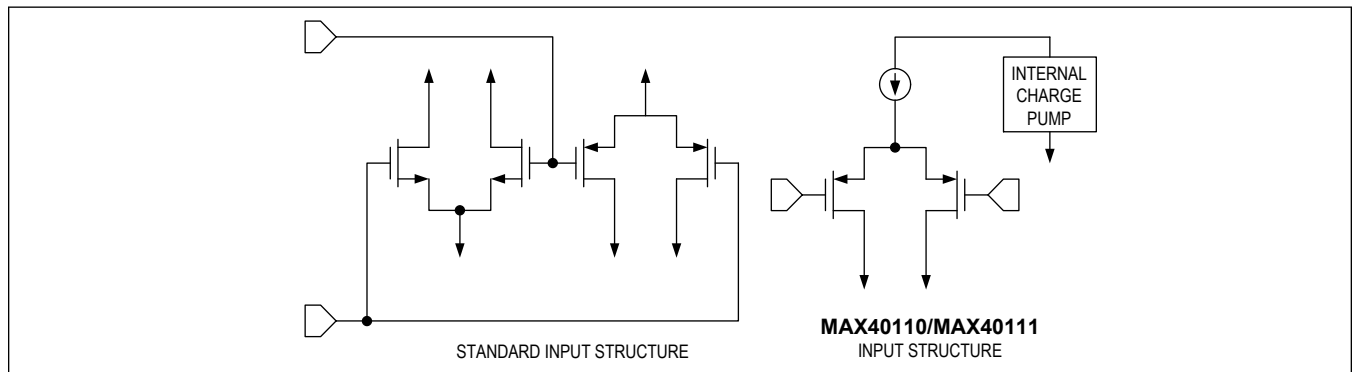


Figure 1. Comparing the Input Structure of the MAX40110/MAX40111 to Standard Op-Amps



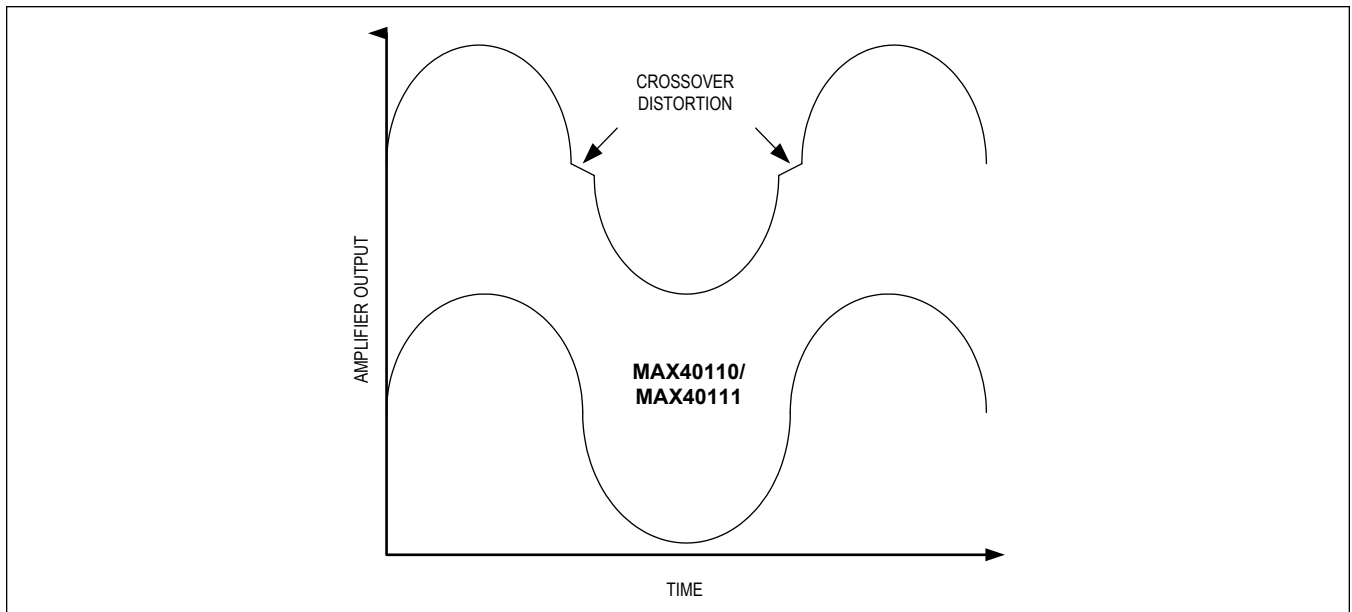


Figure 2. Crossover Distortion of Typical Amplifiers

## Applications Information

### Power-Up Autotrim

The MAX40110/MAX40111 feature an automatic trim that self-calibrates the input offset voltage ( $V_{OS}$ ) to less than  $30\mu\text{V}$  of input offset voltage on power-up. This self-calibration feature allows the device to eliminate input offset voltage effects due to power supply and operating temperature variation simply by cycling its power. The autotrim sequence takes less than 1ms to complete and is triggered by an internal power-on-reset (POR) circuitry. During this time, the inputs and outputs are at high impedance and left unconnected.

### Shutdown Operation

The MAX40110/MAX40111 have an active-low shutdown mode that puts both inputs and outputs into high impedance and substantially lowers the quiescent current to less than  $1\mu\text{A}$ . Putting the output into high impedance allows multiple outputs to be multiplexed onto a single output line without the additional external buffers. The device does not self-calibrate when exiting shutdown mode and retains its power-up trim settings. [Figure 3](#) shows how the device recovers from shutdown in less than  $30\mu\text{s}$ .

The shutdown logic levels of the device are independent of supply, allowing the shutdown feature of the device to operate off a 1.8V or 3.3V microcontroller regardless of supply voltage.

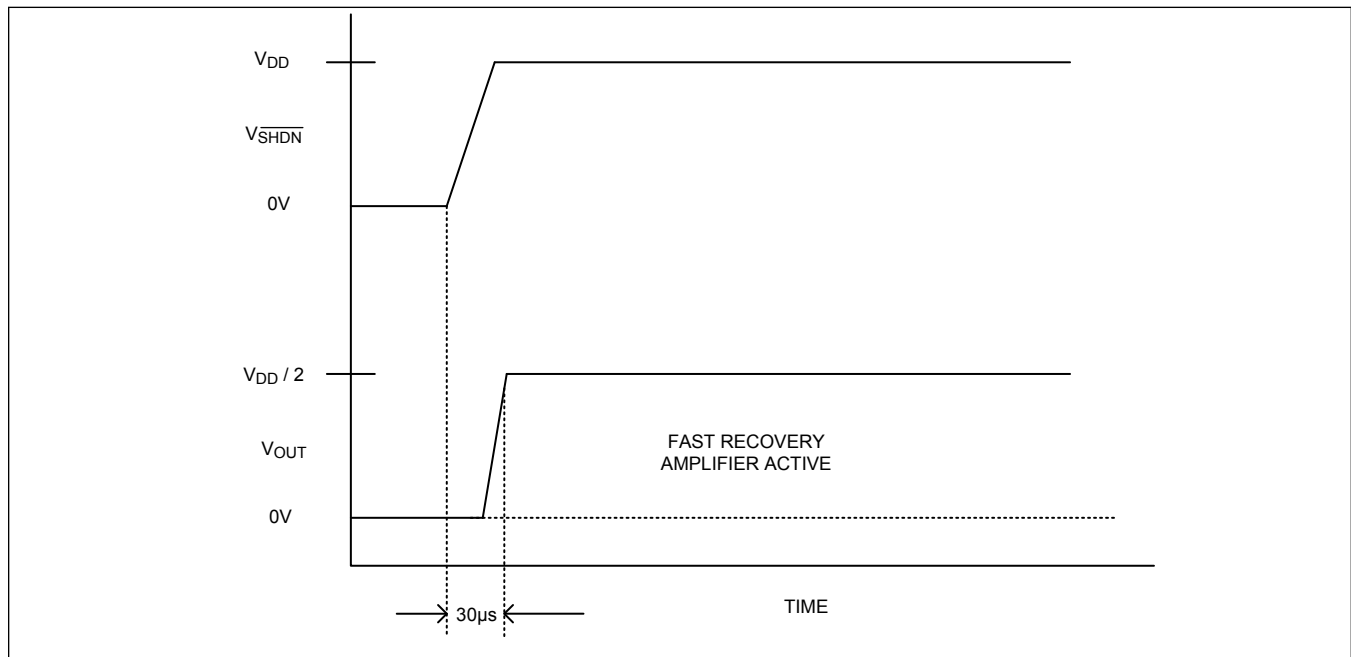


Figure 3. Shutdown Input Operation

### Rail-to-Rail Input/Output

The input voltage range of the device extends  $100\text{mV}$  above  $V_{DD}$  and below GND. The wide input common mode voltage range allows the op-amp to be used as a buffer and as a differential amplifier in a variety of signal processing applications. Output voltage high/low is only  $50\text{mV}$  above GND and below  $V_{DD}$ , allowing maximum dynamic range in single-supply applications. The high output current and capacitance drive capability of the devices make them ideal as an ADC driver and a line driver.

**Input Bias Current**

The MAX40110/MAX40111 feature a high-impedance CMOS input stage and a specialized ESD structure that allows low input bias current operation at low-input, common-mode voltages. Low-input bias current is useful when interfacing with high-impedance sensors. It is also beneficial for designing transimpedance amplifiers for photodiode sensors. This makes these devices ideal for ground referenced medical and industrial sensor applications.

**Active Filters**

The MAX40110/MAX40111 are ideal for a wide variety of active filter circuits that make use of their wide bandwidth, rail-to-rail input/output stages and high-impedance CMOS inputs. Figure 4 shows an example Sallen-Key active filter circuit with a corner frequency of 10kHz. At low frequencies, the amplifier behaves like a simple low-distortion noninverting buffer, while its high bandwidth gives excellent stopband attenuation above its corner frequency.

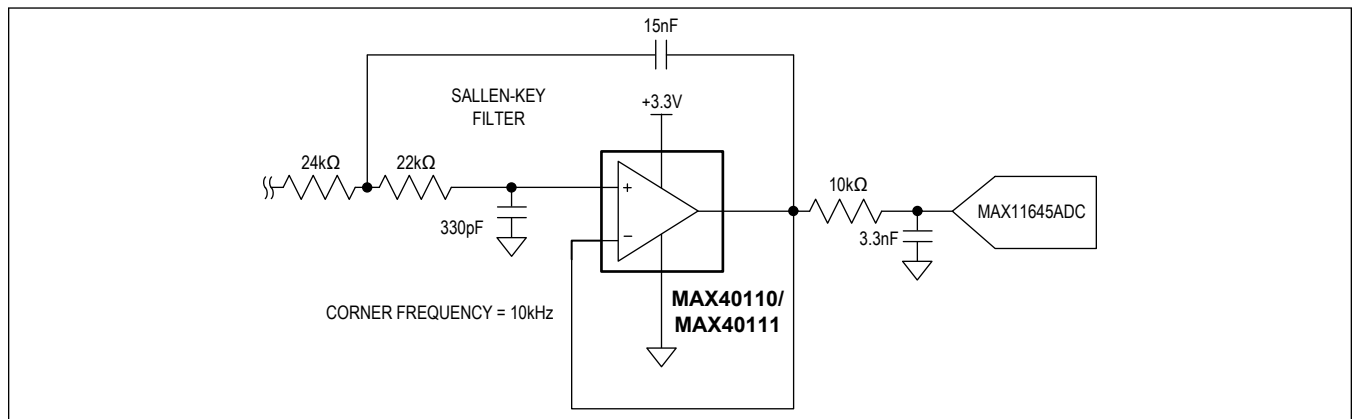


Figure 4. Typical Sallen-Key Active Filter using the MAX40110/MAX40111

**Driver for Interfacing with The MAX11645 ADC**

The MAX40110/MAX40111 tiny size and low noise make them a good fit for driving 12- to 16-bit resolution ADCs in space-constrained applications. Figure 4 shows the MAX40110/MAX40111 amplifier output connected to a lowpass filter driving the MAX11645 ADC. The MAX11645 is part of a family of 3V and 5V, 12-bit and 10-bit, 2-channel ADCs.

The MAX11645 offers sample rates up to 94ksps and measures two single-ended inputs or one differential input. These ADCs dissipate 670µA at the maximum sampling rate, but only 6µA at 1ksps and 0.5µA in shutdown. Offered in the ultra-tiny 1.9mm x 2.2mm WLP and 8-pin µMAX packages, the MAX11645 ADCs are an ideal fit to pair with the MAX40110 in portable applications. Where higher resolution is required, refer to the MAX1069 (14-bit) and MAX1169 (16-bit) ADC families.

**Ordering Information**

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX40110AYT+T	-40°C to +125°C	6 µDFN	+BC
MAX40111ANT+T	-40°C to +125°C	6 WLP	+BQ

+Denotes a lead(Pb)-free/RoHS-compliant package.

T =Tape-and-reel.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Initial Release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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