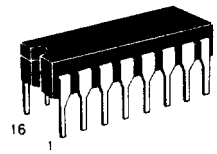
MOTOROLA

MC14500B

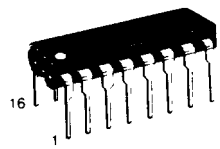
INDUSTRIAL CONTROL UNIT

The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

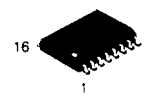
- 16 Instructions
- DC to 1.0 MHz Operation at V_{DD} = 5 V
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



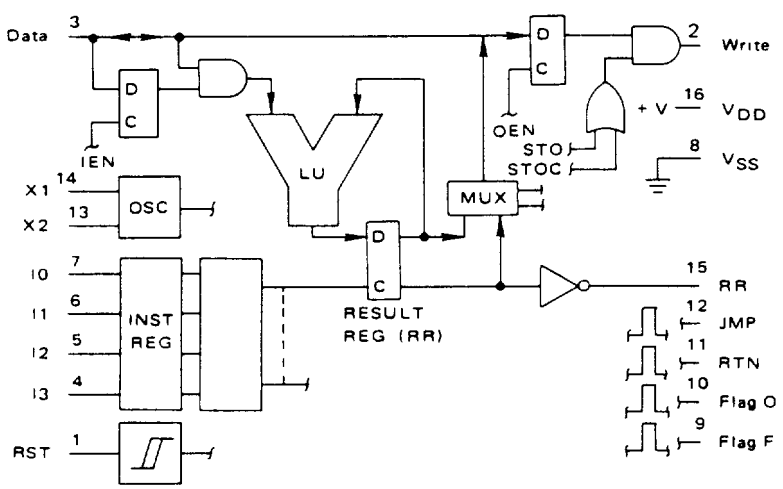
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

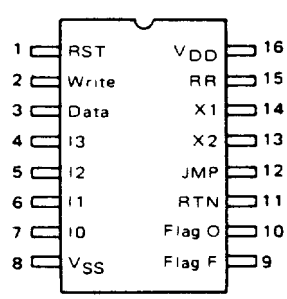
T_A = −55° to 125°C for all packages

BLOCK DIAGRAM



X1 — Oscillator Output
X2 — Oscillator Input

PIN ASSIGNMENT



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0 5 to +18 0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0 5 to V_{DD} +0 5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur

†Temperature Derating Plastic "P and D/DW" Packages −7 0 mW/°C From 65°C To 125°C
Ceramic "L" Packages −12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level										
V_{in} = V_{DD} or 0	V_{OL}	5 0	—	0 05	—	0	0 05	—	0 05	Vdc
		10	—	0 05	—	0	0 05	—	0 05	
		15	—	0 05	—	0	0 05	—	0 05	
"1" Level										
V_{in} = 0 or V_{DD}	V_{OH}	5 0	4 95	—	4 95	5 0	—	4 95	—	Vdc
		10	9 95	—	9 95	10	—	9 95	—	
		15	14 95	—	14 95	15	—	14 95	—	
Input Voltage "0" Level										
RST, D, X2										
(V_O = 4 5 or 0 5 Vdc)	V_{IL}	5 0	—	1 5	—	2 25	1 5	—	1.5	Vdc
(V_O = 9 0 or 1 0 Vdc)		10	—	3 0	—	4 50	3 0	—	3 0	
(V_O = 13 5 or 1 5 Vdc)		15	—	4 0	—	6 75	4 0	—	4 0	
"1" Level										
(V_O = 0 5 or 4 5 Vdc)	V_{IH}	5 0	3 5	—	3 5	2 75	—	3 5	—	Vdc
(V_O = 1 0 or 9 0 Vdc)		10	7 0	—	7 0	5 50	—	7.0	—	
(V_O = 1 5 or 13 5 Vdc)		15	11	—	11	8 25	—	11	—	
Input Voltage # "0" Level										
I0, I1, I2, I3										
(V_O = 4.5 or 0 5 Vdc)	V_{IL}	5 0	—	0 8	—	1 1	0 8	—	0 8	Vdc
(V_O = 9 0 or 1 0 Vdc)		10	—	1 6	—	2 2	1 6	—	1 6	
(V_O = 13 5 or 1 5 Vdc)		15	—	2 4	—	3 4	2 4	—	2 4	
"1" Level										
(V_O = 0 5 or 4 5 Vdc)	V_{IH}	5 0	2 0	—	2 0	1 9	—	2 0	—	Vdc
(V_O = 1 0 or 9 0 Vdc)		10	6 0	—	6 0	3 1	—	6 0	—	
(V_O = 1 5 or 13 5 Vdc)		15	10	—	10	4 3	—	10	—	
Output Drive Current Source										
Data, Write										
(V_{OH} = 4 6 Vdc)	I_{OH}	5 0	−1 2	—	−1 0	−2 0	—	−0 7	—	mAdc
(V_{OH} = 9 5 Vdc)		10	−3 6	—	−3 0	−6 0	—	−2 1	—	
(V_{OH} = 13 5 Vdc)		15	−7 2	—	−6 0	−12	—	−4 2	—	
(V_{OL} = 0 4 Vdc) Sink	I_{OL}	5 0	1 9	—	1 6	3 2	—	1 1	—	mAdc
(V_{OL} = 0 5 Vdc)		10	3 6	—	3 0	6 0	—	2 1	—	
(V_{OL} = 1 5 Vdc)		15	7 2	—	6 0	12	—	4 2	—	
Output Drive Current Source										
Other Outputs										
(V_{OH} = 2 5 Vdc)	I_{OH}	5 0	−3 0	—	−2 4	−4 2	—	−1 7	—	mAdc
(V_{OH} = 4 6 Vdc)		5 0	−0 64	—	−0 51	−0 88	—	−0 36	—	
(V_{OH} = 9 5 Vdc)		10	−1 6	—	−1 3	−2 25	—	−0 9	—	
(V_{OH} = 13 5 Vdc)		15	−4 2	—	−3 4	−8 8	—	−2 4	—	
(V_{OL} = 0 4 Vdc) Sink	I_{OL}	5 0	0 64	—	0 51	0 88	—	0 36	—	mAdc
(V_{OL} = 0 5 Vdc)		10	1 6	—	1 3	2 25	—	0 9	—	
(V_{OL} = 1 5 Vdc)		15	4 2	—	3 4	8 8	—	2 4	—	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Input Current, RST	I_{in}	15	25	—	—	150	—	—	250	μAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (Data)	C_{in}	—	—	—	—	15	—	—	—	pF
Input Capacitance (All Other Inputs)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I_{out} = 0 μA, V_{in} = 0 or V_{DD}	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
**Total Supply Current at an External Load Capacitance (C_L) on All Outputs	I_T	—	$I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$ $I_T = (3.0\ \mu A/kHz)\ f + I_{DD}$ $I_T = (4.5\ \mu A/kHz)\ f + I_{DD}$							μAdc

**The formulas given are for the typical characteristics only at 25°C

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SWITCHING CHARACTERISTICS (T_A = 25°C, $t_r = t_f$ = 20 ns for X and I inputs, C_L = 50 pF for JMP, X1, RR, Flag O Flag F, C_L = 130 pF + 1 TTL load for Data and Write)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Propagation Delay Time, X1 to RR	t_{PLH}, t_{PHL}	5.0	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
X1 to Flag F, Flag O, RTN, JMP		5.0	–	200	400	
		10	–	100	200	
		15	–	85	170	
X1 to Write		5.0	–	225	450	
		10	–	125	250	
		15	–	100	200	
X1 to Data		5.0	–	250	500	
		10	–	120	240	
		15	–	100	200	
RST to RR		5.0	–	250	500	
		10	–	125	250	
		15	–	100	200	
RST to X1		5.0	–	450	Note 1	
		10	–	200		
		15	–	150		
RST to Flag F, Flag O, RTN, JMP		5.0	–	400	800	
		10	–	200	400	
		15	–	150	300	
RST to Write, Data		5.0	–	450	900	
		10	–	225	450	
		15	–	175	350	
Clock Pulse Width, X1	$t_{W(cl)}$	5.0	400	200	–	ns
		10	200	100	–	
		15	180	90	–	
Reset Pulse Width, RST	$t_{W(R)}$	5.0	500	250	–	ns
		10	250	125	–	
		15	200	100	–	
Setup Time — Instruction	$t_{su(I)}$	5.0	400	200	–	ns
		10	250	125	–	
		15	180	90	–	
Data	$t_{su(D)}$	5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
Hold Time — Instruction	$t_{h(I)}$	5.0	100	0	–	ns
		10	50	0	–	
		15	50	0	–	
Data	$t_{h(D)}$	5.0	200	100	–	
		10	100	50	–	
		15	100	50	–	

NOTE 1 Maximum Reset Delay may extend to one-half clock period

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