MOTOROLA
SEMICONDUCTOR ■■■■■■■■
TECHNICAL DATA

MC44807/17

Product Preview

PLL Tuning Circuit with 3-Wire Bus

The MC44807/17 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44807/17 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC® (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3-Wire Bus) Data and Clock Inputs are I²C Bus Compatible
- ÷ 8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies Up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024
- Tri-State Phase/Frequency Comparator with Lock Detect Output
- Op Amp for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP B and Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
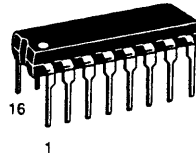- High Sensitivity
- Fully ESD Protected

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SYSTEM 4
PLL TUNING CIRCUIT
with 1.3 GHz PRESCALER
and 3-WIRE BUS

P SUFFIX
PLASTIC PACKAGE
CASE 648

16

1

PIN CONNECTIONS

	(MC44807)	
V_{tun} [1		16] Amp_{In}
V_{CC2} [2		15] Xtal
V_{CC1} [3		14] Cl
HF_{In} [4		13] Da
Gnd [5		12] En
B0 [6		11] Lock
B1 [7		10] V_{CC3}
B2 [8		9] B3

(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

16

1

PIN CONNECTIONS

	(MC44817)	
Da [1		16] En
Cl [2		15] Lock
Xtal [3		14] V_{CC3}
Amp_{In} [4		13] B3
V_{tun} [5		12] B2
V_{CC2} [6		11] B1
V_{CC1} [7		10] B0
HF_{In} [8		9] Gnd

(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

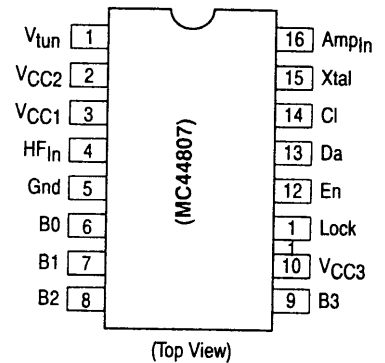| Rating	Pin(807)/(817)		Value	Unit
Power Supply Voltage (V_{CC1})	3	7	6.0	V
Band Buffer OFF Voltage	6 – 9	10 – 13	15	V
Band Buffer ON Current	6 – 9	10 – 13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	6 – 9	10 – 13	Continuous	sec
Op Amp Power Supply Voltage (V_{CC2})	2	6	40	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	5	Continuous	sec
Power Supply Voltage (V_{CC3})	10	14	14.4	V
Storage Temperature	10	14	– 65 to +150	°C
Operating Temperature Range			– 20 to + 80	°C
Band Buffer Operation (Note 1) @ 50 mA each buffer. All buffers ON simultaneously	6 – 9	10 – 13	10	sec
Op Amp Output Voltage	1	5	V_{CC2}	V

NOTES: 1. At V_{CC3} = V_{CC1} to 14.4 V, and T_A = – 20° to + 80°C.
2. At V_{CC3} = V_{CC1} to 14.4 V, and T_A = – 20° to + 80°C, one buffer ON only.

ORDERING INFORMATION

Device	Temperature Range	Package
MC44807P	– 20° to + 80°C	Plastic DIP
MC44817D		SO-16

MOTOROLA LINEAR/INTERFACE ICs DEVICE DATA

Figure 1. Ripple Rejection – Measurement Schematic (MC44807P)
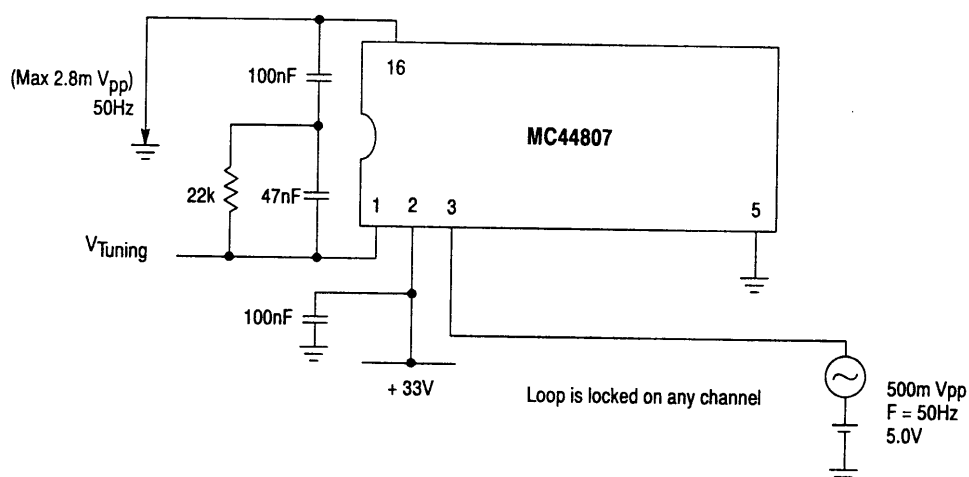
PIN FUNCTION DESCRIPTION

Pin	Function	Description
MC44807P (see Block Diagram)		
1	Out	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply (33 V)
3	V_{CC1}	Positive supply of the circuit (5.0 V)
4	HF_{In}	HF inputs from local oscillator
5	Gnd	Ground
6, 7, 8, 9	B0, B1...B3	Band buffer outputs can drive up to 30 mA (40 mA at 0° to 80° C)
10	V_{CC3}	Positive supply for integrated band buffers (12 V)
11	LOCK	Lock detector output
12	En	Enable input (3-wire Bus)
13	DA	Data input (3-wire Bus)
14	CL	Clock input (supplied by the microprocessor via 3-wire Bus)
15	Xtal	Crystal input (typ: 3.2 MHz)
16	In	Negative operational amplifier input and charge pump
MC44817D		
1	DA	Data input (3-wire Bus)
2	CL	Clock input (supplied by the microprocessor via 3-wire Bus)
3	Xtal	Crystal oscillator (3.2 MHz)
4	In	Negative operational amplifier input and charge pump
5	Out	Operational amplifier output which provides the tuning voltage
6	V_{CC2}	Operational amplifier positive supply (33 V)
7	V_{CC1}	Positive supply of the circuit (5.0 V)
8	HF_{In}	HF input from local oscillator
9	Gnd	Ground
10, 11, 12, 13	B0, B1...B3	Band buffer outputs can drive up to 30 mA (40 mA at 0° to 80°C)
14	V_{CC3}	Positive supply for integrated band buffers (12 V)
15	LOCK	Lock detector output
16	En	Enable input (3-wire Bus)

Figure 2. HF Sensitivity Test Circuit

Device is in Test mode: Sensitivity is level of
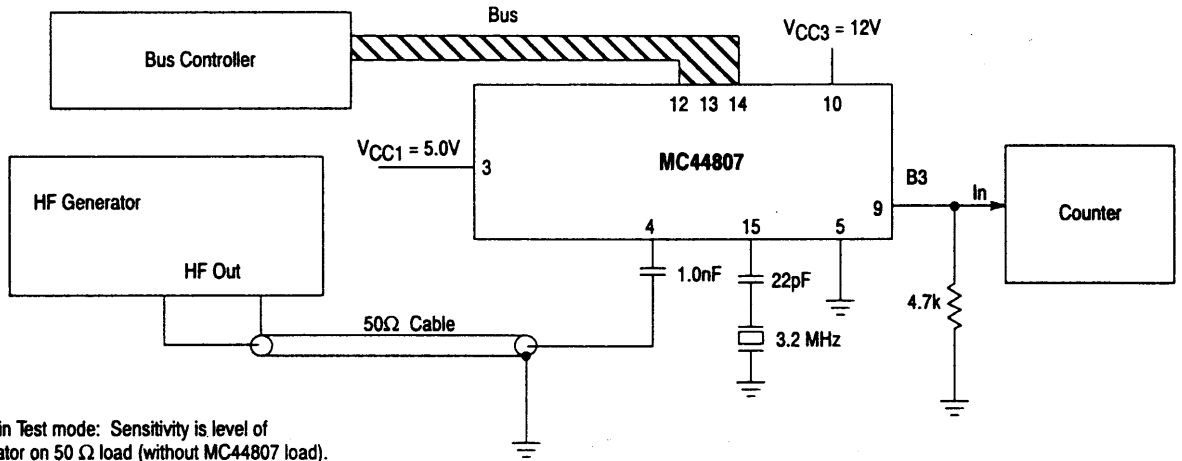HF generator on 50 Ω load (without MC44807 load).
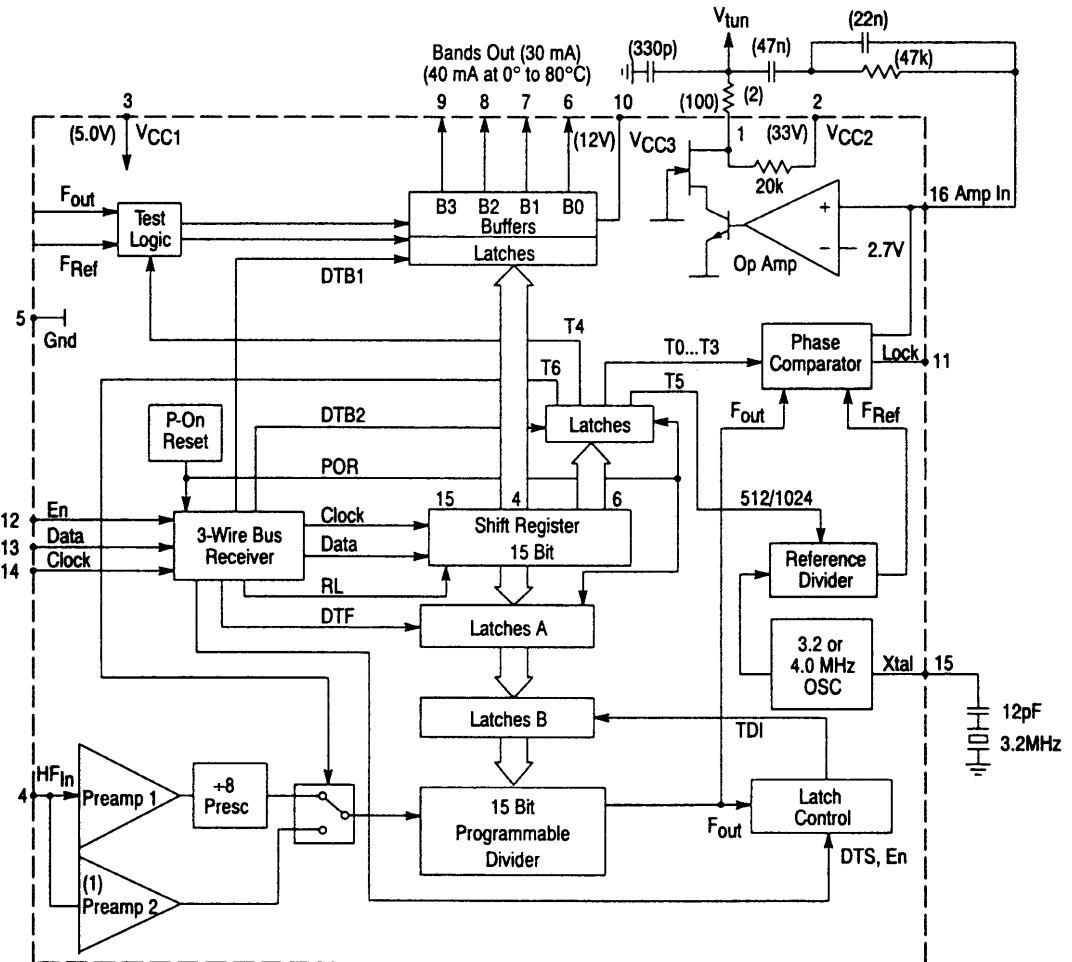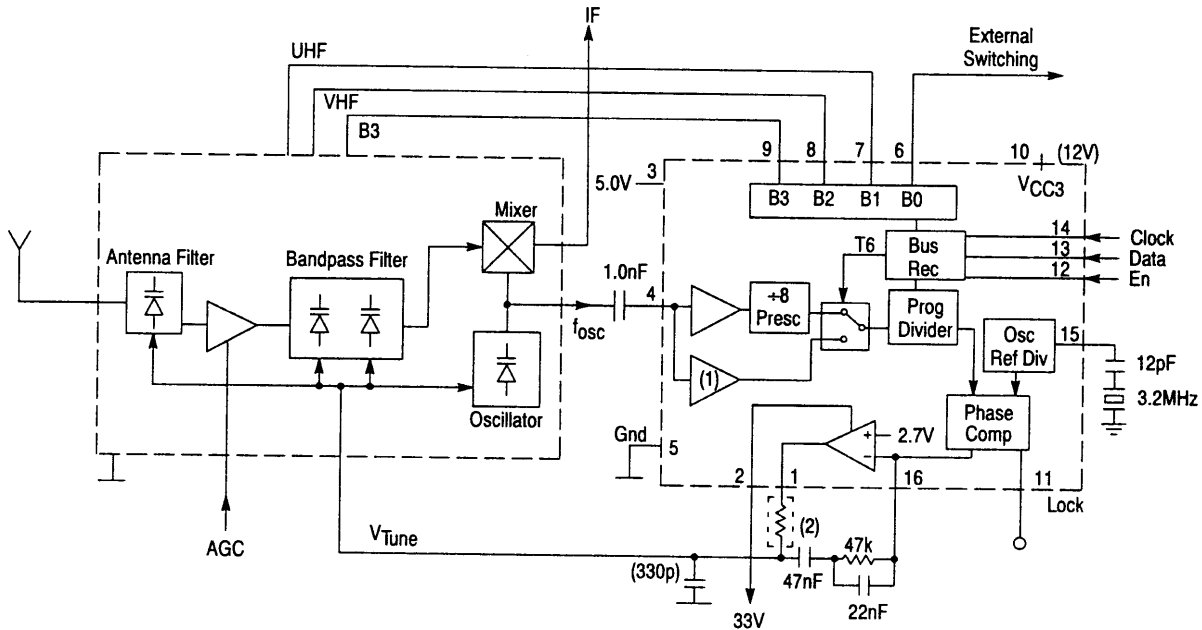
Figure 3. Block Diagram MC44807P

Figure 4. Typical Tuner Application

NOTE: 1. This feature needs to be characterized on the final silicon. In the case that it degrades the HF-sensitivity, it will be eliminated.
2. The 100 Ω resistor is not required any more, but does not disturb the performance.

FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A brief discussion of the features and function of each of the internal blocks follows.

Data Format and Bus Receiver

The circuit is controlled by a 3-wire bus with Data (DA), Clock (CL), and Enable (En) inputs. The Data and Clock inputs may also be shared with an I2C Bus (data changes when clock is low) while the Enable is a separate signal. The circuit is compatible with 18 and 19-bit data transmission and also has a mode for 34-bit transmission for test and additional features.

The 3-wire bus receiver receives data for the internal shift register after the positive-going edge of the En signal. The data is transmitted to the band buffers on the negative-going edge of clock pulse 4 (signal DTB1).

18 and 19-Bit Data Transmission

The programmable divider may receive 14-bit (18-bit transmission) or 15-bit (19-bit transmission). The data is transmitted to the programmable divider (Latches A) on the negative-going edge of clock pulse 19 or on the negative edge of the En signal if En goes down after the 18th clock pulse (signal DTF). If the programmable divider receives

14-bit, its MSB (Bit N14) is internally reset. The reset pulse is generated only if En goes negative after the 18th clock pulse (signal RL).

34-Bit Data Transmission

(For Test and Additional Features) In the test mode, the programmable divider receives 15-bit and the data is transferred to Latches A on the negative edge of clock pulse 19 (signal DTF). The information for test is received on clock pulses 20 to 26 and transmitted to the latches on the negative edge of pulse 34 (signal DTB2). These latches have a power-on reset. The power-on reset sets the programmable divider to a counting ratio of 256 or higher and resets the corresponding latches to test bits T0 to T6 (signal POR). The bus receiver is not disturbed if the data format is wrong. Useless bits are ignored. If, for example, the Enable signal goes low after clock pulse 9, bits 1 to 4 are accepted as valid buffer information and the other bits are ignored. If more than 34 bits are received, bit 35 and the following are ignored.

The Lock Detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.
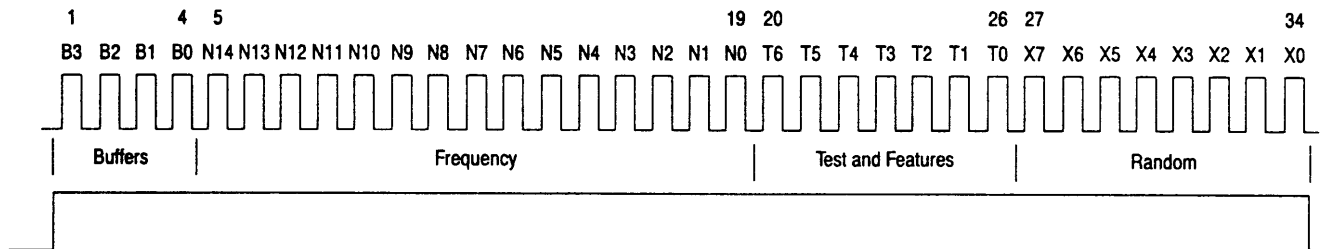
BUS TIMING DIAGRAM

Standard Bus Protocol 18 or 19-Bit
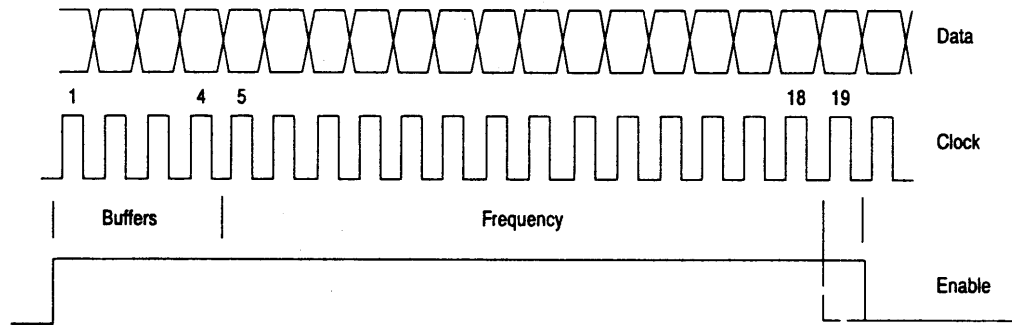
Bus Protocol for Test and Features

DEFINITION OF BUS PROTOCOLS

Bus Protocol for 18-Bit

B3	B2	B1	B0	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Max counting ratio 16363
  N14 is reset internally

Bus Protocol for 19-Bit

B3	B2	B1	B0	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Max counting ratio 32767:
  B0, B1...B3 = Control of band buffers
  N0, N1...N14 = Control of programmable divider

N14 = MSB; N0 = LSB
Min, counting ratio always 17.
B3 = First shifted bit
N0 = Last shifted bit

Bus Protocol for Test and Further Features (34-Bit)

B3	B2	B1	B0	N14...N0	T6	T5	T4	T3	T2	T1	T0	X7	X6...X1	X0

T0, T1...T3 = Control the phase comparator
         T4 = Switches test signals to the buffer outputs
         T5 = Division ratio of the reference divider
         T6 = Bypasses the prescaler (see note Bit T6 table)
X0, X1...X7 = Are random

B3 = First shifted bit
X0 = Last shifted bit

DEFINITION OF THE BITS FOR TEST AND FEATURES

Bit T0 Defines the Charge Pump Current of the Phase Comparator

T0	Charge
0	Pump current 50 μA (Typical)
1	Pump current 15 μA (Typical)

Bits T1 and T2 Define the Digital Function of the Phase Comparator

T2	T1	State	Output Function of Phase Comparator
0	0	1	Normal Operation
0	1	2	High Impedance (Tri-State)
1	0	3	Upper Source On, Lower Source Off
1	1	4	Lower Source On, Upper Source Off

NOTE: State 1 The phase comparator pulls high if the input frequency is too high and it pulls low when the input frequency is too low. (Inversion by op amp) The phase comparator generates a fixed duration offset pulse for each comparison pulse (similar to the MC44802A). This guarantees operation in the linear region. The offset pulse is a positive current pulse (upper source).

Bit T3 Defines the Offset Pulse of the Phase Comparator

T3	Offset Pulse
0	Offset pulse short (200 ns), normal mode
1	Offset pulse long (350 ns)

Bit T4 Switches the Internal Frequencies F_{ref} and FBY2 to the Buffer Outputs (B2, B3)

T4	Buffer Outputs
0	Normal operation
1	F_{Ref} switched to buffer output B2 FBY2 switched to buffer output B3

Bits B2 and B3 = have to be one in this case
F_{Ref} = reference frequency
FBY2 = output frequency of the Programmable Divider, ÷ 2

Bit T5 Defines the Division Ratio of the Reference Divider

T5	Bus Protocol
0	Division ratio 512
1	Division ratio 1024

The division ratio of the Reference Divider can only be programmed in the 34 bit bus protocol. In the standard bus protocol the division ratio is 512. (The power-up reset (POR) sets the division ratio to 512).

Bit T6 Switches the Prescaler

T6	Operation
0	Normal operation, 1.3 GHz Preamp 2 switched OFF
1	Low frequency operation, 165 MHz maximum. The prescaler is bypassed and its power supply is switched OFF. Input, 10 MHz min, 20 mVrms min.

NOTE: This feature needs to be characterized on the final silicon. In the case that it degrades the HF-sensitivity, it will be eliminated.

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Figure 7. Equivalent Circuit of the Integrated Band Buffers

$I_b + I_{sub}$ = 8.0 mA typ, 13 mA max
I_b = Base Current
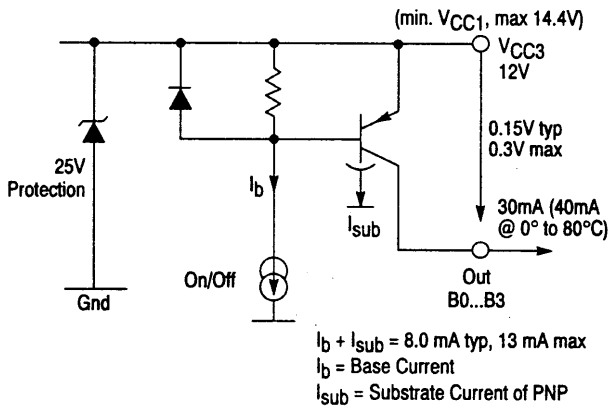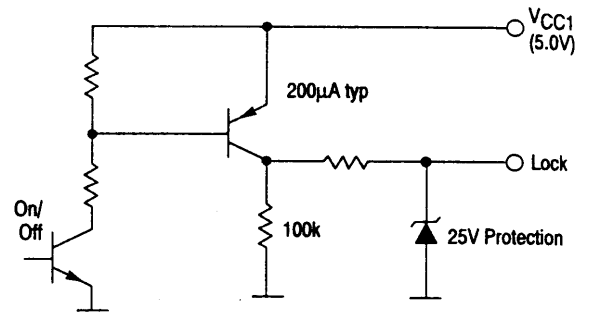I_{sub} = Substrate Current of PNP

Figure 8. Equivalent Circuit of the Lock Output

Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the Latches B. Latches B are loaded from Latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since Latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$$N = 16384 \times N14 + 8132 \times N13 + ... + 4 \times N2 + 2 \times N1 + N0$$

maximum ratio 32767 (16363 in case of 18-bit protocol), minimum ratio 17, where N0...N14 are the different bits for frequency information.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 4 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

Oscillator

The oscillator uses a 3.2 MHz to 4.0 MHz crystal tied to ground in series with a capacitor, used in the series resonance mode. The voltage at Pin 15 (or Pin 3 in SOIC package) "crystal", has low amplitude and low harmonic distortion.

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