Product/process change notification

PCN213001

Dear

GENERAL INBOX
PREMIER FARNELL
ProductChangeNotices@premierfarnell.com

Please find attached our Infineon Technologies AG PCN:

2Gb QSPI Semper Flash Rev *C Silicon Qualification and Datasheet changes

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before **09 Sep 2021**
- Infineon aligns with the widely-recognized JEDEC STANDARD **"JESD46",** which stipulates:
  "Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."

  Notwithstanding the aforesaid individual agreements shall prevail

Your prompt reply will help Infineon Technologies to assure a smooth and well executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance.
For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

Cypress Semiconductor Corporation – An Infineon Technologies Company
198 Champion Court, San Jose, CA 95134. Tel: (408) 943-2600

▶ Products affected:

Please refer to attached affected product list [18]

▶ Detailed change information:

Subject: Qualification of Rev *C Silicon for 2Gb QSPI Semper Flash family and related datasheet changes

Reason: Rev *C silicon fixes the errata impacting 2Gb QSPI Semper Flash products on Rev *A silicon

Description:

Old	New
■ Errata impacts Rev *A silicon ○ Continuous Read across lower addressed Die to upper address Die boundary fails during DDR Reads in protocol modes 1S-4D-4D and 4S-4D-4D using commands (EDh, EEh)	■ Qualified a metal fix (Rev *C) to address the Continuous Read across die boundary read failure errata
■ Errata impacts Rev *A silicon ○ Continuous Read across lower addressed Die to upper address Die boundary fails during SDR reads (1S-1S-1S) and (1S-1S-4S) without Latency Cycles and Mode Bits using commands (03h, 13h, 0Bh, 6Bh, 6Ch)	■ Qualified a metal fix (Rev *C) to address the Continuous Read across die boundary read failure
■ Rev *A silicon parameters: No change	■ Rev *C silicon parameters: Changes in following specifications ○ Standby Current (I_{SB}) ○ DPD Current (I_{DPD}) ○ Refer attachment 2GbSemper_SpecChanges.xlsx

▶ Product identification:

Marking Die Code will be used to differentiate the silicon revision:

Device	OLD (Rev *A)	NEW (Rev *C)
2Gb QSPI Non-Auto (Non-PBO/PBO) Temp: I, V	Die Code “A”	Die Code “C” or “D”
2Gb QSPI Auto (PBO) Temp: A, B, M	Die Code “B”	Die Code “D”

▶ Impact of change:

Quality and reliability verified by qualification. There is no change in form, fit and function (except for the logic fix and electrical parameter change identified in the table above). No other impact on electrical performance.

▶ Attachments:

Affected product list [18]

Supporting documents

▶ Time schedule:

■ Final qualification report:	Available
■ First samples available:	On request (LT 4 – 6 weeks)
■ Intended start of delivery:	Custom MPNs/PPAP: Upon customer approval Standard MPNs: 90 days from PCN date

If you have any questions, please do not hesitate to contact your local sales office.

Device	Symbol	Parameter	Test Conditions	OLD (Rev *A) Max	NEW (Rev *C) Max	Unit
S25HS02GT	I_{SB}	Standby Current (HS-T)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}; 105°C	400	450	µA
S25HS02GT	I_{SB}	Standby Current (HS-T)	RESET#, CS# = VCC; All I/Os = VCC or VSS; 125°C	870	1000	µA
S25HL02GT	I_{SB}	Standby Current (HL-T)	RESET#, CS# = VCC; All I/Os = VCC or VSS; 125°C	790	1000	µA
S25HS02GT	I_{DPD}	Current (HS-T)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}; 105°C	40	45	µA
S25HS02GT	I_{DPD}	Current (HS-T)	RESET#, CS# = VCC; All I/Os = VCC or VSS; 125°C	85	110	µA
S25HL02GT	I_{DPD}	Current (HL-T)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}; 105°C	41	45	µA
S25HL02GT	I_{DPD}	Current (HL-T)	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}; 125°C	60	110	µA