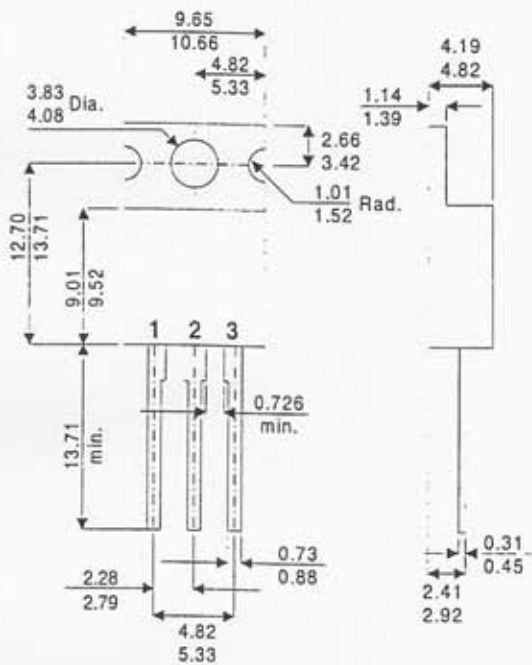


MECHANICAL DATA
Dimensions in mm



**SILICON EPITAXIAL BASE
NPN POWER TRANSISTORS**

NPN Transistors in a plastic TO-220 package.

With their PNP complements BD950 ; 952 ; 954 and 956 they are intended for use in a wide range of power amplifiers and for switching applications.

TO-220AB TO220 Plastic Package

Pin 1 – Base Pin 2 – Collector Pin 3 – Emitter

Collector connected to Mounting Base.

ABSOLUTE MAXIMUM RATINGS

($T_{case} = 25^{\circ}C$ unless otherwise stated)

		BD949	BD951	BD953	BD955
V_{CBO}	Collector – Base Voltage	60V	80V	100V	120V
V_{CEO}	Collector – Emitter Voltage	60V	80V	100V	120V
V_{EBO}	Emitter – Base Voltage		5V		
I_C	Collector Current		5A		
I_{CM}	Peak Collector Current		8A		
P_{tot}	Total Power Dissipation		40W		
T_{stg}	Storage Temperature Range		-65 to 150°C		
T_J	Maximum Junction Temperature		150°C		

$T_{amb} \leq 25^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BE}^* Base - Emitter Voltage ¹	$I_C = 2A$ $V_{CE} = 4V$			1.4	V
$V_{CE(sat)}^*$ Collector - Emitter Saturation Voltage	$I_C = 2A$ $I_B = 0.2A$			1	V
I_{CBO} Collector Cut-off Current	$I_E = 0$ $V_{CB} = V_{CBO(MAX)}$			0.1	mA
	$I_E = 0$ $V_{CB} = \frac{1}{2}V_{CBO(MAX)}$ $T_J = 150^{\circ}C$			2	
	$I_B = 0$ $V_{CE} = \frac{1}{2}V_{CEO(MAX)}$			0.5	
I_{EBO} Emitter Cut-off Current	$I_C = 0$ $V_{EB} = 5V$			1	mA
h_{FE}^* DC Current Gain	$I_C = 0.5A$ $V_{CE} = 4V$	40			—
	$I_C = 2A$ $V_{CE} = 4V$	20			
f_T Transition Frequency	$I_C = 0.5A$ $V_{CE} = 4V$ $f = 1MHz$	3			MHz
t_{ON} Turn-on Time	$I_{C(ON)} = 1A$ $I_{B(ON)} = -I_{B(OFF)} = 0.1A$		0.3		μs
t_{OFF} Turn-off Time			1.5		

* Pulse Test: $t_p \leq 300\mu s$, $\delta < 2\%$

Note 1 V_{EB} decreases by about 2.3mV/K with increasing temperature.

THERMAL CHARACTERISTICS

$R_{\theta J-MB}$ Thermal Resistance Junction to Mounting Base			3.12	K/W
$R_{\theta JA}$ Thermal Resistance Junction to Ambient			70	K/W

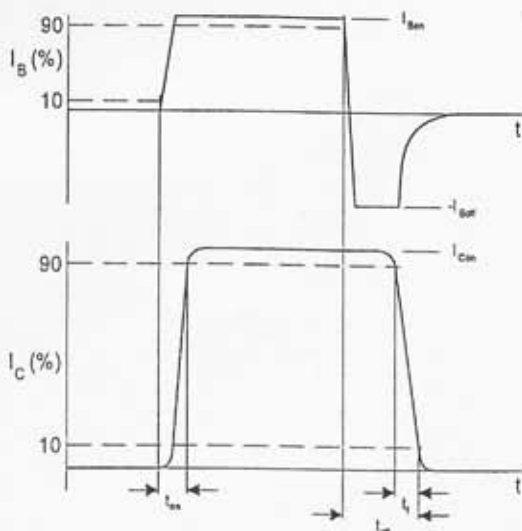


Fig. 1 Switching times waveforms.

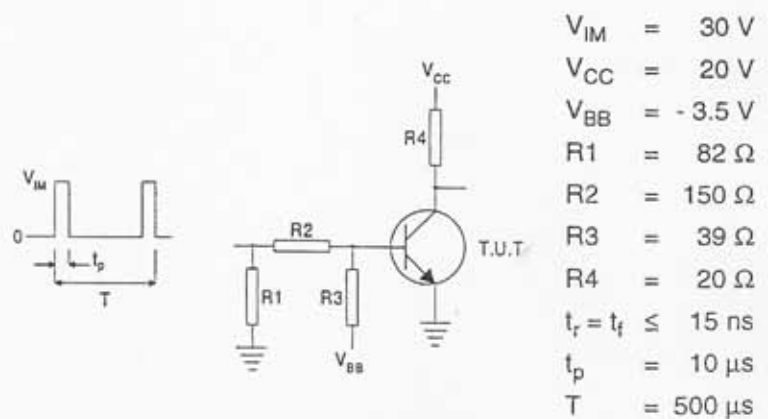


Fig. 2 Switching times test circuit.