Product Change Notification / SYST-15MAVS007

Date:

17-Sep-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATtiny87/167 Automotive Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-15MAVS007_Affected_CPN_09172021.pdf
SYST-15MAVS007_Affected_CPN_09172021.csv

Notification Text:

SYST-15MAVS007

Microchip has released a new Product Documents for the ATtiny87/167 Automotive Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at ATtiny87/ 167 Automotive Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Initial release of this document.

1. Errata content moved from the data sheet and restructured to the new document template
2. Data sheet clarifications added:
   - 3.1 Errata Section in Data Sheet is no Longer Valid
   - Interrupts: 3.2.1 Interrupt Vectors in ATtiny87/167 Automotive
   - LIN/UART: 3.3.1 Baud Rate Generator
   - Package Marking: 3.4 Package Marking Information

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 September 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny87/ 167 Automotive Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

ATTINY87-XU
ATTINY87-SU
ATTINY87-MU
ATTINY87-A15XD
ATTINY87-A15MD-VAO
ATTINY87-XUR
ATTINY87-SUR
ATTINY87-MUR
ATTINY87-A15XZ
ATTINY87-A15SZ
ATTINY87-A15MZ
ATTINY167-W-NG
ATTINY167-XU
ATTINY167-SU
ATTINY167-MU
ATTINY167-MMU
ATTINY167-A15XD
ATTINY167-A15MD
ATTINY167-XUR
ATTINY167-SUR
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ATTINY167-MMUR
ATTINY167-MMURB20
ATTINY167-A15XZ
ATTINY167-A15SZ
ATTINY167-A15MZ
ATTINY167-A15MZ-V01
ATTINY167-A15MZ-V02
ATTINY167-A15MZ-V03

ATtiny87/167 Automotive

Automotive Silicon Errata and Data Sheet Clarifications

Introduction

The ATtiny87/167 Automotive devices you have received conform functionally to the current device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en590544), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny87/167 Automotive devices.

Note:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous and current.

1. Silicon Issue Summary

Legend

-	Erratum is not applicable.
X	Erratum is applicable.

Errata Overview

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A	Rev. B	Rev. C
		Date Code > 1207	Date Code > 1208	
System Clock and Clock Options	2.2.1 Gain Control of the Crystal Oscillator	X	X	X
	2.2.2 “Disable Clock Source” Command Remains Enabled	X	X	X
LIN-UART	2.3.1 CRC Calculation of Diagnostic Frames in LIN 2.x	X	-	-
	2.3.2 LIN Break Delimiter	X	X	-
ADC	2.4.1 Comparison Between ADC Inputs and Voltage References	X	-	-
	2.4.2 Register Bits of DIDR1	X	-	-

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 System Clock and Clock Options

2.2.1 Gain Control of the Crystal Oscillator

The crystal oscillator (0.4 → 16 MHz) doesn't latch its gain control (CKSEL/CSEL[2..0] bits):

1. The 'recover system clock source' command doesn't return CSEL[2..0] bits.
2. The gain control can be modified on the fly if CLKSELR changes.

Work Around

1. No work around.
2. As soon as possible, after any CLKSELR modification, re-write the appropriate crystal oscillator setting (CSEL[3]=1 and CSEL[2..0] / CSUT[1..0] bits) in CLKSELR.

Code example:

```
; Select crystal oscillator (16MHz crystal, fast rising power)
        ldi     temp1,((0x0F<<CSEL0)|(0x02<<CSUT0))
        sts     CLKSELR, temp1
; Enable clock source (crystal oscillator)
        ldi     temp2,(1<<CLKCCE)
        ldi     temp3,(0x02<<CLKC0)     ; CSEL = "0010"
        sts     CLKCSR,temp2            ; Enable CLKCSR register access
        sts     CLKCSR,temp3            ; Enable crystal oscillator clock
; Clock source switch
        ldi     temp3,(0x04<<CLKC0)     ; CSEL = "0100"
        sts     CLKCSR,temp2            ; Enable CLKCSR register access
        sts     CLKCSR,temp3            ; Clock source switch
; Select watchdog clock (128KHz, fast rising power)
        ldi     temp3,((0x03<<CSEL0)|(0x02<<CSUT0))
        sts     CLKSELR, temp3          ; (*)
; (*) !!! Loose gain control of crystal oscillator !!!
; ==> WORKAROUND ...
        sts     CLKSELR, temp1
;  ...
```

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.2.2 "Disable Clock Source" Command Remains Enabled

In the dynamic clock switch module, the 'disable clock source' command remains running after disabling the targeted clock source (the clock source is set in the CLKSELR register).

Work Around

After a 'disable clock source' command, reset the CLKCSR register by writing `0x80`.

Code example:

```
; Select crystal oscillator
        ldi temp1,(0x0F<<CSEL0)
        sts CLKSELR, temp1
; Disable clock source (crystal oscillator)
        ldi temp2,(1<<CLKCCE)
        ldi temp3,(0x01<<CLKC0) ; CSEL = "0001"
        sts CLKCSR,temp2 ; Enable CLKCSR register access
        sts CLKCSR,temp3 ; (*) Disable crystal oscillator clock
; (*) !!! At this moment, if any other clock source is selected by CLKSELR,
; this clock source will also stop !!!
; ==> WORKAROUND ...
        sts CLKCSR,temp2
```

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

2.3 LIN-UAT

2.3.1 CRC Calculation of Diagnostic Frames in LIN 2.x

Diagnostic frames of LIN 2.x use “classic checksum” calculation. Unfortunately, the setting of the checksum mode is enabled when the HEADER is transmitted/received. Usually, in LIN 2.x, the LIN/UART controller is initialized to process “enhanced checksums”. A slave task does not know what kind of frame it will work on before checking the ID.

Work Around

This work around is to be implemented only in the case of transmission/reception of diagnostic frames.

1. Slave task of master node: Before enabling the HEADER, the master must set the appropriate LIN13 bit value in the LINCR register.
2. For slave nodes, the work around is in two parts:
   a. Before enabling the RESPONSE, use the following function:

```
        void lin_wa_head(void) {
unsigned char temp;
temp = LINBTR;
LINCR = 0x00; // It is not a RESET !
LINBTR = (1<<LDISR)|temp;
LINCR = (1<<LIN13)|(1<<LENA)|(0<<LCMD2)|(0<<LCMD1)|(0<<LCMD0);
LINDLR = 0x88; // If it isn't already done
}
```

   b. Once the RESPONSE is received or sent (having RxOK or TxOK as well as LERR), use the following function:

```
        void lin_wa_tail(void) {
LINCR = 0x00; // It is not a RESET !
LINBTR = 0x00;
LINCR = (0<<LIN13)|(1<<LENA)|(0<<LCMD2)|(0<<LCMD1)|(0<<LCMD0);
}
```

The time-out counter is disabled during the RESPONSE when this work around is set.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C

X	-	-

2.3.2 LIN Break Delimiter

In SLAVE MODE, a BREAK field detection error can occur under the following conditions.

The problem occurs if two conditions occur simultaneously:

1. The DOMINANT part of the BREAK is (N+0.5)*Tbit long with N=13, 14,15, ...
2. The RECESSIVE part of the BREAK (BREAK DELIMITER) is equal to 1*Tbit. (See the note below).

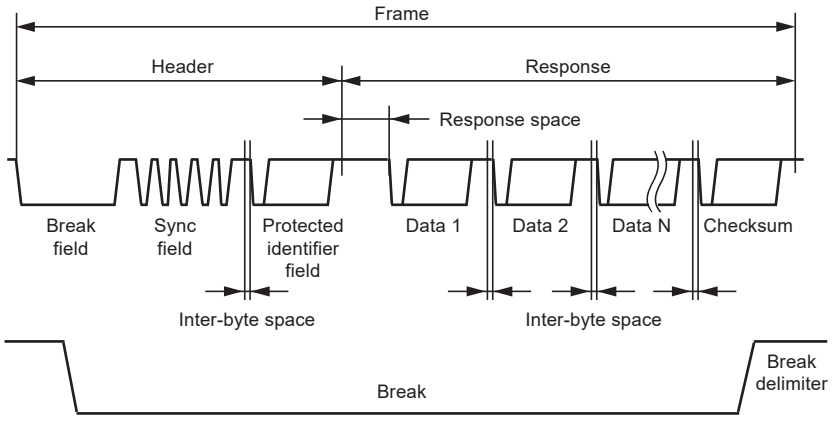
The BREAK_high is not detected, and the 2nd bit of the SYNC field is interpreted as the BREAK DELIMITER. The error is detected as a framing error on the first bits of the PID or subsequent Data or a Checksum error.

There is no error if BREAK_high is greater than 1 x Tbit + 18%.

There is no problem in Master mode.

Note: LIN2.1 protocol specification paragraph 2.3.1.1 Break field says (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en590544): “A break field is always generated by the master task (in the master node) and it shall be at least 13 nominal bit times of dominant value, followed by a break delimiter, as shown in Figure 2-1. The break delimiter shall be at least one nominal bit time long.”

Figure 2-1. The Break Field



Work Around

None

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	-

2.4 ADC

2.4.1 Comparison Between ADC Inputs and Voltage References

In the analog comparator module, comparing any ADC input (ADC[10..0]) with voltage references (2.56V, 1.28V, 1.10V, 0.64V or 0.32V) fails.

Regardless, AIN1 input can be compared with the voltage references, and any ADC input can be compared with the AIN0 input.

Work Around
Do not use this configuration.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

2.4.2 Register Bits of DIDR1

ADC8D, ADC9D and ADC10D (digital input disable) initially located at bit 4 up to 6 are instead located at bit 0 up to 2. These register bits are also in write-only mode.

Work Around
Allow for the change in bit locations and the access mode restriction.

Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en590544).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Errata Section in Data Sheet is no Longer Valid

A clarification for the Errata section in the device data sheet has been made.

The errata content has been moved to a separate document, *ATtiny87/167 Automotive Silicon Errata and Data Sheet Clarifications* (this document).

For the latest errata, see the *Silicon Errata Issues* section of this document.

3.2 Interrupts

3.2.1 Interrupt Vectors in ATtiny87/167 Automotive

A clarification for the source names of the Interrupt vectors has been made to comply with the header file naming convention.

Table 3-1. Reset and Interrupt Vectors in ATtiny87/167 Automotive

Vector Nb.	Program Address		Source	Interrupt Definition
	ATtiny87	ATtiny167		
1	0x0000	0x0000	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0001	0x0002	INT0	External Interrupt Request 0
3	0x0002	0x0004	INT1	External Interrupt Request 1
4	0x0003	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0004	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x0005	0x000A	WDT	Watchdog Time-out Interrupt
7	0x0006	0x000C	**TIMER1_CAPT**	Timer/Counter1 Capture Event
8	0x0007	0x000E	**TIMER1_COMPA**	Timer/Counter1 Compare Match A
9	0x0008	0x0010	**TIMER1_COMPB**	Timer/Counter1 Compare Match B
10	0x0009	0x0012	**TIMER1_OVF**	Timer/Counter1 Overflow
11	0x000A	0x0014	**TIMER0_COMPA**	Timer/Counter0 Compare Match A
12	0x000B	0x0016	**TIMER0_OVF**	Timer/Counter0 Overflow
13	0x000C	0x0018	**LIN_TC**	LIN/UART Transfer Complete
14	0x000D	0x001A	**LIN_ERR**	LIN/UART Error
15	0x000E	0x001C	**SPI_STC**	SPI Serial Transfer Complete
16	0x000F	0x001E	ADC	ADC Conversion Complete
17	0x0010	0x0020	**EE_READY**	EEPROM Ready
18	0x0011	0x0022	**ANA_COMP**	Analog Comparator

.....continued				
Vector Nb.	Program Address		Source	Interrupt Definition
	ATtiny87	ATtiny167		
19	0x0012	0x0024	**USI_START**	USI Start Condition Detection
20	0x0013	0x0026	**USI_OVF**	USI Counter Overflow

3.3 LIN/UART - Local Interconnect Network Controller or UART

3.3.1 Baud Rate Generator

A clarification has been made for the equations in the Baud Rate Generator section.

The baud rate is defined to be the transfer rate in bits per second (bps):

- BAUD: Baud rate (in bps)
- $fclk_{i/o}$: System I/O clock frequency
- LDIV[11..0]: Contents of LINBRRH & LINBRRL registers - (0-4095), the pre-scaler receives $clk_{i/o}$ as input clock
- LBT[5..0]: Least significant bits of - LINBTR register- (0-63) is the number of samplings in a LIN or UART bit (default value 32)

Equation for calculating baud rate:
$BAUD = fclk_{i/o} / (LBT[5..0] \times (LDIV[11..0] + 1))$

Equation for setting LINDIV value:
$LDIV[11..0] = (fclk_{i/o} / (LBT[5..0] \times BAUD)) - 1$

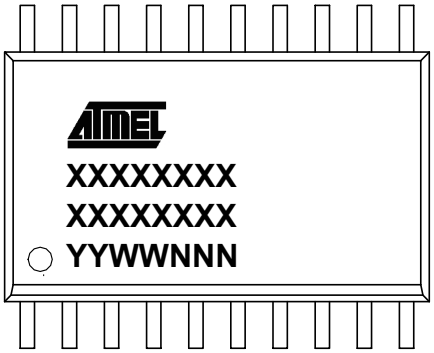
Note that in reception, a majority vote on three samplings is made.

3.4 Package Marking Information

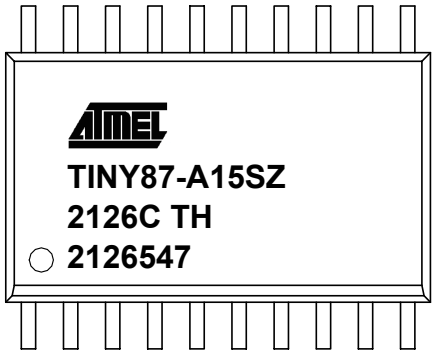
Legend:	XX...X	Customer-specific information or Microchip part number
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

3.4.1 20-Pin SOIC

General

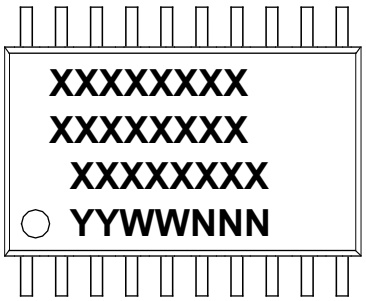


Example

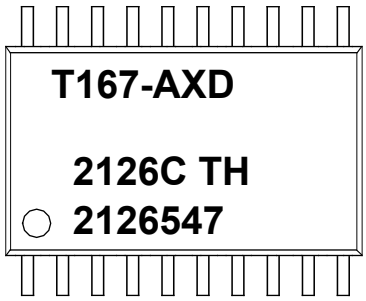


3.4.2 20-Pin TSSOP

General

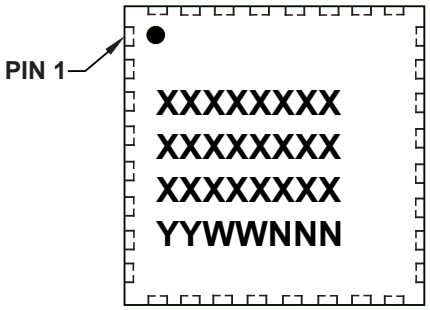


Example

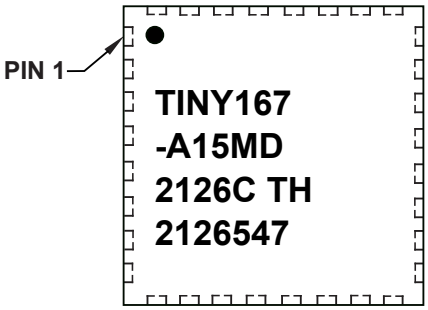


3.4.3 32-Pin VQFN

General



Example



4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	09/2021	Initial release of this document • Errata content moved from the data sheet and restructured to the new document template • Data sheet clarifications added: – 3.1 Errata Section in Data Sheet is no Longer Valid – Interrupts: 3.2.1 Interrupt Vectors in ATtiny87/167 Automotive – LIN/UART: 3.3.1 Baud Rate Generator – Package Marking: 3.4 Package Marking Information

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