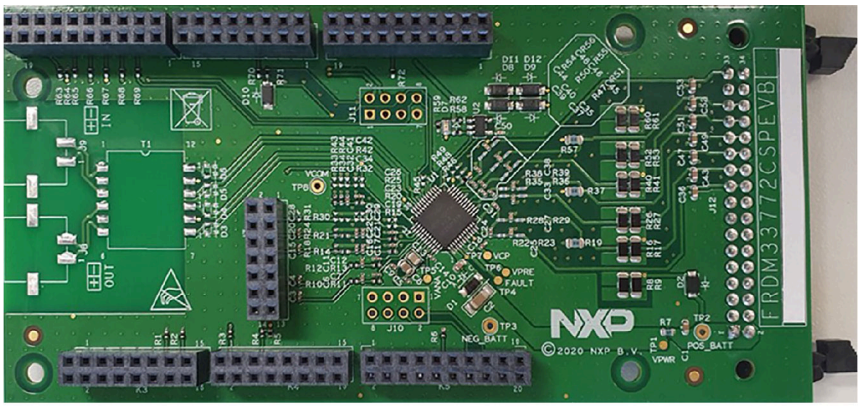
UM11561

FRDM33772CSPEVB user manual

Rev. 1 — 4 March 2021 User manual

1 FRDM33772CSPEVB



aaa-040758

Figure 1. FRDM33772CSPEVB

2 Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Typical parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including Typical, must be validated for each customer application by customer’s technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part.

3 Getting started

The NXP analog product development boards provide a platform for evaluating a broad range of NXP analog, mixed-signal, and power solution products. NXP analog product development boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer a long battery life, a small form factor, reduced component counts, low cost, and improved performance in powering state-of-the-art systems.

The tool summary page for the FRDM33772CSPEVB evaluation board is at http://www.nxp.com/FRDM33772CSPEVB. The tool summary page provides information related to using the evaluation board. The page contains the following sections:

- Overview – A brief summary of the evaluation board and its capabilities
- Supported devices – A list of devices that the evaluation board supports
- Specifications – An overview of the technical and functional specifications for the board
- Documents and software/design resources – All of the information and resources required by users who have already purchased the FRDM33772CSPEVB. This section includes:
  - Design tools & files – Click the download button to download the board bill of materials and the Gerber files for the PCB assemblies.
  - Printed circuit boards and schematics – Click the download button to download a .pdf version of the FRDM33772CSPEVB board schematics.

The get started link in the upper left of the menu bar provides information applicable to using the FRDM33772CSPEVB.

3.1 Kit contents/packing list

The kit contents include:

- Assembled and tested evaluation board/module in anti-static bag
- Quick-start guide

3.2 Required equipment

To use this evaluation board, you need:

- A 3-cell to 6-cell battery pack, such as BATT-14AAAPACK, or a battery pack emulator, such as BATT-6EMULATOR

4 Getting to know the hardware

4.1 Board overview

The FRDM33772CSPEVB serves as a hardware evaluation tool in support of the MC33772C device of NXP. The MC33772C is a battery cell controller that monitors up to 6 lithium-ion battery cells. It is designed for use in both automotive and industrial applications. The device performs analog-to-digital conversions on differential cell voltages and currents. It is also capable of battery charge coulomb counting and battery temperature measurements. The FRDM33772CSPEVB is an ideal platform for rapid prototyping of MC33772C based applications that involve current, voltage, and temperature sensing.

The FRDM33772CSPEVB supports a standard serial peripheral interface (SPI). The information is digitally transmitted to a microcontroller for processing.

4.2 Board features

The main features of FRDM33772CSPEVB are:

- Standard SPI communication
- LED indicator for operation mode
- Cell-balancing resistors
- Cell sense input with RC filter
- General-purpose input/output (GPIO): digital I/O, wake-up inputs, convert trigger inputs, ratiometric analog inputs, analog inputs with absolute measurements
- EEPROM (connected to the IC with I^2C-bus interface) to store user-defined calibration parameters
- Fault detection pin report
- Current measurement input via external shunt

4.3 Block diagram

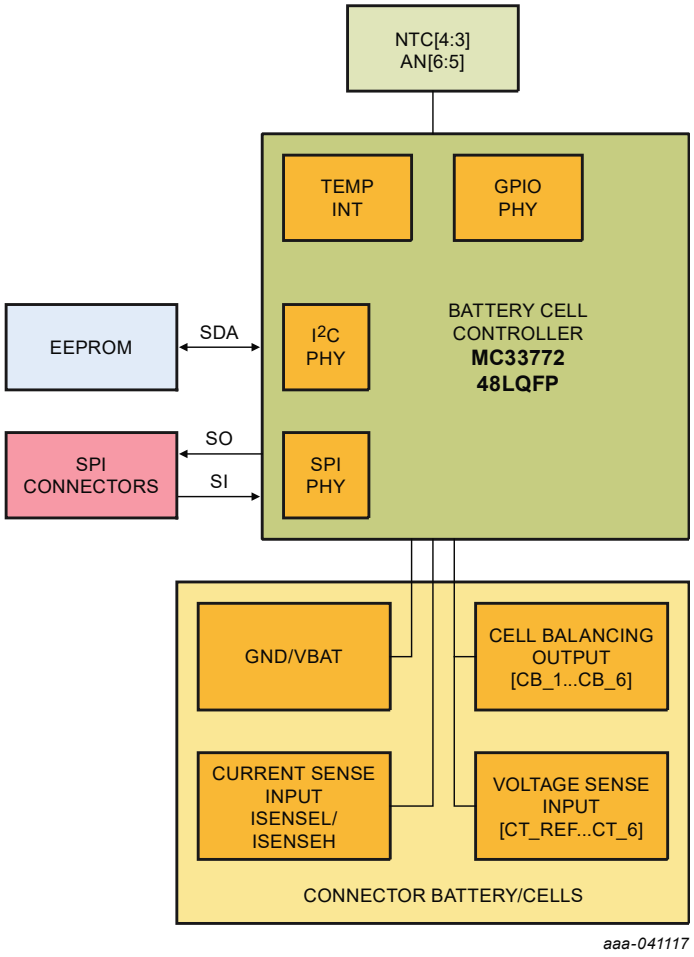


Figure 2. FRDM33772CSPEVB block diagram

4.4 Device features

The MC33772C is a battery cell controller IC designed to monitor battery characteristics, such as voltage, current, and temperature. The MC33772C contains all the circuit blocks necessary to measure synchronous battery cell voltage/current, coulomb counting, cell temperature measurement, and integrated cell balancing. The device supports the following functions:

Table 1. MC33772C device features

Device	Description	Features
MC33772C	battery cell controller	• 5.0 V ≤ V_{PWR} ≤ 30 V operation, 40 V transient • 3 to 6 cells management • Isolated 2.0 Mbit/s differential communication or 4.0 Mbit/s SPI • Addressable on initialization • Bidirectional transceiver to support up to 63 nodes in daisy chain • 0.8 mV maximum total voltage measurement error • Synchronized cell voltage/current measurement with coulomb count • Averaging of cell voltage measurements • Total stack voltage measurement • Seven GPIO/temperature sensor inputs • 5.0 V at 5.0 mA reference supply output • Automatic over/undervoltage and temperature detection routable to fault pin • Integrated sleep mode over/undervoltage and temperature monitoring • Onboard 300 mA passive cell balancing with diagnostics • Hot plug capable • Detection of internal and external faults, as open lines, shorts, and leakage • Designed to support ISO 26262, up to ASIL D safety system • Qualified in compliance with AEC-Q100

4.5 Board description

The FRDM33772CSPEVB allows the user to exercise all the functions of the MC33772C battery controller cell.

It is stacked onto an S32K144EVB. SPI communication is done through connector K1 to K6. The FRDM33772CSPEVB is supplied when connected to a battery cell stack through connector J12. The S32K144EVB is supplied through its USB connection when connected to a PC.

The VCOM LED indicates when the device is in normal mode. Upon reset, the MC33772C enters init mode (VCOM turns on). If there is no activity on the bus after a timeout period of 60 s, the device enters low-power idle mode (VCOM turns off). Once the device is initialized, if no communication occurs on the transformer physical layer (TPL) bus after 1 s, the device resets, and the LED turns off after the 60 s timeout period (VCOM off).

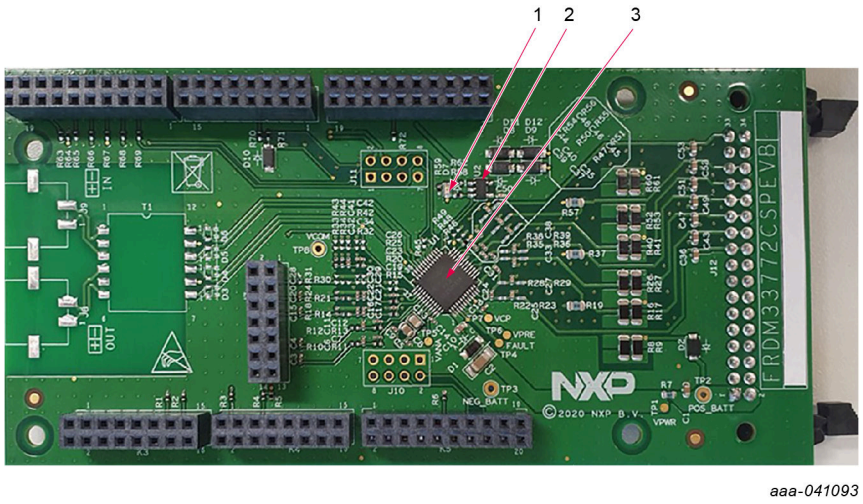


Figure 3. Board description

Table 2. Board components

Number	Label	Name	Description
1	D7	VCOM LED	indicates whether the device is in normal mode or in low-power mode
2	U2	24LC01BT-I/OT	IC memory EEPROM
3	U1	MC33772C	battery cell controller IC

4.6 Test point definitions

The following test points provide access to various signals to and from the board. Figure 4 shows the location of the test points on the board.

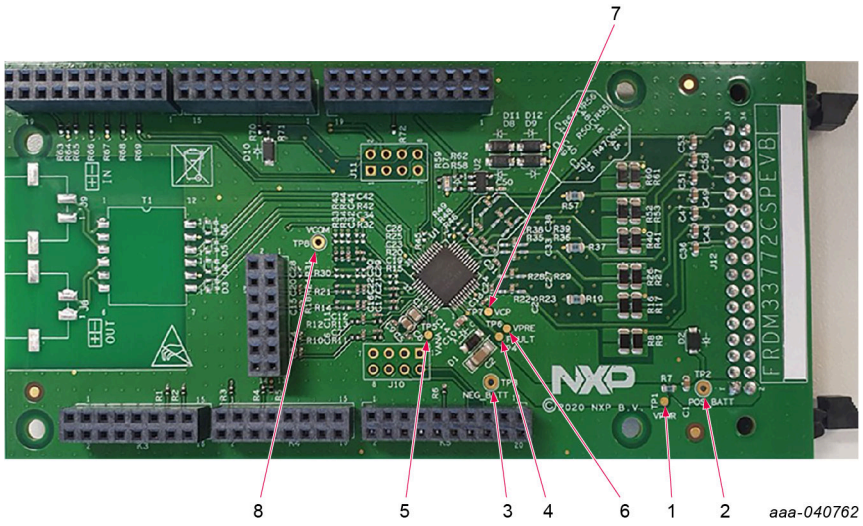


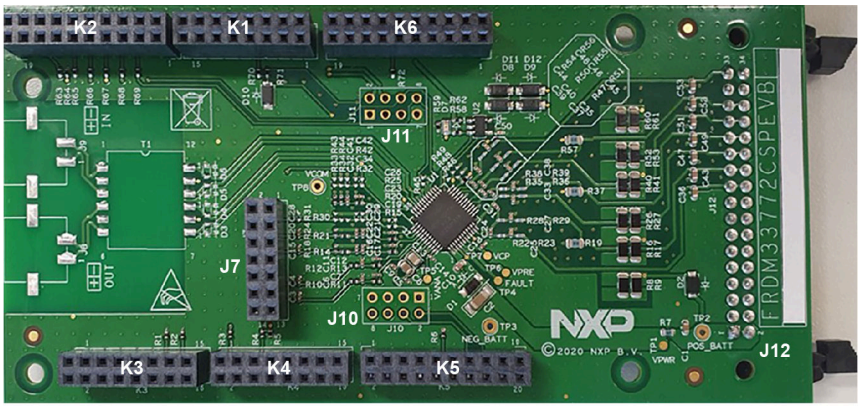
Figure 4. Test points

Table 3. Test points

Number	Label	Name	Description
1	TP1	VPWR	power input to the device
2	TP2	POS_BATT	battery positive
3	TP3	NEG_BATT	battery negative
4	TP4	FAULT	device FAULT output pin
5	TP5	VANA	precision analog supply output
6	TP6	VPRE	VPRE pre-regulator output
7	TP7	VCP	charge pump output voltage
8	TP8	VCOM	VCOM output regulator

4.7 Connectors

Figure 5 shows the location of connectors on the board. The accompanying tables list the pinouts for each connector.



aaa-040763

Figure 5. Connectors

Table 4. SPI connector (K1)

Pin number	Connection	Description
7	FAULT	connects via FAULT_MCU to the device FAULT pin
Other	-	no connection

Table 5. SPI connector (K2)

Pin number	Connection	Description
5	CSB, J11-8	connects via CSB to: • The device CSB pin • Debug connector J11 pin 8
7	SI/RDTX_IN+, J11-2	connects via master output slave input (MOSI) to: • The device SI/RDTX_IN+ pin • Debug connector J11 pin 2
9	SO, J11-6	connects via master input slave output (MISO) to: • The device SO pin • Debug connector J11 pin 6
11	SCLK/RDTX_IN-, J11-4	connects via SCLK to: • The device SCLK/RDTX_IN- pin • Debug connector J11 pin 4
13	GND	connects to the device ground reference
17	GPIO0	connects via GPIO_WAKEUP to the device GPIO0 pin
Other	-	no connection

Table 6. SPI connector (K3)

Pin number	Connection	Description
11	GND	connects to the device ground reference
13	GND	connects to the device ground reference
Other	-	no connection

Table 7. SPI connector (K4)

Pin number	Connection	Description
1	RESET	connects via RESET to the device RESET pin
5	GPIO2	connects via GPIO2_SOC to the device GPIO2 pin
Other	-	no connection

Table 8. SPI connector (K5)

Pin number	Connection	Description
12	GND	connects to the device ground reference
13	DEBUG1	connects via DEBUG1 to DEBUG1 (pin 4) on SPI analyzer interface connector J10
15	DEBUG2	connects via DEBUG2 to DEBUG2 (pin 2) on SPI analyzer interface connector J10
Other	-	no connection

Table 9. SPI connector (K6)

Pin number	Connection	Description
12	GND	connects to the device ground reference
Other	-	no connection

Table 10. Debug connector (J10)

Pin number	Connection	Description
J10-2	DEBUG2	connects via DEBUG2 to pin 15 on connector K5
J10-4	DEBUG1	connects via DEBUG1 to pin 13 on connector K5
J10-6	VCOM	connects to the device VCOM pin
J10-8	FAULT, K1-7	connects via FAULT_MCU to: • The device FAULT pin • Pin 7 on connector K1
Other	GND	connects to the device ground reference

Table 11. Debug connector (J11)

Pin number	Connection	Description
J11-2	SI/RDTX_IN+, K2-7	connects via MOSI to: • The device SI/RDTX_IN+ pin • Pin 7 on connector K2
J11-4	SCLK/RDTX_IN-, K2-11	connects via SCLK to: • The device SCLK/RDTX_IN- pin • Pin 11 on connector K2
J11-6	SO, K2-9	connects via MISO to: • The device SO pin • Pin 9 on connector K2
J11-8	CSB, K2-5	connects via CSB to: • The device CSB pin • Pin 5 on connector K2
Other	GND	connects to the device ground reference

Table 12. Temperature sensor and AN connector (J7)

Pin number	Connection	Description
J7-4	NTC3_P input	GPIO3 pin through low-pass filter (LPF) for negative temperature coefficient (NTC) acquisition
J7-6	NTC4_P input	GPIO4 pin through LPF for NTC acquisition
J7-12	AN5	GPIO5 pin through LPF for absolute measurement
J7-14	AN6	GPIO6 pin through LPF for absolute measurement
J7-odd	GND	odd pins connected to GND; all even numbers, not mentioned in this table are not connected

Table 13. Cell terminal connector (J12)

Pin number	Connection	Description
J12-1 and J12-2	VBAT	MC33772C power supply; positive battery
J12-19	CT_6	cell pin 6 input with external LPF
J12-20	CB_6	cell balance driver; terminate to cell 6 cell balance resistor
J12-21	CT_5	cell pin 5 input with external LPF
J12-22	CB_6:5_C	cell balance driver; terminate to cell 6 and cell 5 cell balance resistor
J12-23	CT_4	cell pin 4 input with external LPF
J12-24	CB_4	cell balance driver; terminate to cell 4 cell balance resistor
J12-25	CT_3	cell pin 3 input with external LPF
J12-26	CB_4:3_C	cell balance driver; terminate to cell 4 and cell 3 cell balance resistor

Table 13. Cell terminal connector (J12)*...continued*

Pin number	Connection	Description
J12-27	CT_2	cell pin 2 input with external LPF
J12-28	CB_2	cell balance driver; terminate to cell 2 cell balance resistor
J12-29	CT_1	cell pin 1 input with external LPF
J12-30	CB_2:1_C	cell balance driver; terminate to cell 2 and cell 1 cell balance resistor
J12-31	ISENSE_P	current measurement input+ with external RC filter
J12-32	ISENSE_N	current measurement input− with external RC filter
J12-33	CT_REF	cell pin REF input with external LPF
	CB_1	cell balance driver; terminate to cell 1 cell balance resistor
J12-34	GND	negative battery

4.8 External EEPROM

The FRDM33772CSPEVB has an integrated gateway communication link to an external local EEPROM. The I^2C-bus communication interface of the MC33772C manages communication with the EEPROM.

After a reset, the EEPROM is not enabled. When the EEPROM is enabled, the device can load the EEPROM calibration parameters into the MC33772C registers.

For more information on using an external EEPROM with the MC33772C device, see the MC33772C data sheet.

4.9 GPIO configuration

The MC33772C has seven GPIO pins available for external connections. On the FRDM33772CSPEVB, those pins are allocated as follows:

- GPIO0 is connected to the S32K connector K2 for the wake-up function
- GPIO1 is connected to an onboard NTC for evaluation board (EVB) temperature measurement
- GPIO2 is connected to the S32K connector K4 for start of conversion (SOC) requests
- GPIO3 and GPIO4 are available for temperature measurement through connector J7 to an external NTC
- GPIO5 and GPIO6 are available for absolute analog measurement through connector J7

4.10 Cell terminal voltage measurement

The differential measurement of each cell terminal input is designed to function with an external anti-aliasing filter with a corner frequency.

4.11 Current sensing

The FRDM33772CSPEVB supports a current sense function with an off-board shunt resistor. The off-board shunt resistor must be connected between J12-31 (ISENSE_P) and J12-32 (ISENSE_N). Refer to the MC33772C data sheet regarding the maximum voltage that can be applied on these pins. The onboard current sensing filter and protection circuits are found on the FRDM33772CSPEVB tool summary page: http://www.nxp.com/FRDM33772CSPEVB.

4.12 SPI communication

The MC33772C SPI is a standard SPI slave interface with a chip select (CSB), clock (SCLK), slave output (SO), and slave input (SI). The SI/SO shifting of the data follows a FIFO protocol, with both input and output words transferring the most significant bit (MSB) first.

The microcontroller controls all SPI communication to the MC33772C. One 48-bit register of previously requested data is retrieved through serial out for each current serial in message sent by the MCU. For message integrity and communication robustness, each SPI transmit message consists of six fields containing 48 bits.

5 Configuring the hardware

The FRDM33772CSPEVB can be configured as a shield board connected to an S32K144EVB board.

5.1 Board configuration

See Figure 6. When both boards are connected together, the SPI connector is directly connected with the MCU SPI pins. In this configuration, power is supplied to the S32K144EVB through a USB cable connected between the S32K144EVB board and a PC. No external power supply is required.

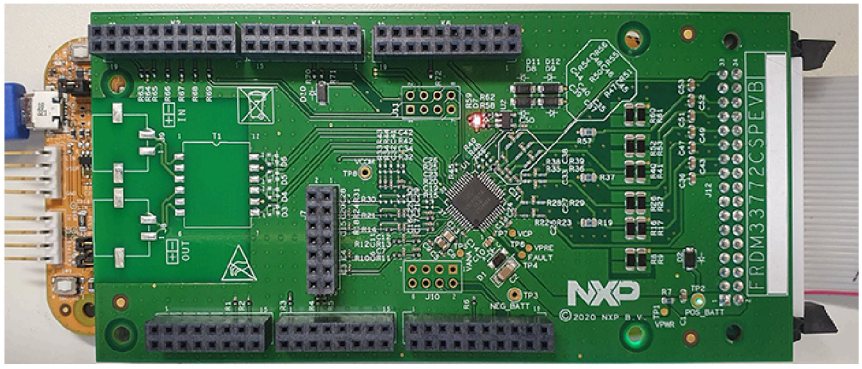


Figure 6. FRDM33772CSPEVB mounted to an S32K144EVB

5.2 Battery emulator connection

The FRDM33772CSPEVB supports the use of a battery cell emulator such as BATT-6EMULATOR board and BATT-14AAAPACK of NXP.

The BATT-6EMULATOR is a 6 cell battery emulator board that provides an intuitive way to change the voltage across any of the 6 cells and four voltage outputs in order to emulate four external NTC.

The emulator board can be connected to the FRDM33772CSPEVB connector J12 using the provided supply cable.

To exercise the FRDM33772CSPEVB in combination with the BATT-6EMULATOR, a graphical user interface is available at https://www.nxp.com/webapp/Download?colCode=KIT3377xC_APPSP&appType=license.

6 Available accessories

Note: *NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the responsibility of the customer to validate their application.*

Table 14. BOM

Part number	Description
BATT-6EMULATOR	6-cell slider battery pack emulator kit with shunt for current sense
BATT-14AAAPACK	configurable battery pack to supply the EVBs of the MC33772

7 References

[1] **FRDM33772CSPEVB tool summary page** — detailed information on the board, including documentation, downloads, software and tools
http://www.nxp.com/FRDM33772CSPEVB

[2] **Product summary page** — product information on the MC33772C battery cell controller IC
http://www.nxp.com/MC33772C

[3] **Tool summary page for battery emulators** — detailed information on the cell battery pack emulator, including documentation, downloads, software and tools
http://www.nxp.com/BATT-6EMULATOR and http://www.nxp.com/BATT-14AAAPACK

[4] **NXP DocStore** — released NXP documents available to users
docstore.nxp.com

8 Revision history

Revision history

Revision	Date	Description
v.1	20210304	initial version

9 Legal information

9.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 March 2021
Document identifier: UM11561