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1. Overview

R9A06G061 is a modem LSI for narrow-band power line communications (Narrow Band PLC). The R9A06G061 is a product that optimizes performance and functionality (small package, low power, low cost) and provides demodulation signal processing (physical layer) for software-based PLCs based on a high-performance DSP with an MCU (link layer) (ARM® Cortex™-M0+) to provide a flexible and inexpensive PLC solution.

1.1 Features

- High-performance DSP
  - Handle PHY layer of power line communication etc.
  - Maximum operating frequency: 276MHz
  - IRAM: 128KB, DRAM: 128KB
  - Dedicated instructions for Viterbi and Reed Solomon processing, AES128 encryption/decryption processing, and others
- MCU (ARM® Cortex™-M0+)
  - Handle protocol conversion processing for the external MCU interface etc.
  - Maximum operating frequency: 92MHz
  - RAM: 32KB
  - CRC Operation H/W Core
- Analog front-end (AFE) circuit
  - DAC
    - Delta Sigma DA converter
    - ENOB:11bit
  - Variable Output Amplifiers
    - 114dBuVrms output (high output mode, 50-ohm drive for differential terminals)
    - Gain variable, in 3dB steps
  - Variable Receiving Amplifiers
    - Dynamic range: -18dB to +60dB, 2dB steps
    - AGC with DSP control
  - ADC
    - Delta Sigma ADC
    - ENOB:10bit
- A variety of External IOs
    - UART(1ch), SPIs(1ch), Serial Flash IF(Single/Dual)
    - PORT(10ch) (* however, exclusive use with above peripherals)
- Built-in regulator: 3.3V input, 1.15V DC-DC converter
- Supply voltage:3.3V
- PKG:40-pin QFN 6mm x 6mm, 0.5mm pitch□
- Operating temperature
  - -40 to+ 85 degrees

1.2 System configuration

The R9A06G061 provides customers with a high level of communication performance and cost-effective solutions for the formation of power line communication networks. Figure 1. 1and Figure 1. 2show examples of system configurations of a PLC module using R9A06G061.

1.2.1 Low-cost configuration: No external line driver (direct drive）

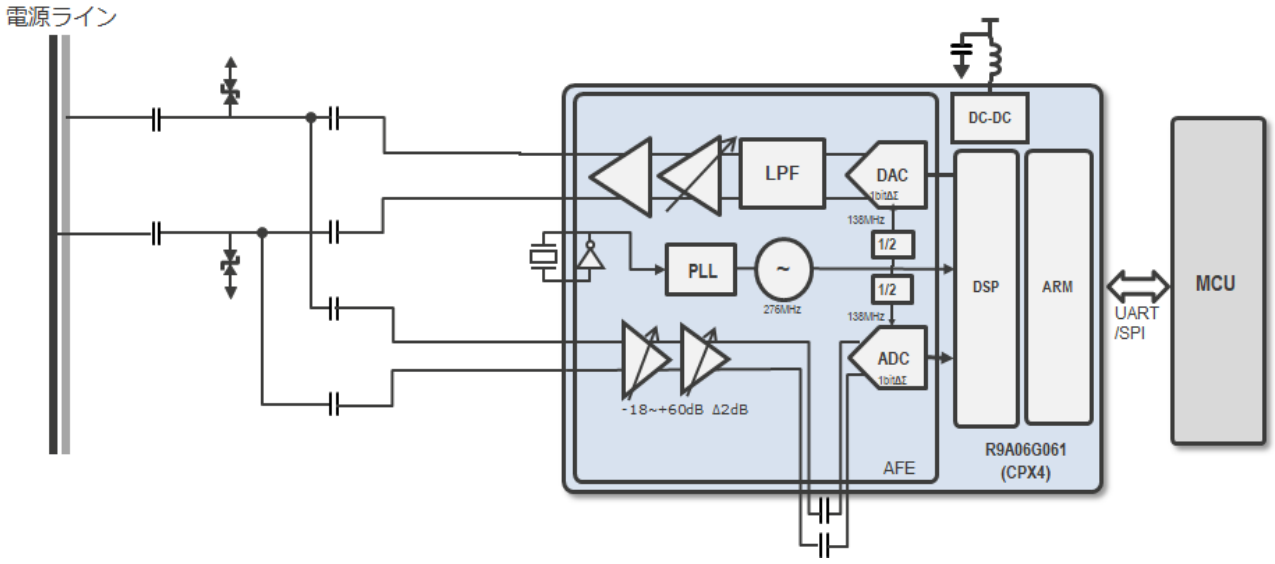


Figure 1. 1 R9A06G061 System Configuration Example 1

1.2.2 High-drive configuration: External line driver

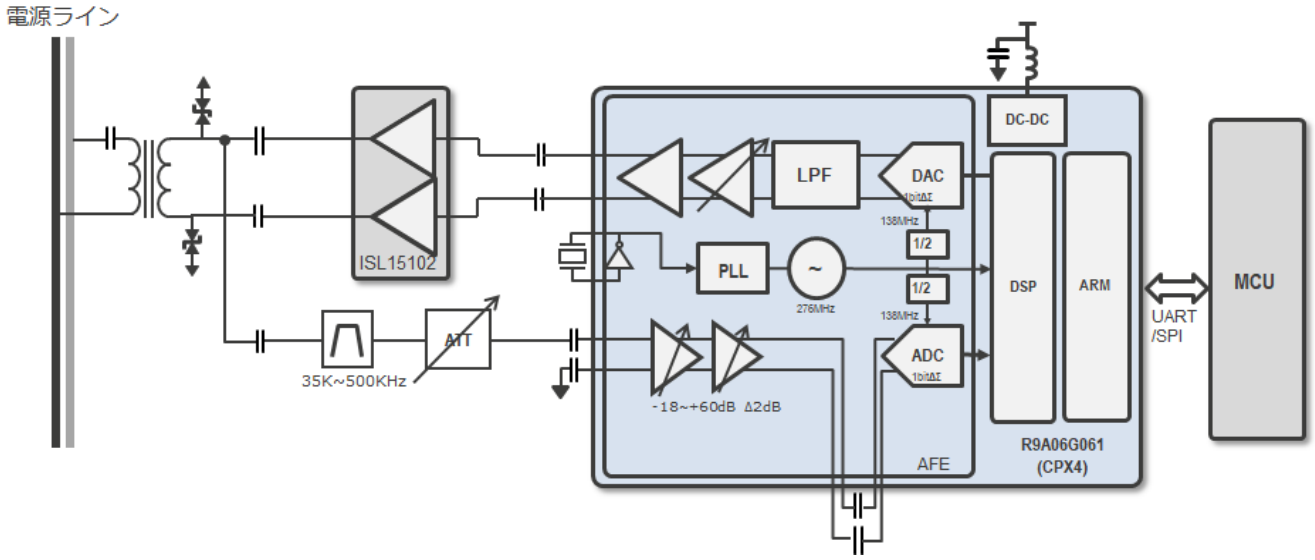


Figure 1. 2 R9A06G061 System Configuration Example 2

2. Pin function

2.1 Pin assignment

Fig.2.1 shows the pin assignment of R9A06G061.

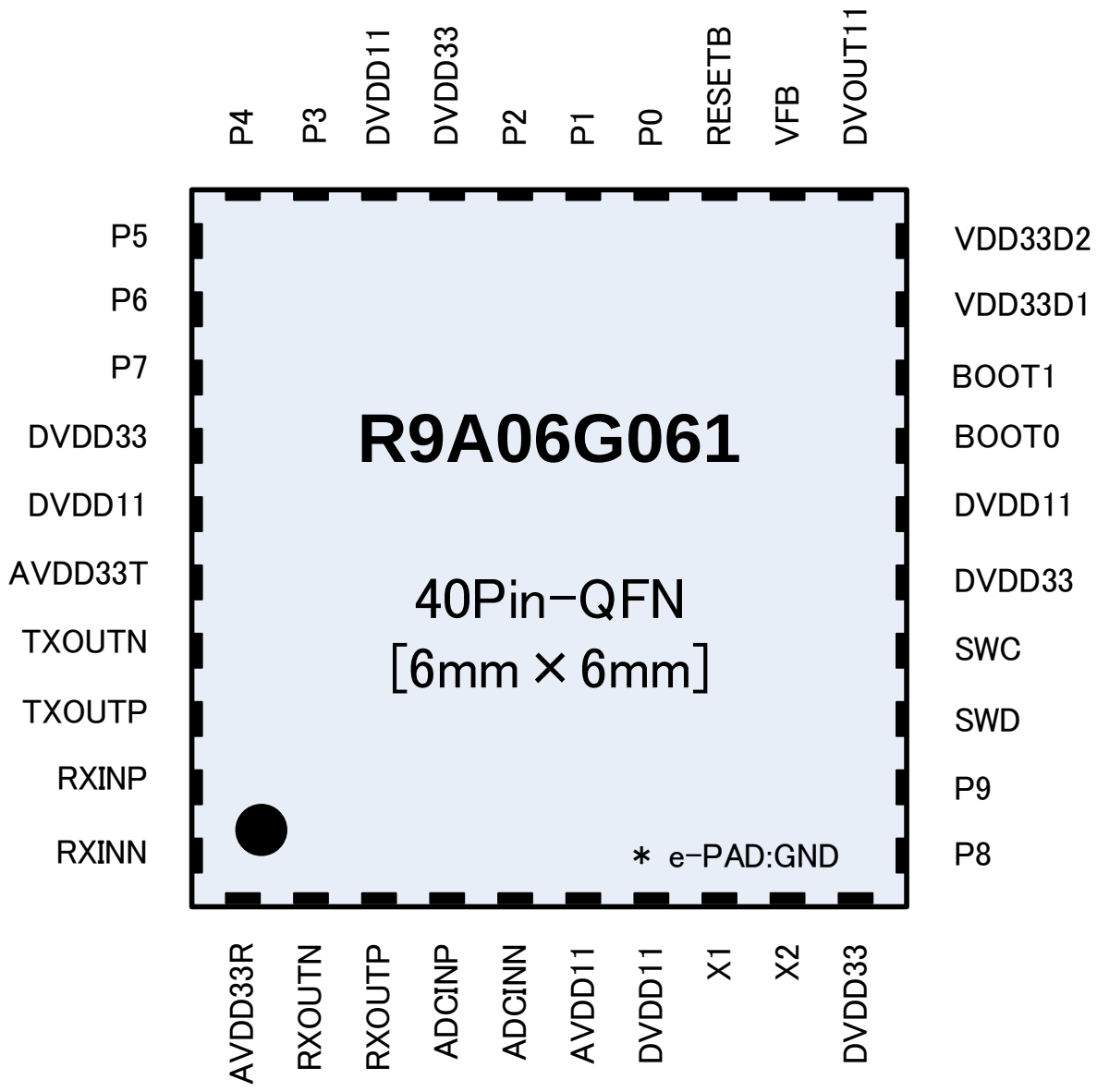


Figure 2. 1 configuration

2.2 Pin description

2.2.1 System Clocks & Reset

Pin name	I/O	BUFTYPE	Pin No	Functions
X1	I	-	8	External X'tal oscillator input f:16MHz/20MHz/24MHz/32MHz Set the value of P2 and P1 at the time of system reset release. 16MHz: P2=High, P1=High 20MHz: P2=High, P1=Low 24MHz: P2=Low , P1=High 32MHz: P2=Low , P1=Low
X2	O	-	9	External X'tal oscillator Output
RESETB	I	Schmitt/PU	23	System Reset (with Pull-Up resistor)

PU: With a 50KΩ internal pullup resistor

2.2.2 BOOT I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
BOOT0	I	PU	17	Boot mode selection (with an internal Pullup resistor) UART [BOOT1 =High, BOOT0=High] SPI [BOOT1 =Low, BOOT0=High] SROM [BOOT1 =High, BOOT0=Low] <u>UART_S-IF</u> RXD :P2 TXD :P1 <u>SPI-IF</u> SO :P1 SSB :P4 SCK :P3 SI :P2 REQ :P5 <u>SROM-IF</u> SIO1/MISO :P9 SSB :P7 SCK :P8 SIO0/MOSI :P6
BOOT1	I	PU	18	

PU: With a 130KΩ internal pullup resistor

2.2.3 PORT I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
P0	I/O	B-4/8mA Schmitt/PU/PD	24	I/O Port [0] *Note1
P1	I/O	B-4/8mA Schmitt/PU/PD	25	I/O Port [1]
P2	I/O	B-4/8mA Schmitt/PU/PD	26	I/O Port [2]
P3	I/O	B-4/8mA Schmitt/PU/PD	29	I/O Port [3]
P4	I/O	B-4/8mA Schmitt/PU/PD	30	I/O Port [4]
P5	I/O	B-4/8mA Schmitt/PU/PD	31	I/O Port [5]
P6	I/O	B-4/8mA Schmitt/PU/PD	32	I/O Port [6]
P7	I/O	B-4/8mA Schmitt/PU/PD	33	I/O Port [7]
P8	I/O	B-4/8mA Schmitt/PU/PD	11	I/O Port [8]
P9	I/O	B-4/8mA Schmitt/PU/PD	12	I/O Port [9]

PD: With a 160KΩ internal pulldown resistor / PU: With a 130KΩ internal pullup resistor.
The default buffer type for P1-P9 is 8mA / PU ((with 130KΩ internal pullup resistor).
The function of each PORT pins can be selected from UART, CSI, IIC, Serial-ROM-IF (Single/Dual/Quad), PWM.
*Note1: The initial value of P0 is the output of the system clock entered in X1/X2.

2.2.4 TX_PGA I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
TXOUTP	O	Analog	38	TX_PGA signal output (+)
TXOUTN	O	Analog	37	TX_PGA signal output (-)

2.2.5 RX_PGA I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
RXINP	I	Analog	39	RX_PGA signal input (+)
RXINN	I	Analog	40	RX_PGA signal input (-)
RXOUTP	O	Analog	3	RX_PGA signal output (+)
RXOUTN	O	Analog	2	RX_PGA signal output (-)

2.2.6 ADC I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
ADCINP	I	Analog	4	ADC signal input (+)
ADCINN	I	Analog	5	ADC signal input (-)

2.2.7 Power/Other

Pin name	I/O	BUFTYPE	Pin No	Functions
DVDD33	I	-	10 15 27 34	IO buffer power supply 3.3V
DVDD11	I	-	7 16 28 35	Internal core power supply 1.15V (Supplied from DCDC output DVOUT11 with external LC smoothing filter)
VDD33D1	I	-	19	DCDC 3.3V power supply (control unit)
VDD33D2	I	-	20	DCDC 3.3V power supply (output stage)
DVOUT11	O	-	21	DCDC output (3.3V PWM) 1.15V generation with external LC smoothing filter
VFB	I	-	22	DCDC 1.15V Feedback (for PWM control)
AVDD33T	I	-	36	Analog power supply 3.3V (for transmission circuit)
AVDD33R	I	-	1	Analog power supply 3.3V (for receiving and common circuit)
AVDD11	I	-	6	Analog power supply 1.15V (Supplied from DCDC output DVOUT11 with external LC smoothing filter)
GND	I	-	-	Common Ground (Backside PAD)

2.2.8 Debug I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
SWC	I	Schmitt/PU	14	SWDCLK
SWD	I/O	Schmitt/PU	13	SWDIO

PU: With a 130KΩ internal pullup resistor

3. Function overview

3.1 Block diagram

Figure 3. 1shows an internal functional block diagram of R9A06G061. R9A06G061 is made up of ARM domain, DSP domain and AFE domain. It also has a built-in PORT and regulator.

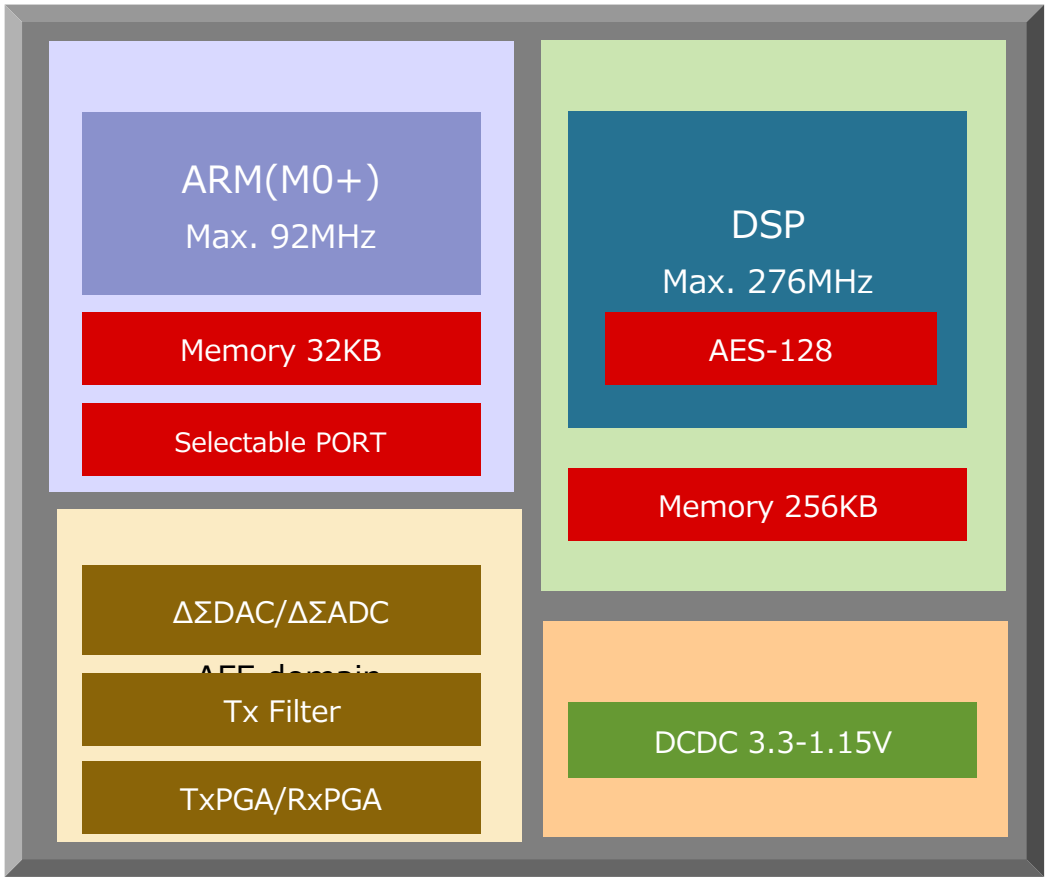


Figure 3. 1 R9A06G061 Block Diagram

3.2 ARM domain

3.2.1 ARM M0+

R9A06G061 integrates ARM® Cortex™-M0+. Maximum operational clock frequency is 92MHz.

3.2.2 Memory

ARM domain includes 32Kbytes of RAM. This is used for protocol processing and data translation between ARM and DSP domains.

3.3 DSP domain

3.3.1 DSP

DSP domain has a high-performance DSP. The DSP supports a variety of hardware-based instructions for Viterbi, Read Solomon and other functions. The DSP can effectively realize various power line communication PHY layer with the hardware-based instructions. The maximum clock frequency of the DSP is 276MHz. The clock frequency can be changed from 4.3MHz and 276MHz dynamically. When the clock frequency is managed according to the load of the DSP, the power consumption can be optimized.

3.3.2 Memory

DSP domain includes 128KBytes of instruction RAM and 128KBytes of data RAM.

3.4 AFE (Analog Front End) domain

3.4.1 DAC

Delta sigma DA converter. Achieves ENOB :11bit accuracy at a sampling frequency of 138MHz.

3.4.2 TX_ PGA

Programable Transmit Amplifier that can adjust ouput signal gain. The gain is programmable in 3dB steps from -3dB to +18dB

3.4.3 RX_ PGA

Programable Receive Amplifier that can adjust received signal gain. The gain is programmable in 2dB steps from -18dB to +60dB. DSP computes the received signal level optimization. DSP controls the gain of RX PGA based on the computation. Then, AGC (Auto Gain Control) that controls the amplitude of the recived signal automatically can be realized.

3.4.4 ADC

Delta Sigma AD converter. Maximum sampling frequency 276MHz. Achieves ENOB :10bit accuracy (SINAD :62 dB) in PLC signal bands below 600KHz.

3.5 Regulator

3.5.1 DC-DC

3.3V to 1.15V power supply voltage is generated by the switching regulator. It can supply 1.15V power supplies for digital and analog circuits in R9A06G061.

4. Electrical characteristics

4.1 Absolute maximum ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD, AVDD	1.15V	-0.3～+1.6	V
		3.3V	-0.3～+4.2	V
I/O voltage	V_i/V_o	VI/VO<VDD+0.5V	-0.3～+4.2	V
Output current (3.3V buffer)	I_o	4mA/8mA	8.7/16	mA

Cautions)

Product quality may be impaired if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, therefore, the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

4.2 Recommended operating condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage (Digital)	VDD	3.3V	3.0	3.3	3.6	V
Power supply voltage (Analog)	AVDD	3.3V	3.0	3.3	3.6	V
Negative trigger input voltage	V_N	3.3V operation	0.8		1.8	V
Positive trigger input voltage	V_P	3.3V operation	1.1		2.4	V
Hysteresis Voltage	V_H	3.3V operation	0.15		1.1	V
Low level input voltage	V_{IL}	3.3V operation	-0.3		0.8	V
High level input voltage	V_{IH}	3.3V operation	2.4		VDD33+0.3	V
An input rise/ fall time (data)	t_{rid}	-	0		200	ns
	t_{fid}	-	0		200	ns
An input rise/ fall time (clock)	t_{ric}	-	0		4	ns
	t_{fic}	-	0		4	ns
An input rise/ fall time (Schmidt)	t_{ris}	-	0		1	ms
	t_{fis}	-	0		1	ms
Operating ambient temperature	T_a		-40		+85	℃

4.3 Power Up/Down and Reset Sequence

4.3.1 Power Up/Down Sequence

Figure 4. 1shows the power up/down sequence. It is recommended that the time which elapses from the start of power-supply rise (Analog power (AVDD33) and I/O power (IO_VDD) until both power supplies are stabilized should be within 100ms, regardless of the order of power supply.

Power supply voltage is recommended to rise from 0.1 VDD to 0.95 VDD within 100ms.

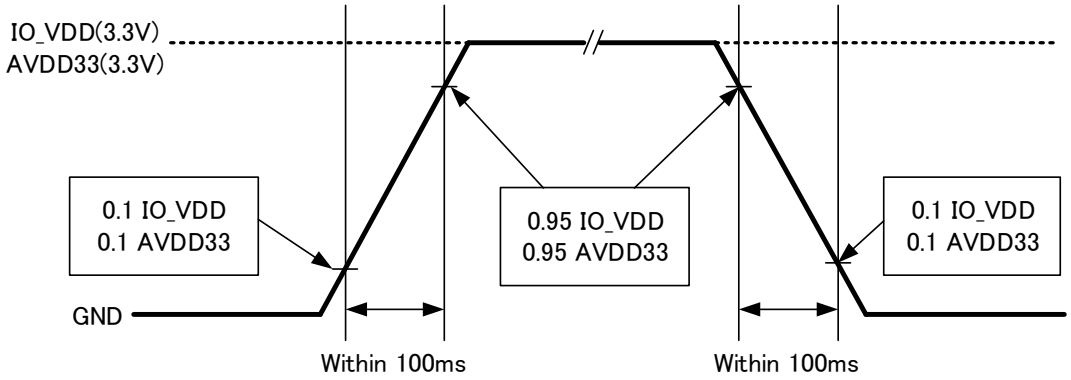


Figure 4. 1 diagram of the power ON/OFF sequence

4.3.2 Reset Sequence

Figure 4. **2**shows R9A06G061 reset sequence. Do not de-assert RESETB before keeping the low level for at least 1ms from the moment IO power supply reaches 95% of 3.3V (0.95 IO_VDD).

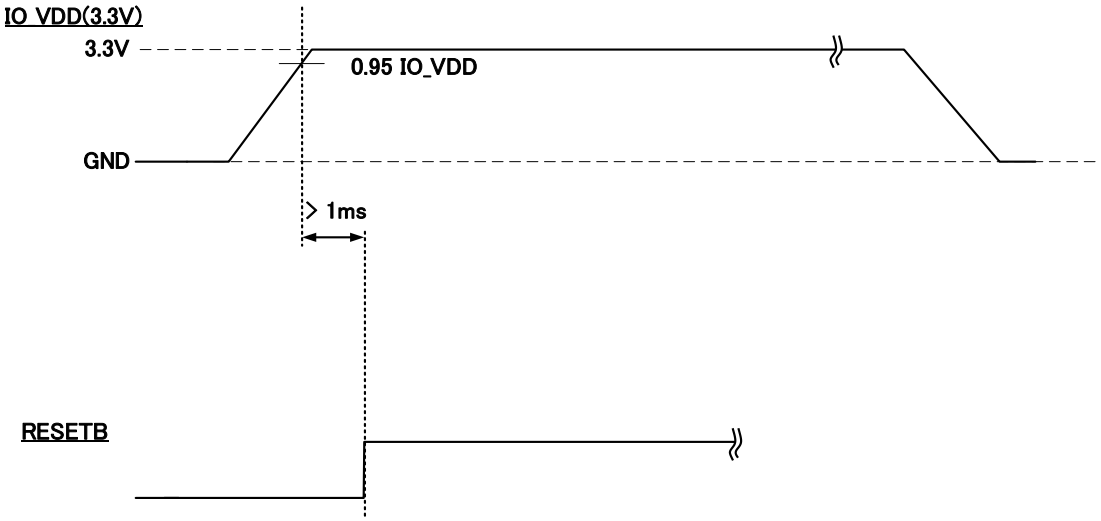


Figure 4. 2 Timing diagram of reset sequence and power-up constraints

4.3.3 System Clocks & Timings

Symbol	Parameter	MIN	TYP	MAX	Units
$F_{XTALcyc}$	X1/X2 X'tal clock frequency		16,20,24,32 ±25ppm		MHz

Clock timing

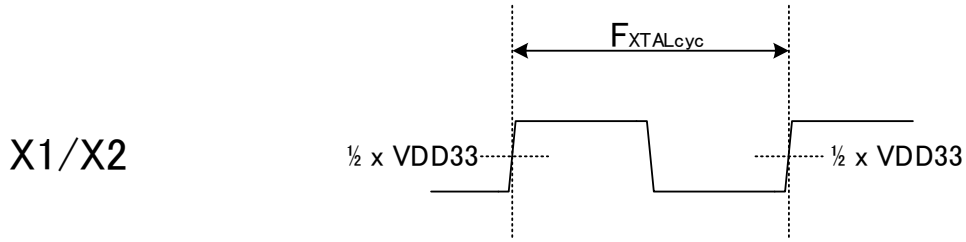


Figure 4. 3 System clock timing

4.4 DC Characteristics

DC Characteristics (VDD=3.3+/-0.3V, T_a = −40~+85 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	Normal input V_{in}=GND	-	-	-10	μA
	I_{IH}	Normal input V_{in}=IOVDD	-	-	10	μA
	I_{PU1} (Other than RESETB)	Pull-up resistor V_{in}=GND	-6.7	-	-200	μA
	I_{PD1} (Other than RESETB)	Pull-down resistor V_{in}=IOVDD	6.7	-	200	μA
	I_{PU2} (RESETB only)	Pull-up resistor V_{in}=GND	-30	-	-144	μA
Output leakage current	I_{OZL}	V_o=GND	-	-	-10	μA
	I_{OZH}	V_o=IOVDD	-	-	10	μA
Low level output current	I_{OL}	V_{OL}=0.4V 4mA/8mA	4/8	-	-	mA
High level output current	I_{OH}	V_{OH}=IOVDD-0.4V 4mA/8mA	-4/-8	-	-	mA
Pull up resistor 1 (other than RESETB)	R_{PU1}	V_{in}=GND	18	130	450	KΩ
Pull down resistor	R_{PD1}	V_{in}=IOVDD	18	160	450	KΩ
Pull-up resistor 2 (RESETB Pull up resistor only)	R_{PU2}	V_{in}=GND	25	50	100	KΩ
Low level output voltage	V_{OL}	I_{ol}=0mA	-	-	0.1	V
High level output voltage	V_{OH}	I_{oh}=0mA	IOVDD-0.1	-	-	V

4.5 AC Characterstics

4.5.1 UART I/F

Figure 4. 4shows a timing diagram of UART interface.

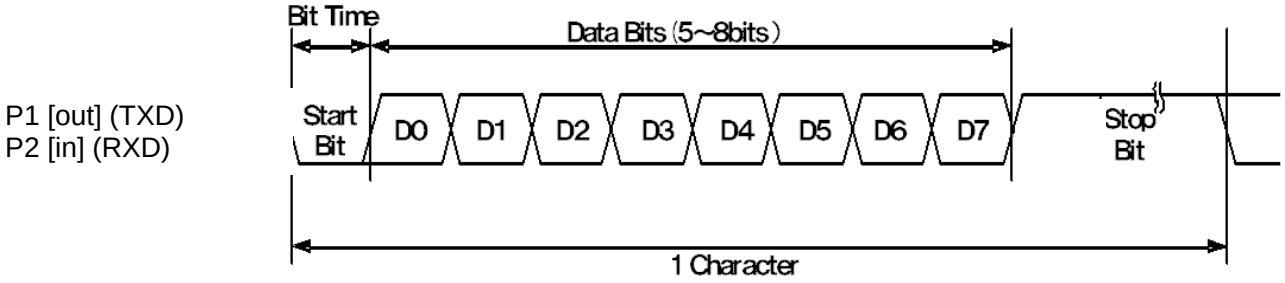


Figure 4. 4of UART interface

4.5.2 SPIs I/F

Figure 4. 5shows a timing diagram of SPIs interface.

Symbol	Parameter	MIN	TYP	MAX	Units
F_{CLK}	Communication clock frequency			25 (T_{SCK} = 40.0ns)	MHz
T_{SCKH}, T_{SCKL}	Communication clock high-low width	T_{SCK}×0.45		T_{SCK}×0.55	ns
T_{DD}	Output signal (SI,SO,SS) Data delay (P1)	0		9	ns
	Output signal (SI,SO,SS) Data delay (P6)	0		14	ns
T_{DS}	Input signal (SI,SO) Data set-up time (P2)	4.6			ns
	Input signal (SI,SO) Data set-up time (P7))	5.6			ns
T_{DH}	Input signal (SI,SO) Data hold time	0			ns
T_{CS}	SS Signal Inactive Time	T_{SCK} × 1.0			ns
T_{CSS}	SS Signal Setup Time	T_{SCK} × 1.5			ns
T_{CSH}	SS Signal Hold Time	T_{SCK} × 1.5			ns

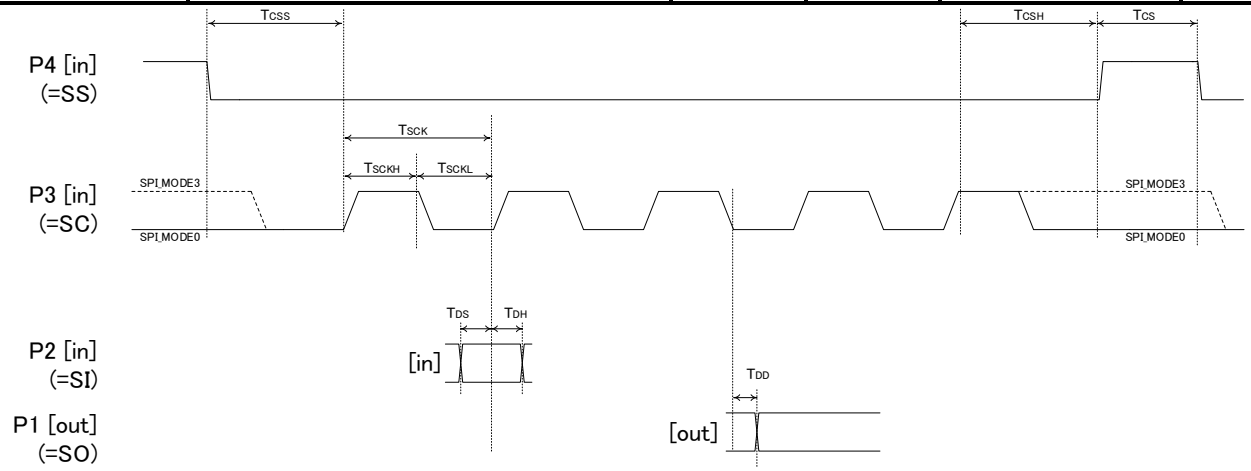


Figure 4. 5of SPIs interface

4.5.3 Serial-ROM I/F

Figure 4. 6shows a timing diagram of the SerialROM interface.

Symbol	Parameter	MIN	TYP	MAX	Units
FCLK	Communication clock frequency	2.875 (TSCK = 347.8ns)		46 (TSCK = 21.7ns)	MHz
TSCKH, TSCKL	Communication clock high-low width	TSCK×0.45		TSCK×0.55	ns
TDD	Output signal (SI,SO,SS) Data delay	0		5	ns
TDS	Input signal (SI,SO) Data setup time (P1,P2)	6			ns
	Input signal (SI,SO) Data setup time (P6,P9)	7			ns
TDH	Input signal (SI,SO) Data hold time	0			ns

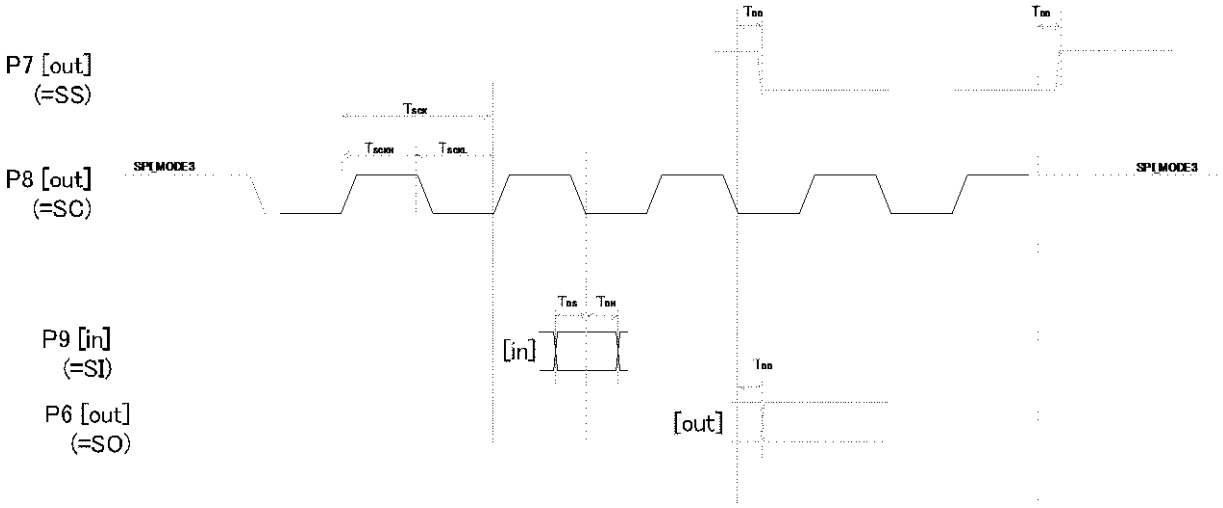


Figure 4. 6 Timing diagram of the SerialROM interface

4.5.4 Debug I/F

Figure 4. 7shows a timing diagram of SCHD interface.

Symbol	Parameter	MIN	TYP	MAX	Units
FCLK	Communication clock frequency			50 (TSCK = 20.0ns)	MHz
TSCKH, TSCKL	Communication clock high-low width	TSCK×0.45		TSCK×0.55	ns
TDD	Output Signal(SWD)) Data Delay	4.0		14.0	ns
TDS	Input Signal(SWD)) Data Setup Time	3.6			ns
TDH	Input Signal(SWD)) Data Hold Time	0			ns

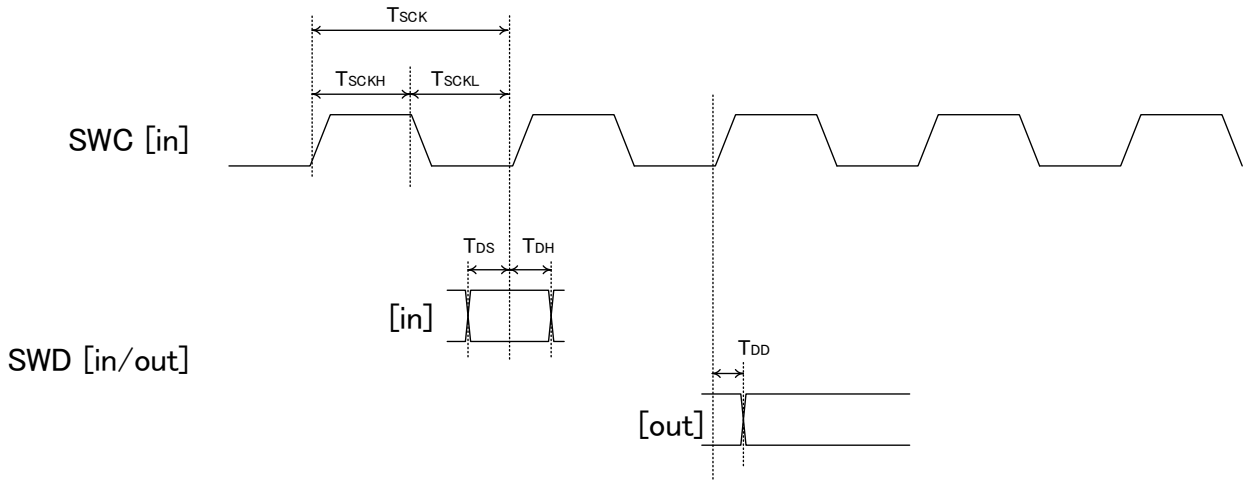


Figure 4. 7 PWD interface

4.5.5 Current Consumption

VDD	MIN.	TYP.	MAX.	Unit
VDD33		38		mA

Conditions: VDD33 = 3.3±0.3V, VDD11 is generated by internal DC-DC converter
With Renesas evaluation board, DSP:276MHz, receive mode with G3-FCC

4.6 Analog block characteristics

4.6.1 DC characteristics

Pin No.	Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
2	Power Supply Voltage		AVDD33T	3.0	3.3	3.6	V
12	Power Supply Voltage		AVDD33R	3.0	3.3	3.6	V

4.6.2 Performance characteristics

4.6.2.1 Receiving blocks

(a) RX_PGA interface

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_i	60u		3.0	Vp-p
Input frequency		F_{sig}	30		500	kHz
Dynamic range (voltage gain range)		DR		78		dB
Gain control step		D_{STEP}		2		dB
Input 1dB Compression	G_V= -14dB, f_{sig}= 30kHz, Differential	$P_{in\ 1dB}$	2.8	3.3		Vp-p
Maximum voltage gain	f_{sig}= 500kHz	G_{V_max}		60		dB
Minimum voltage gain	f_{sig}= 500kHz	G_{V_min}		-18		dB
Input impedance		Z_i		1		kΩ
Output load impedance		R_L		20		kΩ

(b) ADC Interfaces

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_{sig}			800	mVp-p
Input Frequency		F_{SIG}			500	kHz
Sampling frequency		F_{CLK}	-	138	-	MHz
ENOB		ENOB	-	10	-	bit
SINAD		SINAD	-	62	-	dB
Input Impedance		Z_i		20		kΩ

4.6.2.2 Transmit block

(a) TX_PGA interface

Direct-drive (high-power) mode

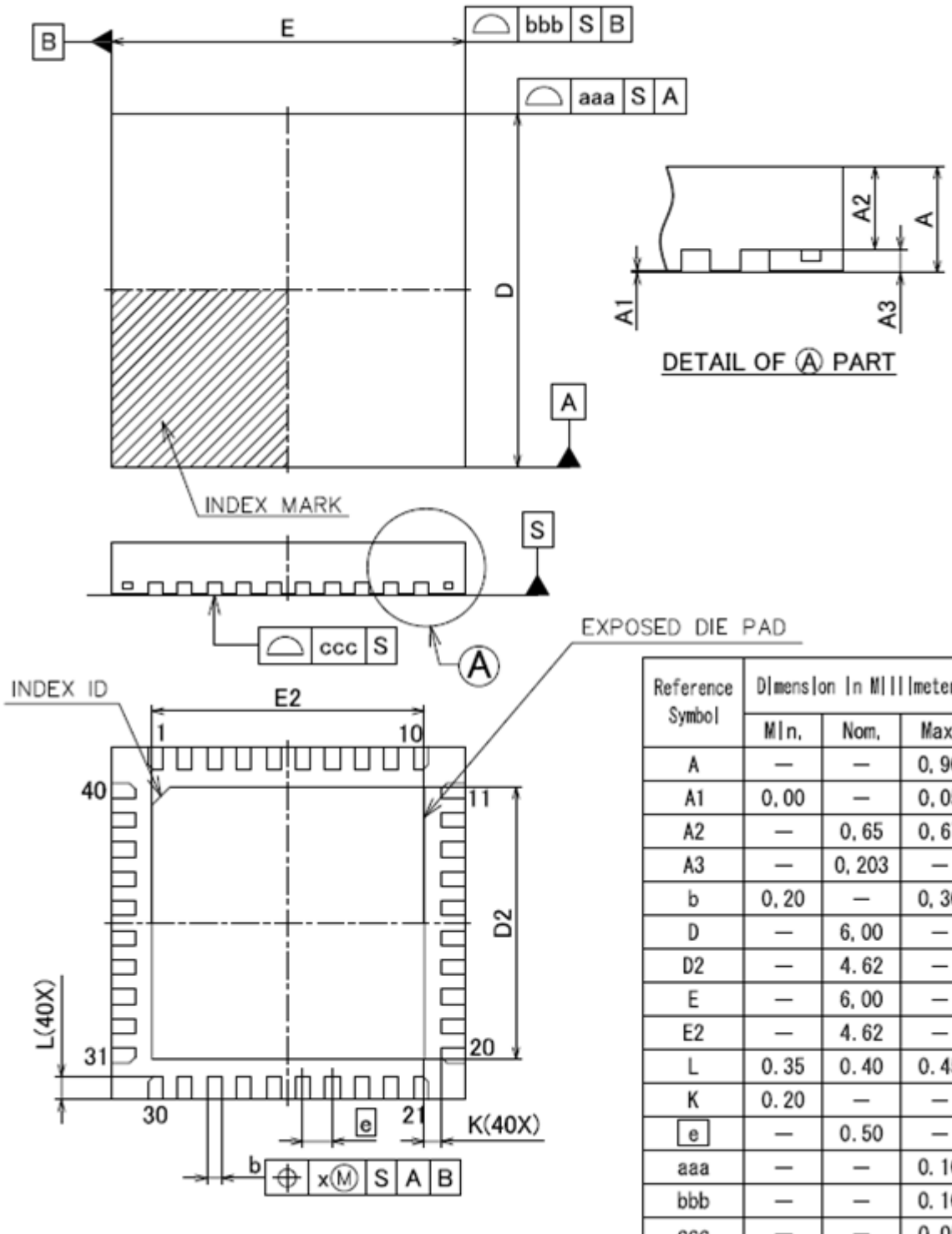
Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Output frequency band		f_{sig}	30		500	kHz
Dynamic range (voltage gain range)		DR		21		dB
Gain control step		D_{STEP}		3		
Maximum voltage gain	f_{sig}= 500kHz, differential output	G_{v_max}		18		dB
Minimum voltage gain	f_{sig}= 500kHz, differential output	G_{v_min}		-3		dB
Output -1dB compression	f_{sig}= 500kHz, differential output Z_L=50Ω (Each terminal), G_V = +3dB	P_1	3			Vp-p
Harmonic Distortion	f_{sig}= 100kHz, 1.4Vp-p differential output, Z_L= 50 Ω (each pin), G_V = +9dB,	HD	-	-70	-60	dBc
Output load impedance		Z_L		50		Ω

External send driver (low output) mode

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Output frequency band		f_{sig}	30		500	kHz
Dynamic range (voltage gain range)		DR		21		dB
Gain control step		D_{STEP}		3		
Maximum voltage gain	f_{sig}= 500kHz, differential output	G_{v_max}		18		dB
Minimum voltage gain	f_{sig}= 500kHz, differential output	G_{v_min}		-3		dB
Output-1dB compression	f_{sig}= 500kHz, differential output Z_L=,390ohms (Each terminal), G_V = +3dB,	P_1	2			Vp-p
Harmonic Distortion	f_{sig}-100kHz, 0.9Vp-p differential output, Z_L= 390Ω (each pin), G_V= +3dB	HD	-	-70	-60	dBc
Output load impedance		Z_L		390		Ω

5. Package

JEITA Package Code	RENESAS Code	MASS [Typ.]
P-HVQFN40-6×6-0.50	PVQN0040KK-A	0.10g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.90
A1	0.00	—	0.05
A2	—	0.65	0.67
A3	—	0.203	—
b	0.20	—	0.30
D	—	6.00	—
D2	—	4.62	—
E	—	6.00	—
E2	—	4.62	—
L	0.35	0.40	0.45
K	0.20	—	—
e	—	0.50	—
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
x	—	—	0.10

6. Part Number

R9A06G061GNP

7. Appendix

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(Rev.4.0-1 November 2017)

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