



Product Change Notification / SYST-17SSCY946

Date:

20-Dec-2021

Product Category:

P-Channel Enhancement Mode MOSFETs

PCN Type:

Document Change

Notification Subject:

Data Sheet - VP2110 Datasheet - P-Channel Enhancement-Mode Vertical DMOS FET Data Sheet
Document Revision

Affected CPNs:

[SYST-17SSCY946_Affected_CPN_12202021.pdf](#)
[SYST-17SSCY946_Affected_CPN_12202021.csv](#)

Notification Text:

SYST-17SSCY946

Microchip has released a new Product Documents for the VP2110 Datasheet - P-Channel Enhancement-Mode Vertical DMOS FET of devices. If you are using one of these devices please read the document located at [VP2110 Datasheet - P-Channel Enhancement-Mode Vertical DMOS FET](#).

Notification Status: Final

Description of Change:

- Converted Supertex Doc# DSFP-VP2110 to Microchip DS20006600A
- Changed the package marking format
- Added sections to comply with Microchip formatting standards
- Made minor text changes throughout the document

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Dec 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

VP2110 Datasheet - P-Channel Enhancement-Mode Vertical DMOS FET

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Affected Catalog Part Numbers (CPN)

VP2110K1-G

VP2110K1-G-D537

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

General Description

The VP2110 Enhancement-mode (normally-off) transistors use a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



See [Table 3-1](#) for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	-100	—	—	V	$V_{GS} = 0V$, $I_D = -1$ mA
Gate Threshold Voltage	$V_{GS(th)}$	-1.5	—	-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1$ mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	5.8	6.5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}$, $I_D = -1$ mA (Note 1)
Gate Body Leakage Current	I_{GSS}	—	-1	-100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	$V_{GS} = 0V$, $V_{DS} =$ Maximum rating
		—	—	-1	mA	$V_{DS} = 0.8$ Maximum rating, $V_{GS} = 0V$, $T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	-0.5	-1	—	A	$V_{GS} = -10V$, $V_{DS} = -25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	11	15	Ω	$V_{GS} = -5V$, $I_D = -100$ mA
		—	9	12	Ω	$V_{GS} = -10V$, $I_D = -500$ mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	0.55	1	%/ $^{\circ}C$	$V_{GS} = -10V$, $I_D = -500$ mA (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T _A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G _{FS}	150	200	—	mmho	V _{DS} = −25V, I _D = −500 mA
Input Capacitance	C _{ISS}	—	45	60	pF	V _{GS} = 0V, V _{DS} = −25V, f = 1 MHz
Common-Source Output Capacitance	C _{OSS}	—	22	30	pF	
Reverse Transfer Capacitance	C _{RSS}	—	3	8	pF	
Turn-On Delay Time	t _{d(ON)}	—	4	5	ns	V _{DD} = −25V, I _D = −500 mA, R _{GEN} = 25Ω
Rise Time	t _r	—	5	8	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	5	9	ns	
Fall Time	t _f	—	4	8	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V _{SD}	—	−1.2	−2	V	V _{GS} = 0V, I _{SD} = −500 mA (Note 1)
Reverse Recovery Time	t _{rr}	—	400	—	ns	V _{GS} = 0V, I _{SD} = −500 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C . Pulse test: 300 μs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	$^\circ\text{C/W}$	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead SOT-23	-120	-400	0.36	-120	-400

Note 1: I_D (continuous) is limited by maximum rated T_J .

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

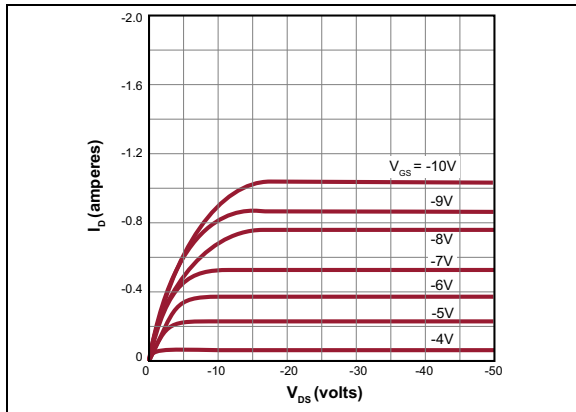


FIGURE 2-1: Output Characteristics.

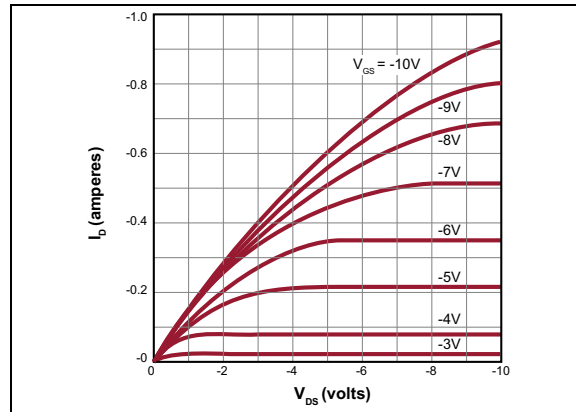


FIGURE 2-4: Saturation Characteristics.

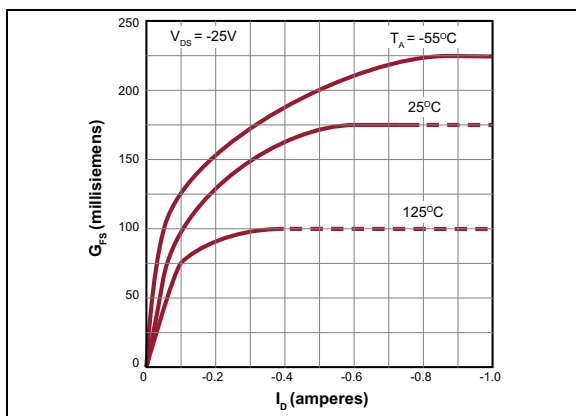


FIGURE 2-2: Transconductance vs. Drain Current.

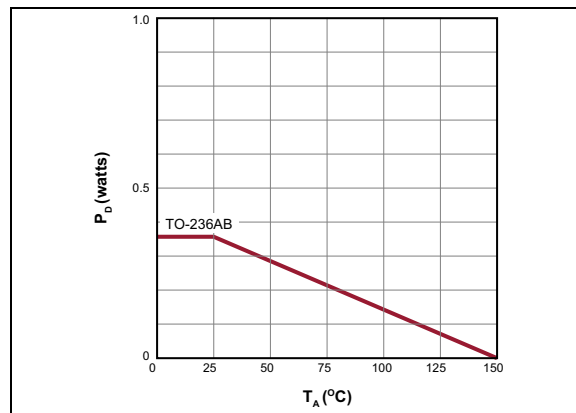


FIGURE 2-5: Power Dissipation vs. Ambient Temperature.

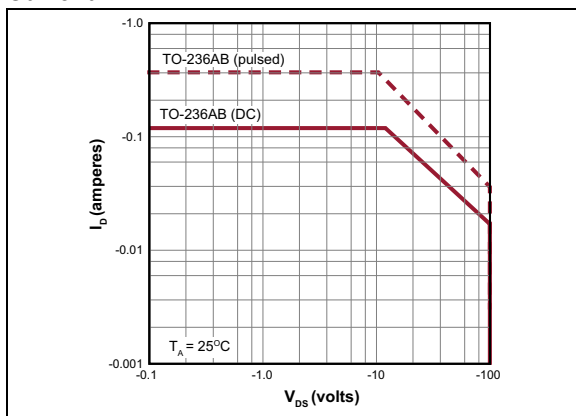


FIGURE 2-3: Maximum Rated Safe Operating Area.

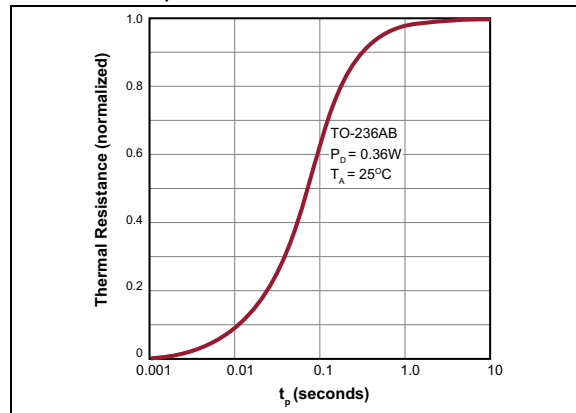


FIGURE 2-6: Thermal Response Characteristics.

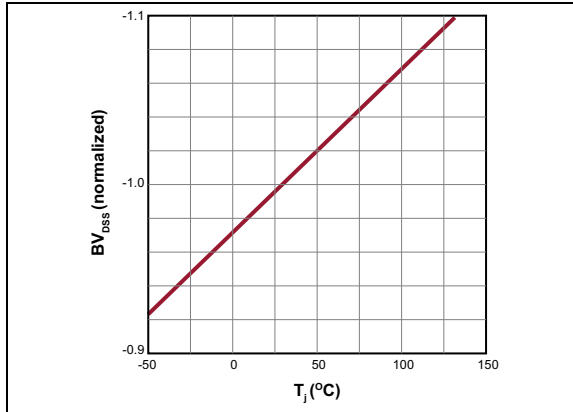


FIGURE 2-7: BV_{DSS} Variation with Temperature.

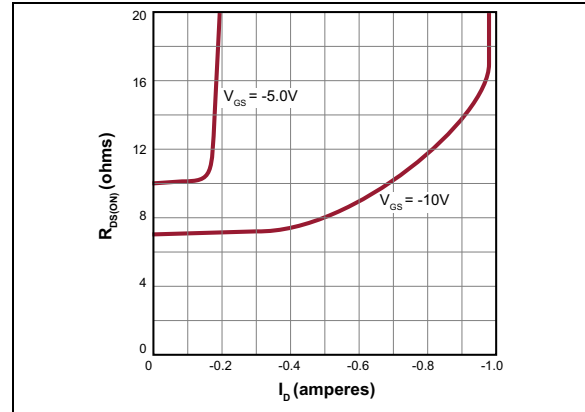


FIGURE 2-10: On-Resistance vs. Drain Current.

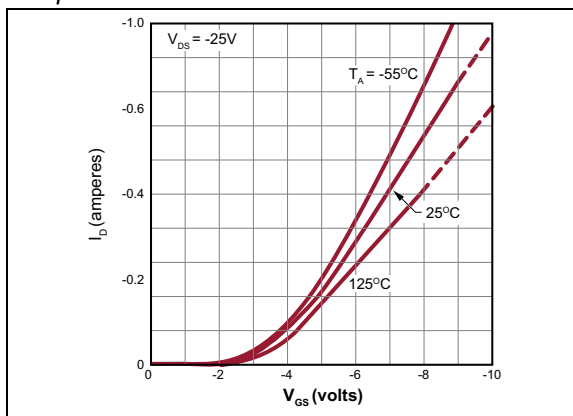


FIGURE 2-8: Transfer Characteristics.

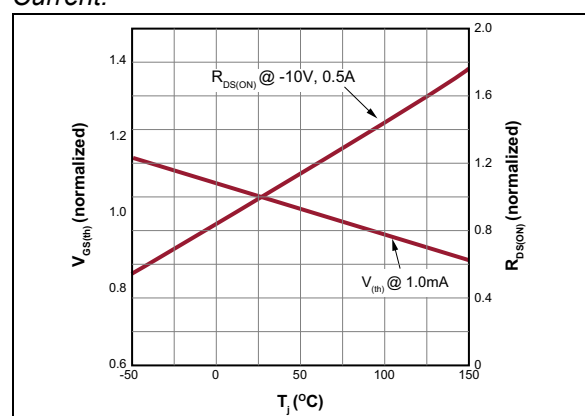


FIGURE 2-11: V_{th} and R_{DS} Variation with Temperature.

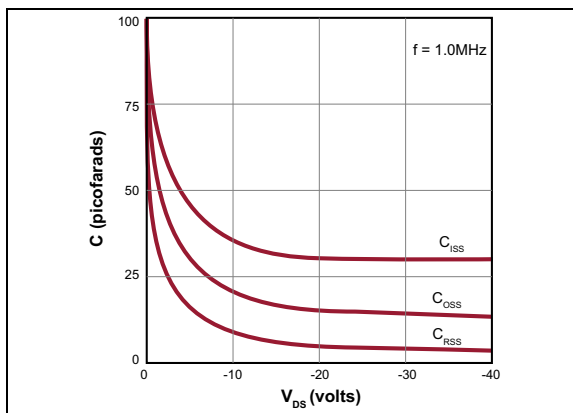


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

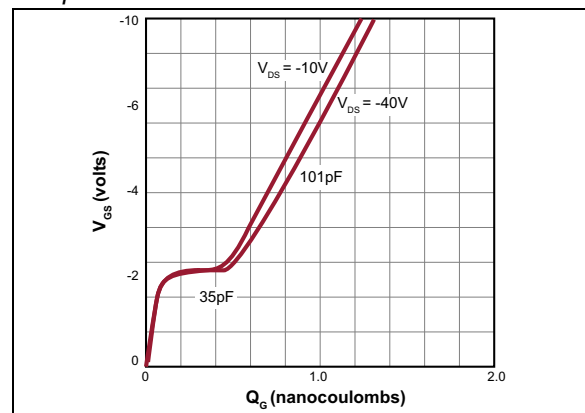


FIGURE 2-12: Gate Drive Dynamic Characteristics.

VP2110

3.0 PIN DESCRIPTION

The details on the pins of VP2110 are listed in [Table 3-1](#). Refer to [Package Type](#) for the location of pins.

TABLE 3-1: 3-LEAD SOT-23 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VP2110.

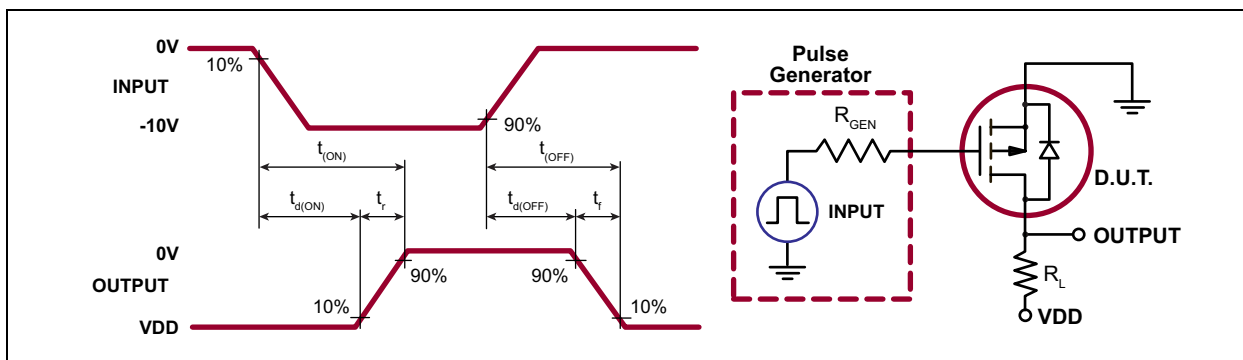


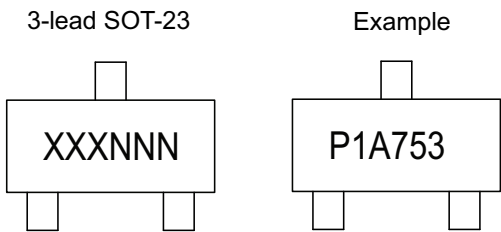
FIGURE 4-1: Switching Waveforms and Test Circuit.

TABLE 4-1: PRODUCT SUMMARY

Device	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (mA)
VP2110	-100	12	-500

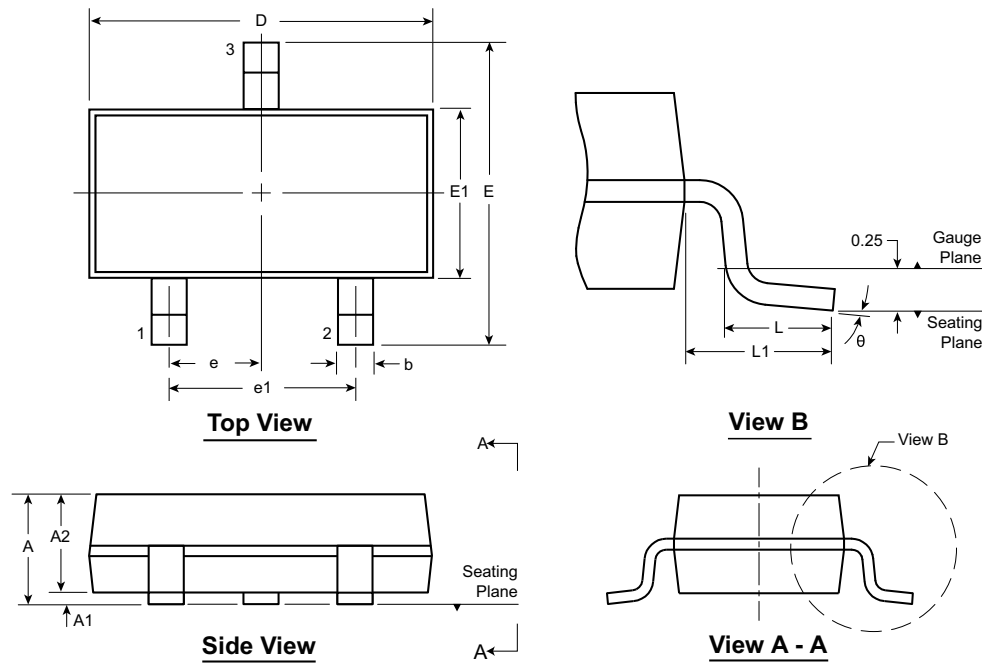
5.0 PACKAGING INFORMATION

5.1 Package Marking Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

3-Lead TO-236AB (SOT-23) Package Outline (K1/T) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2021)

- Converted Supertex Doc# DSFP-VP2110 to Microchip DS20006600A
- Changed the package marking format
- Added sections to comply with Microchip formatting standards
- Made minor text changes throughout the document

VP2110

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	VP2110	=	P-Channel Enhancement-Mode Vertical DMOS FET		
Package:	K1	=	3-lead SOT-23		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3000/Reel for a K1 Package		
Example:					
a) VP2110K1-G: P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-23, 3000/Reel					

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