



### DESCRIPTION

The MP4573 is a fully integrated, fixed-frequency, synchronous step-down converter. It can achieve up to 2.5A of continuous output current with peak current control for excellent transient response.

The wide 4.5V to 60V input voltage range accommodates a variety of step-down applications in automotive input environments. The device's 2 $\mu$ A shutdown current also makes it ideal for battery-powered applications.

The MP4573's integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively) provide high efficiency without the need for an external Schottky diode. Advanced asynchronous modulation (AAM) mode achieves high efficiency under light-load conditions by scaling down the frequency to reduce switching and gate driver losses.

Features include built-in soft start (SS), enable (EN) control, and power good (PG) indication. High duty cycle and low-dropout (LDO) mode enable the device to withstand automotive cold crank conditions.

The MP4573 employs over-current protection (OCP) with valley current detection to avoid current runaway. It also features short-circuit protection (SCP) with hiccup mode, input under-voltage lockout (UVLO), and auto-recovery thermal protection.

With internal compensation, the MP4573 offers an ultra-compact solution that requires a minimal number of readily available, standard external components. It is available in a QFN-12 (2.5mmx3mm) package.

### FEATURES

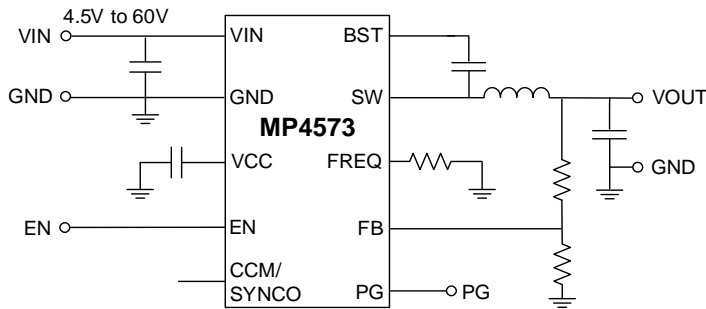
- Wide 4.5V to 60V Operating Input Range
- 2.5A Continuous Output Current
- High-Efficiency, Synchronous Mode Control
- 250m $\Omega$ /45m $\Omega$  Internal Power MOSFETs
- Up to 2.2MHz Configurable Frequency
- 180° Out-of-Phase SYNCO Clock
- 40 $\mu$ A Quiescent Current ( $I_Q$ )
- Low 2 $\mu$ A Shutdown Current
- FB Tolerance: 1% at Room Temp, 2% at across the Full Temperature Range (-40°C to +125°C)
- Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM) during Light-Load Operation
- 0.45ms Internal Soft Start (SS)
- Remote Enable (EN) Control
- Power Good (PG) Indicator
- Low-Dropout (LDO) Mode
- Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- $V_{IN}$  Under-Voltage Lockout (UVLO)
- Thermal Shutdown
- Available in a QFN-12 (2.5mmx3mm) Package
- Available in a Wettable Flank Package

### APPLICATIONS

- Infotainment Systems
- Lamps and LEDs
- Motor Controls
- Industrial Power Systems

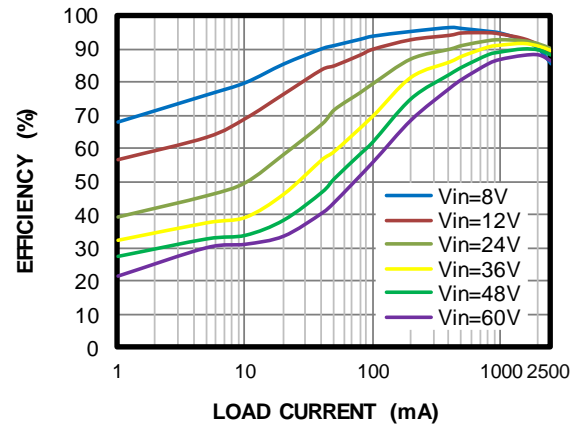
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**TYPICAL APPLICATION**



**Efficiency vs. Load Current**

$V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ , AAM



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MP4573GQBE	QFN-12 (2.5mmx3mm)	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MP4573GQBE-Z).

\*\* Moisture sensitivity level rating.

### TOP MARKING

**BQN**

**YWW**

**LLL**

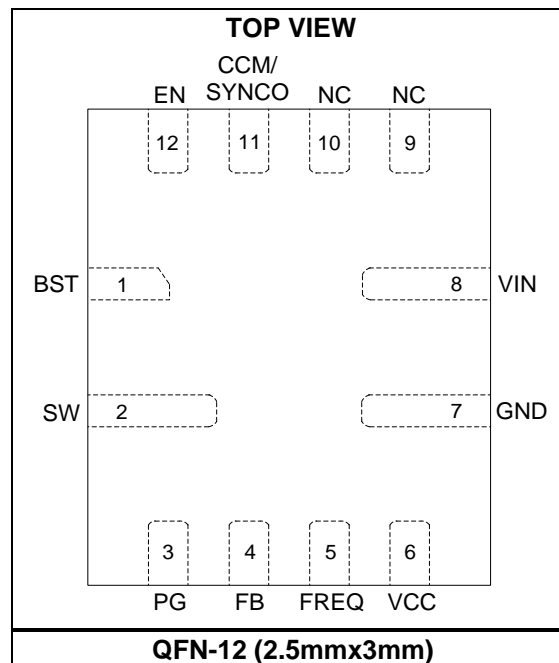
BQN: Product code

Y: Year code

WW: Week code

LLL: Lot number

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	BST	<b>Bootstrap.</b> Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
2	SW	<b>Switch output.</b> The SW pin is the output of the internal power switches.
3	PG	<b>Power good indicator.</b> The PG pin is an open drain; it requires a pull-up resistor to the power source. If the output voltage ( $V_{OUT}$ ) is between 90% and 108% of the nominal voltage, PG is pulled up to the power source. If $V_{OUT}$ exceeds 116% or drops below 84% of the nominal voltage, PG goes low.
4	FB	<b>Feedback point.</b> The FB pin is the negative input of the error amplifier (EA), and the value is typically 0.8V. To set the regulation voltage, connect FB to the tap of an external resistor divider between the output and GND. The PG and under-voltage lockout (UVLO) circuits use FB to monitor $V_{OUT}$ .
5	FREQ	<b>Configurable switching frequency (<math>f_{sw}</math>).</b> To set $f_{sw}$ , connect a resistor to ground.
6	VCC	<b>Internal bias supply.</b> The VCC pin supplies power to the internal control circuit and gate drivers. Place a 1 $\mu$ F or greater decoupling capacitor close to ground.
7	GND	<b>IC ground.</b> Connect the large copper areas to the negative terminals of the input and output capacitors.
8	VIN	<b>Input supply.</b> The VIN pin supplies power to the converter. To reduce switching spikes, place a decoupling capacitor close to ground, as close to the IC as possible.
9, 10	NC	<b>No connection.</b> To improve thermal and EMI performance, connect the NC pins to GND.
11	CCM/ SYNCO	<b>Mode selection/synchronous output.</b> To force the converter into continuous conduction mode (CCM), connect the CCM/SYNCO pin to GND via a 10k $\Omega$ to 300k $\Omega$ resistor. Float this pin to force the converter into advanced asynchronous modulation (AAM) mode under light-load conditions. CCM/SYNCO is also a synchronization output pin that can output a 180° out-of-phase clock to other devices.
12	EN	<b>Enable.</b> Drive the EN pin above 1.45V to turn the converter on; float EN or drive it below 1.12V to turn the converter off.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

$V_{IN}$ .....	65V
$V_{SW}$ .....	-0.3V to $V_{IN} + 0.3V$
$V_{BST}$ .....	$V_{SW} + 6V$
All other pins .....	-0.3V to +6V
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>	
QFN-12 (2.5mmx3mm) .....	2.08W
Junction temperature .....	150°C
Lead temperature .....	260°C
Storage temperature .....	-65°C to +150°C

**ESD Ratings**

Human body model (HBM) .....	±2kV
Charged device model (CDM) .....	±750V

**Recommended Operating Conditions**

Continuous supply voltage ( $V_{IN}$ ) .....	4.5V to 60V
Output voltage ( $V_{OUT}$ ) .....	1V to 90% of $V_{IN}$
Load current range .....	0A to 2.5A
Operating junction temp ( $T_J$ ) ....	-40°C to +125°C

<b>Thermal Resistance</b>	$\theta_{JA}$	$\theta_{JC}$
QFN-12 (2.5mmx3mm)		
JESD51-7 <sup>(3)</sup> .....	60.....	13....°C/W
EVQ4573-QB-00A <sup>(4)</sup> .....	45.....	11....°C/W

**Notes:**

- 1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the module may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- 4) Measured on MPS standard evaluation board (8.9cmx8.9cm), thick 2oz copper, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(5)</sup>, typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Input Supply and Under-Voltage Lockout (UVLO)</b>						
Quiescent supply current	$I_Q$	No load, $V_{FB} = 0.85V$ , AAM		40	65	$\mu A$
Shutdown supply current	$I_{SD}$	$V_{EN} = 0V$		2	5	$\mu A$
$V_{IN}$ UVLO rising threshold	$V_{IN\_UV\_RISING}$		3.8	4	4.2	V
$V_{IN}$ UVLO falling threshold	$V_{IN\_UV\_FALLING}$		3.3	3.5	3.7	V
$V_{IN}$ UVLO threshold hysteresis	$V_{IN\_UV\_HYS}$			500		mV
<b>Output and Regulation</b>						
Feedback (FB) reference voltage	$V_{REF}$	$T_J = 25^{\circ}C$	0.792	0.8	0.808	V
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	0.784		0.816	V
FB input current	$I_{FB}$	$V_{FB} = 0.85V$		10	50	nA
<b>Switches and Frequency</b>						
HS-FET on resistance	$R_{DS(ON)\_HS}$	$V_{BST} - V_{SW} = 5V$ , $T_J = 25^{\circ}C$	150	250	350	m $\Omega$
		$V_{BST} - V_{SW} = 5V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$	100		500	
LS-FET on resistance	$R_{DS(ON)\_LS}$	$T_J = 25^{\circ}C$	30	45	60	m $\Omega$
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	20		90	
SW leakage current	$I_{SW\_LKG}$	$V_{EN} = 0V$ , $V_{SW} = 0V$ or $60V$		0.1	30	$\mu A$
Switching frequency	$f_{SW}$	$R_{FREQ} = 76.8k\Omega$	300	400	500	kHz
		$R_{FREQ} = 28k\Omega$	750	1000	1250	kHz
		$R_{FREQ} = 12.1k\Omega$	1800	2200	2700	kHz
Minimum on time <sup>(6)</sup>	$t_{ON\_MIN}$			90		ns
Minimum off time <sup>(6)</sup>	$t_{OFF\_MIN}$			100		ns
<b>Power Good (PG)</b>						
PG current sink	$V_{PG\_SINK}$	Sink 4mA			300	mV
PG delay time	$t_{PG\_DELAY}$	Rising edge		70		$\mu s$
		Falling edge		25		$\mu s$
PG leakage current	$I_{PG\_LKG}$			10	1000	nA
PG rising threshold ( $V_{FB} / V_{REF}$ )	$PG_{RISING}$	$V_{FB}$ rising		90		%
		$V_{FB}$ falling		108		%
PG falling threshold ( $V_{FB} / V_{REF}$ )	$PG_{FALLING}$	$V_{FB}$ falling		84		%
		$V_{FB}$ rising		116		%
<b>Enable (EN)</b>						
EN rising threshold	$V_{EN\_RISING}$		1.38	1.45	1.52	V
EN falling threshold	$V_{EN\_FALLING}$		1.05	1.12	1.19	V
EN threshold hysteresis	$V_{EN\_HYS}$			330		mV
EN input current	$I_{EN}$	$V_{EN} = 2V$		0.7		$\mu A$
EN turn-off delay	$t_{EN\_DELAY}$		5			$\mu s$
<b>Bootstrap (BST)</b>						
(BST - SW) UVLO				1.4	2.5	V
(BST - SW) UVLO hysteresis				60		mV
<b>Soft Start (SS) and VCC</b>						
Soft-start time	$t_{SS}$			0.45		ms
VCC regulator	$V_{CC}$	$I_{CC} = 0mA$	4.6	4.9	5.2	V

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(5)</sup>, typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Protections</b>						
Peak current limit threshold	$I_{PEAK\_LIMIT}$	20% duty cycle	3	3.9	5.4	A
Valley current limit threshold	$I_{VALLEY\_LIMIT}$		3			A
Zero-current detection (ZCD) threshold	$I_{ZCD}$	AAM	-100	140	+300	mA
Negative current limit threshold	$I_{NEG\_LIMIT}$	FCCM	-2	-1.3	-0.8	A
Thermal shutdown <sup>(6)</sup>	$T_{SD}$	Rising temperature		170		$^{\circ}C$
Thermal shutdown hysteresis <sup>(6)</sup>	$T_{SD\_SYS}$			25		$^{\circ}C$

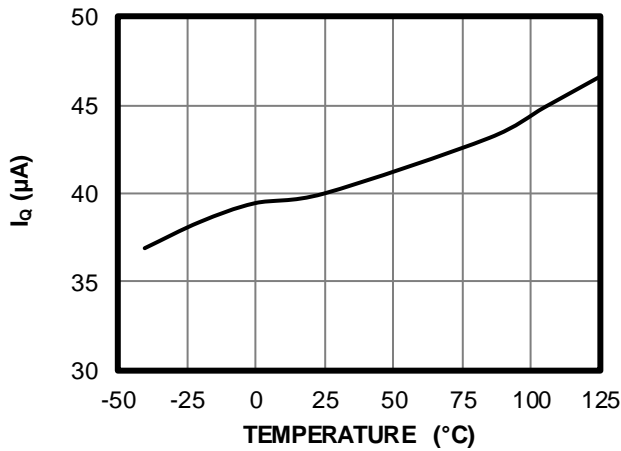
**Notes:**

- 5) Not tested in production. Guaranteed by over-temperature correlation.  
 6) Derived from bench characterization. Not tested in production.

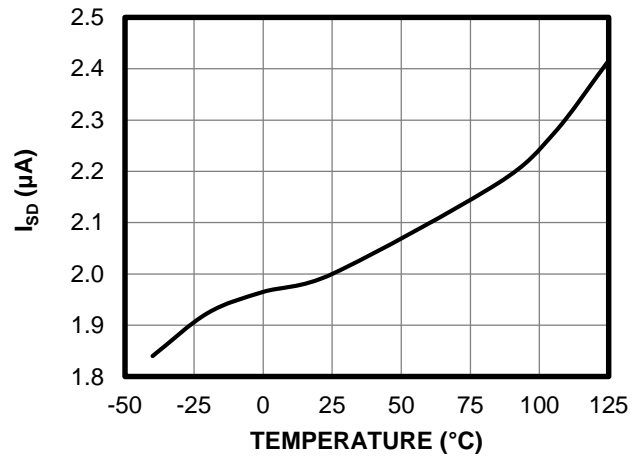
## TYPICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

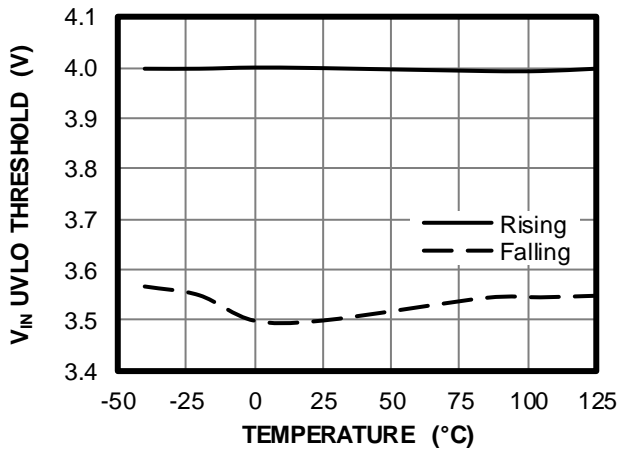
**Quiescent Current vs. Temperature**



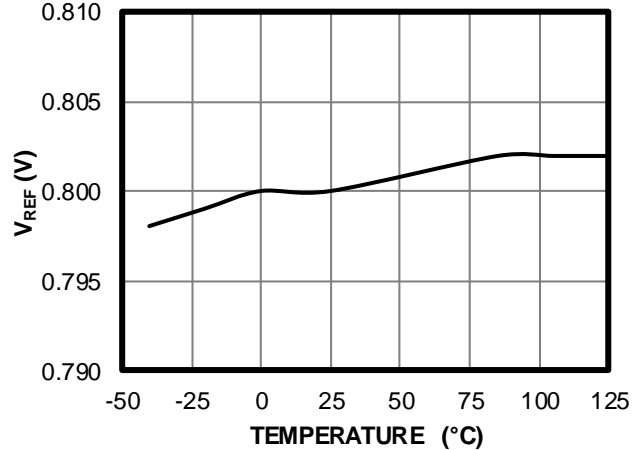
**Shutdown Current vs. Temperature**



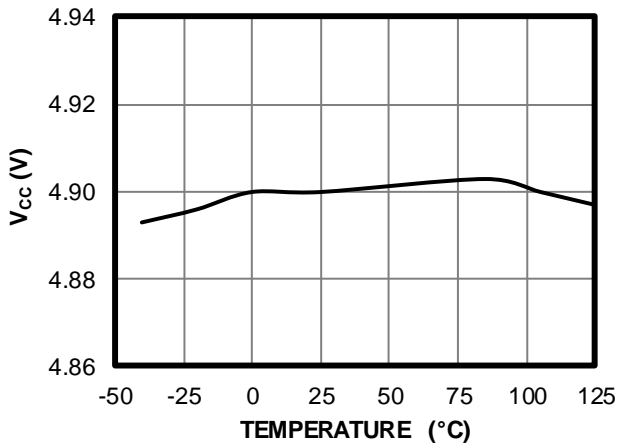
**$V_{IN}$  UVLO Threshold vs. Temperature**



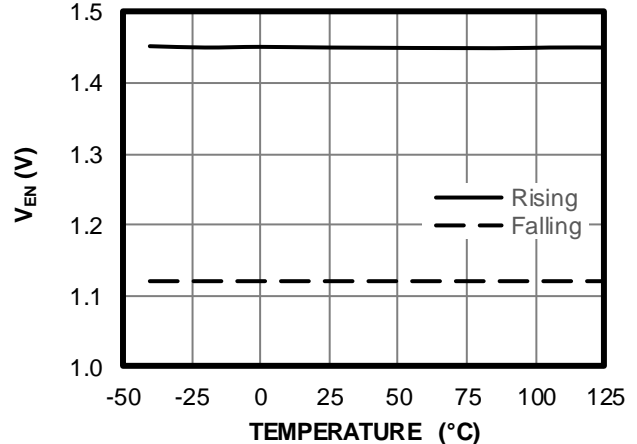
**Feedback Reference Voltage vs. Temperature**



**$V_{CC}$  vs. Temperature**

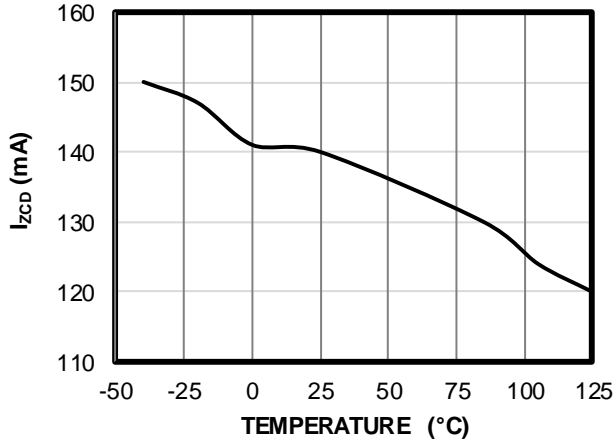
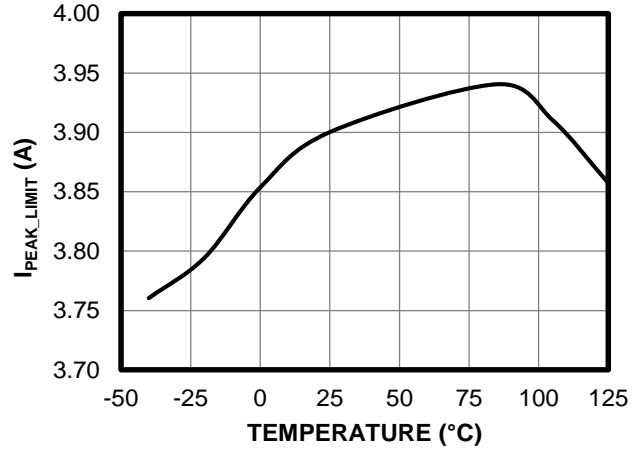
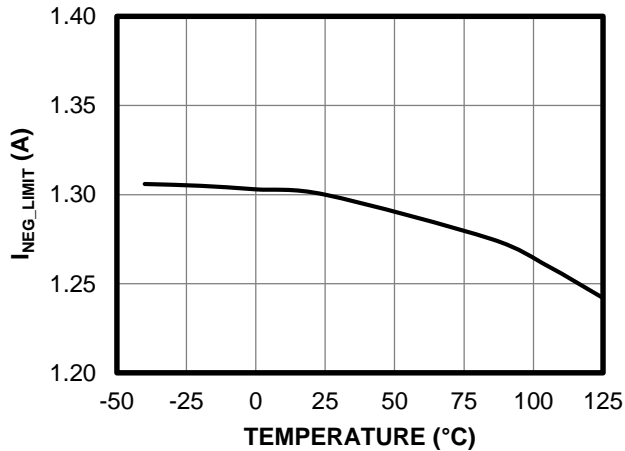
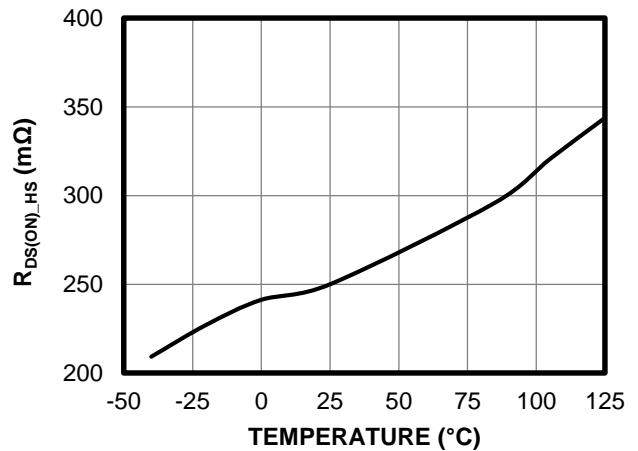
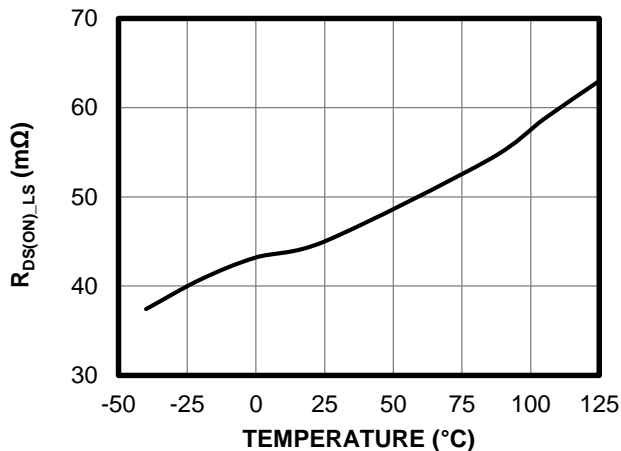
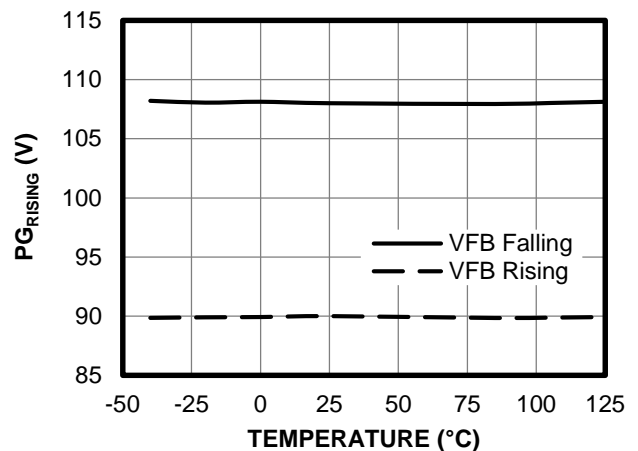


**EN Threshold vs. Temperature**





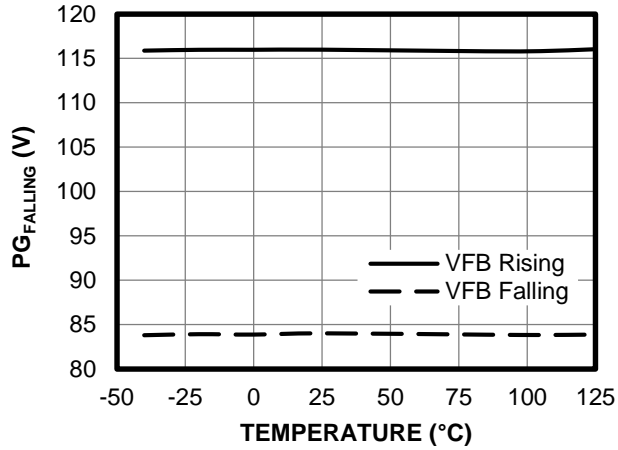
**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 24V, T_J = -40^{\circ}C \text{ to } +125^{\circ}C$ , unless otherwise noted.

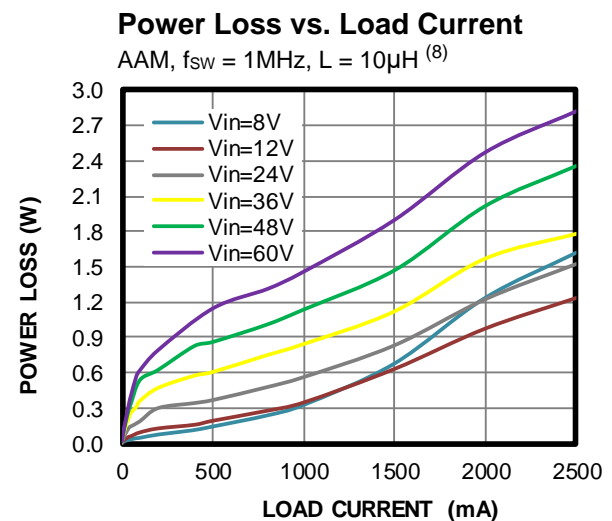
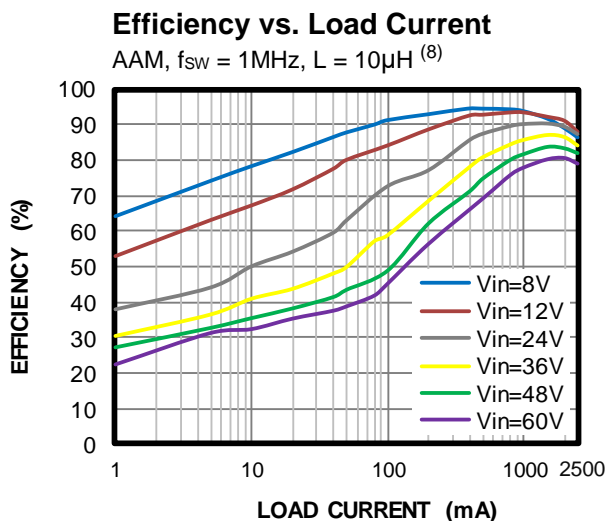
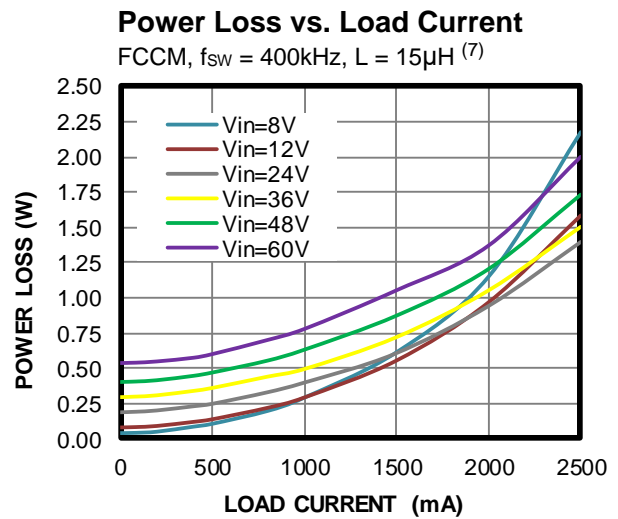
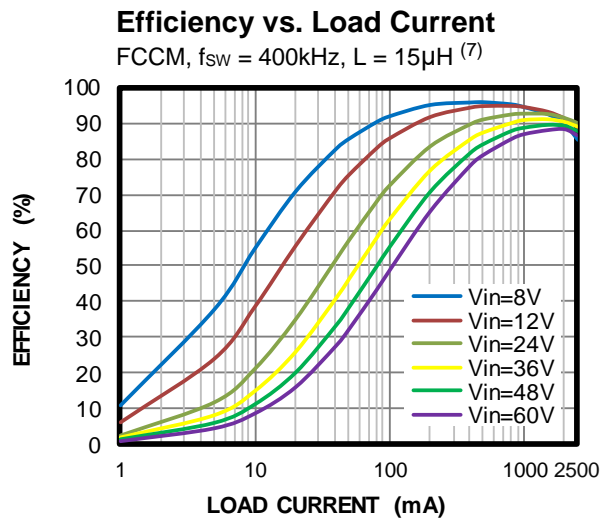
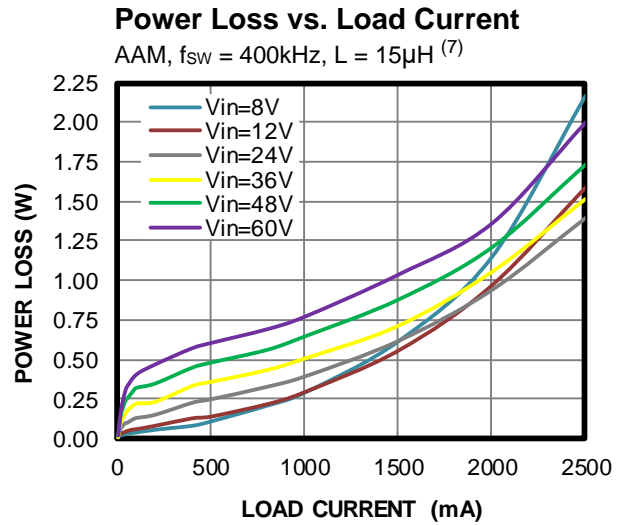
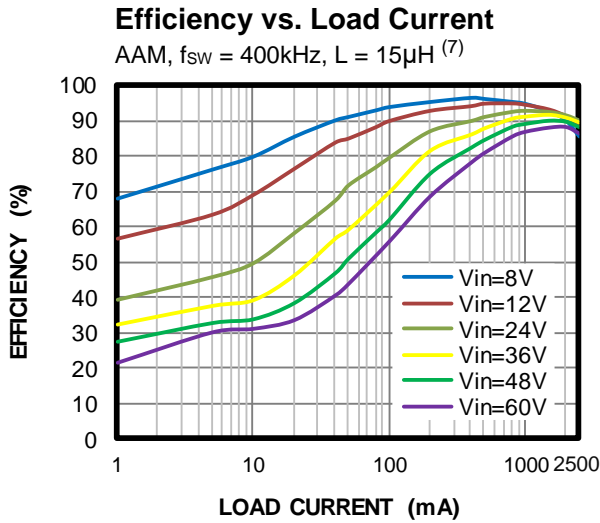
**ZCD Threshold vs. Temperature**

**Peak Current Limit vs. Temperature**

**Negative Current Limit vs. Temperature**

**HS-FET On Resistance vs. Temperature**

**LS-FET On Resistance vs. Temperature**

**PG Rising Threshold vs. Temperature**


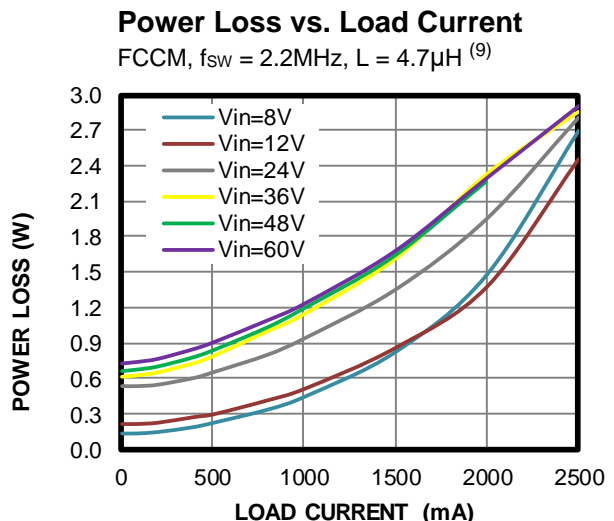
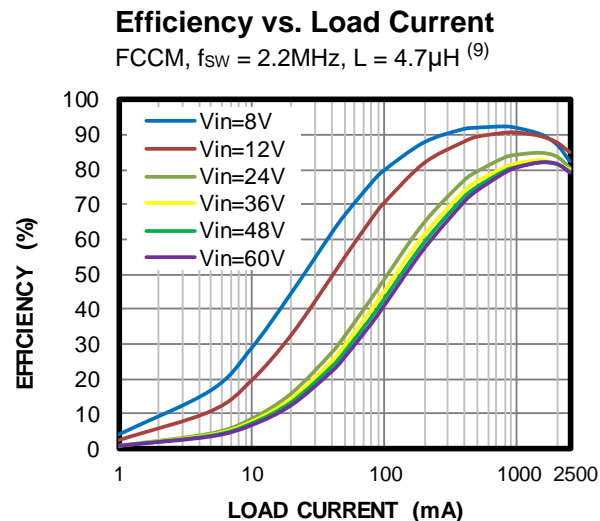
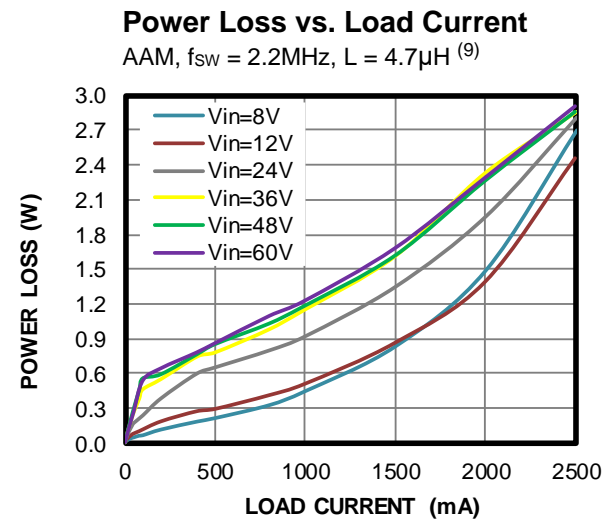
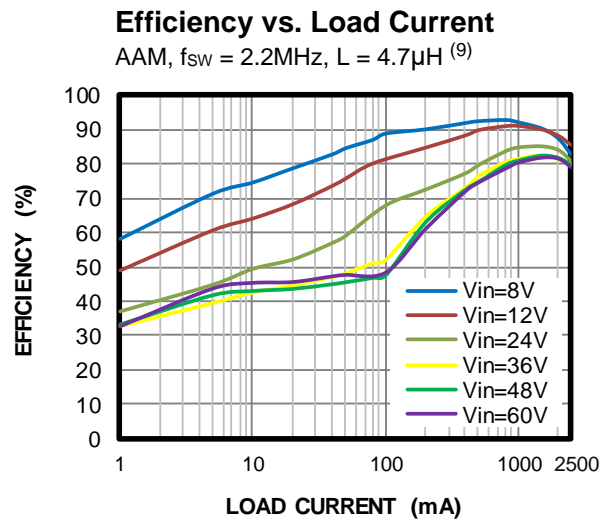
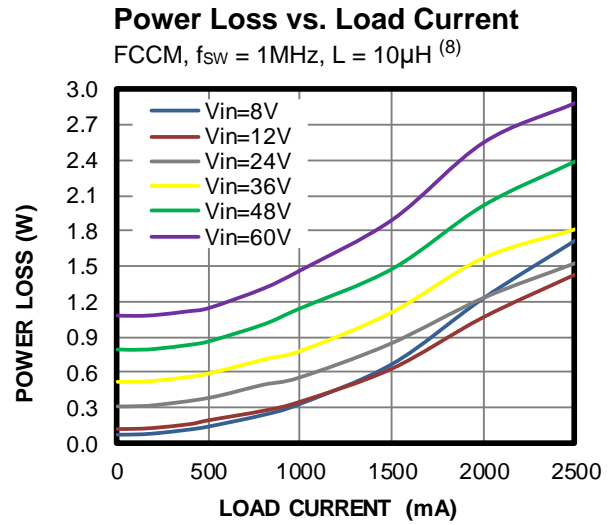
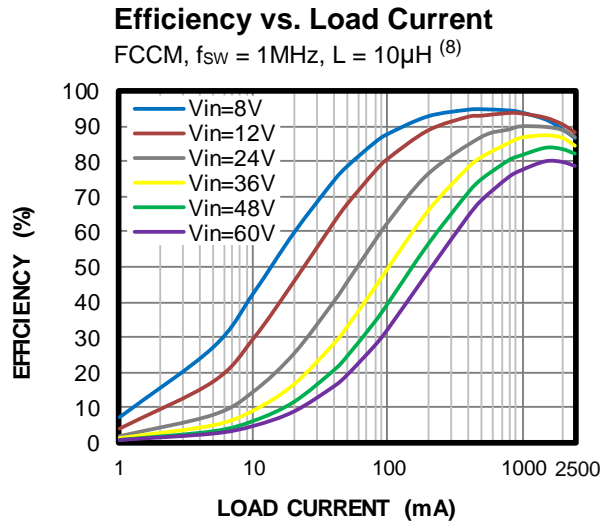
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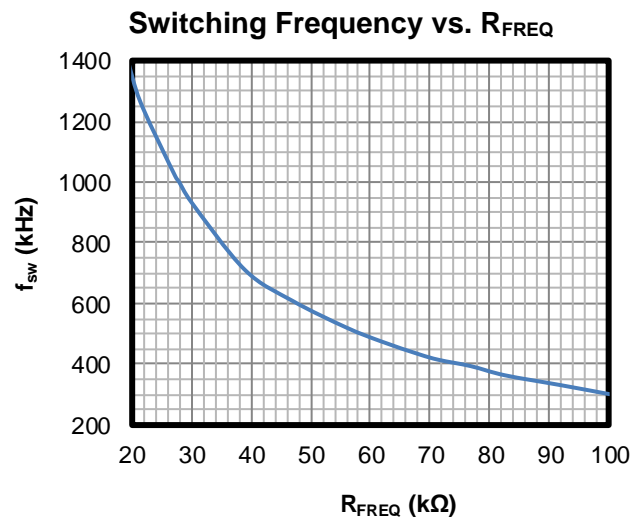
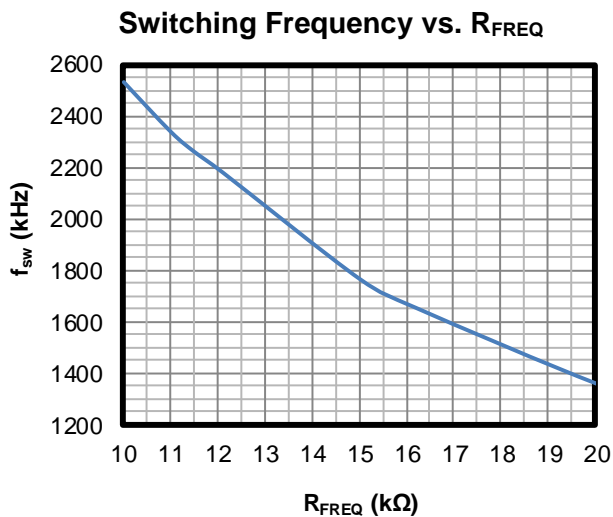
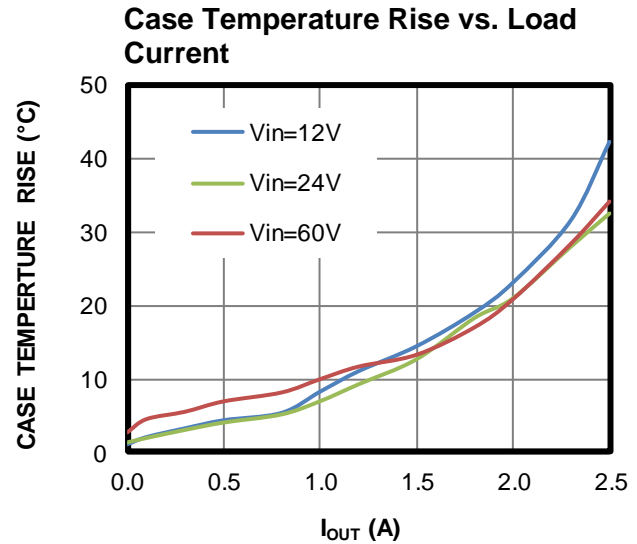
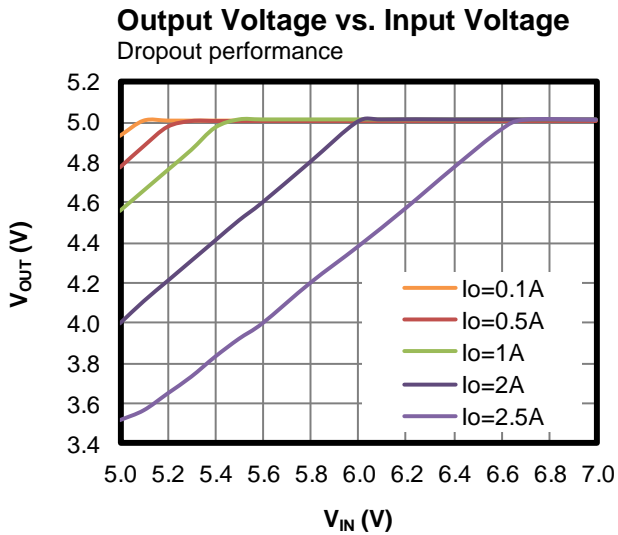
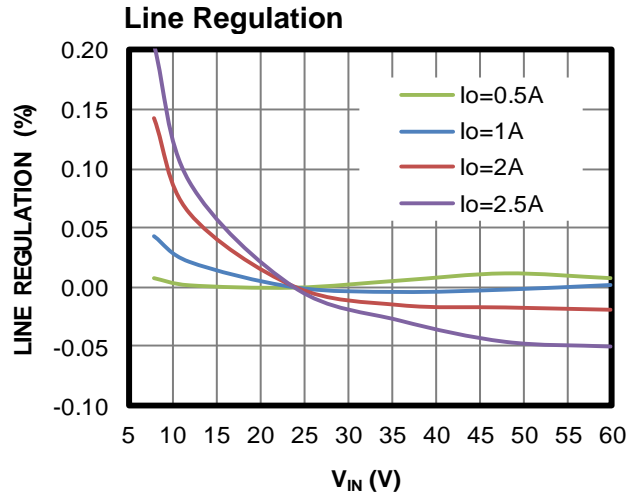
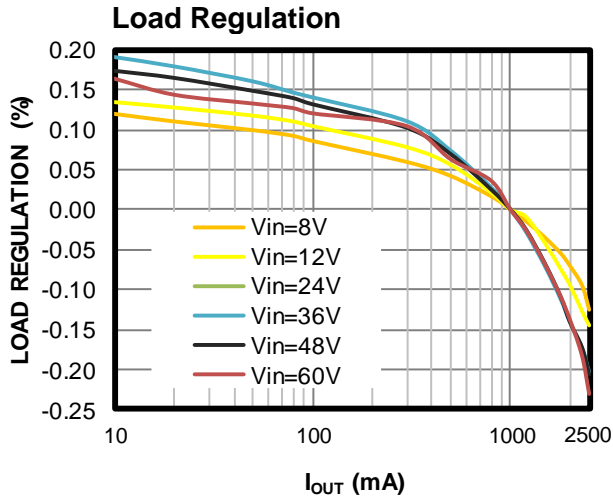
$V_{IN} = 24V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

PG Falling Threshold vs. Temperature

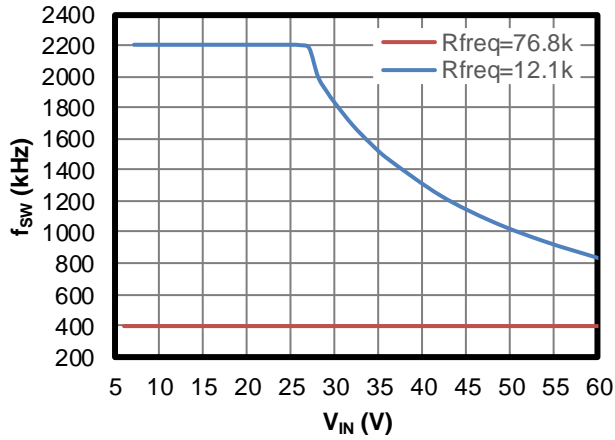


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V, V_{OUT} = 5V, L = 15\mu H, f_{SW} = 400kHz, T_A = 25^\circ C$ , unless otherwise noted.


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{SW} = 400kHz$ , AAM,  $T_A = 25^\circ C$ , unless otherwise noted.


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{SW} = 400kHz$ , AAM,  $T_A = 25^\circ C$ , unless otherwise noted.

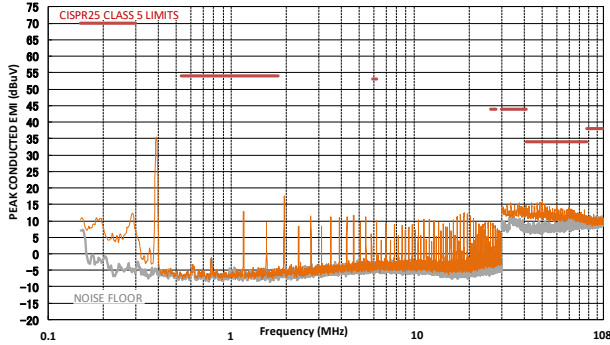
**Switching Frequency vs. Input Voltage**

**Notes:**

- 7) Inductor PN: XAL6060-153MEB/C; DCR = 43.75mΩ.
- 8) Inductor PN: XAL6060-103MEB/C; DCR = 29.82mΩ.
- 9) Inductor PN: XAL5030-472MEB/C; DCR = 36mΩ.

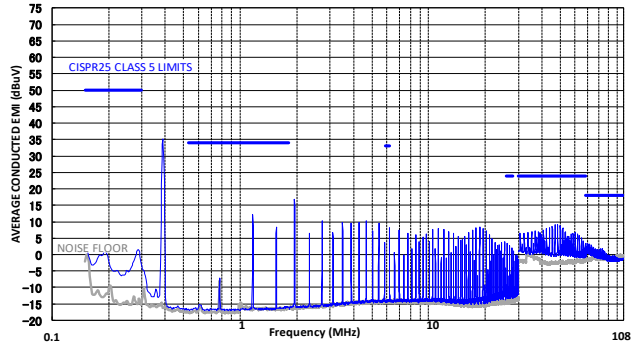
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 2.5A$ ,  $L = 10\mu H$ ,  $f_{SW} = 400kHz$ , AAM,  $T_A = 25^\circ C$ , unless otherwise noted.

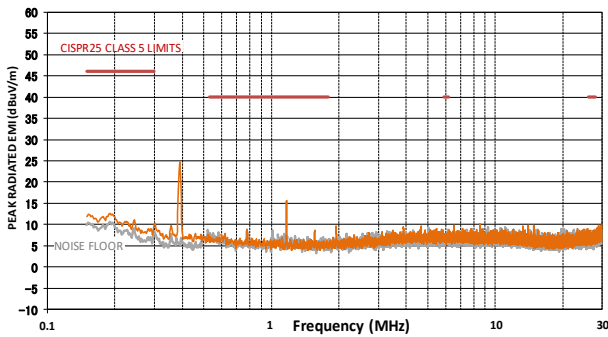
**CISPR25 Class 5 Peak Conducted Emissions** <sup>(10)</sup>  
150kHz to 108MHz



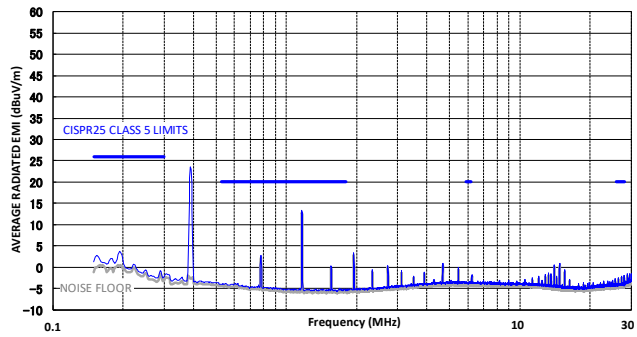
**CISPR25 Class 5 Average Conducted Emissions** <sup>(10)</sup>  
150kHz to 108MHz



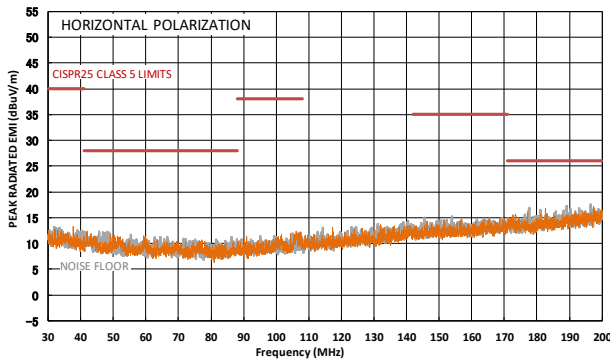
**CISPR25 Class 5 Peak Radiated Emissions** <sup>(10)</sup>  
150kHz to 30MHz



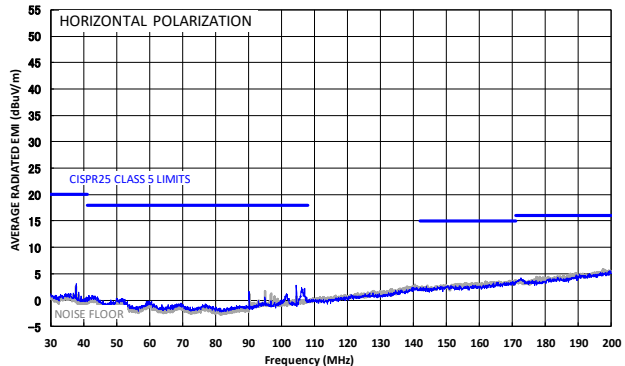
**CISPR25 Class 5 Average Radiated Emissions** <sup>(10)</sup>  
150kHz to 30MHz



**CISPR25 Class 5 Peak Radiated Emissions** <sup>(10)</sup>  
Horizontal, 30MHz to 200MHz



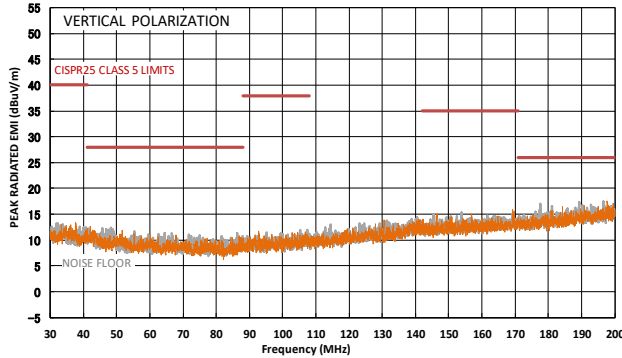
**CISPR25 Class 5 Average Radiated Emissions** <sup>(10)</sup>  
Horizontal, 30MHz to 200MHz



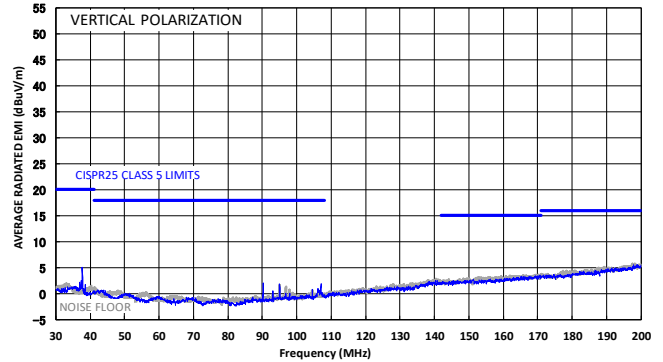
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 2.5A$ ,  $L = 10\mu H$ ,  $f_{SW} = 400kHz$ , AAM,  $T_A = 25^\circ C$ , unless otherwise noted.

**CISPR25 Class 5 Peak Radiated Emissions <sup>(10)</sup>**

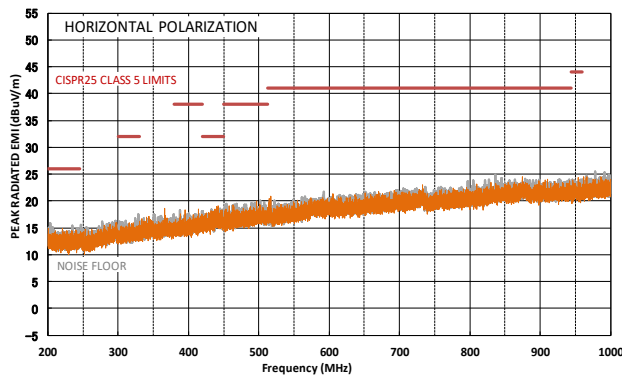
Vertical, 30MHz to 200MHz


**CISPR25 Class 5 Average Radiated Emissions <sup>(10)</sup>**

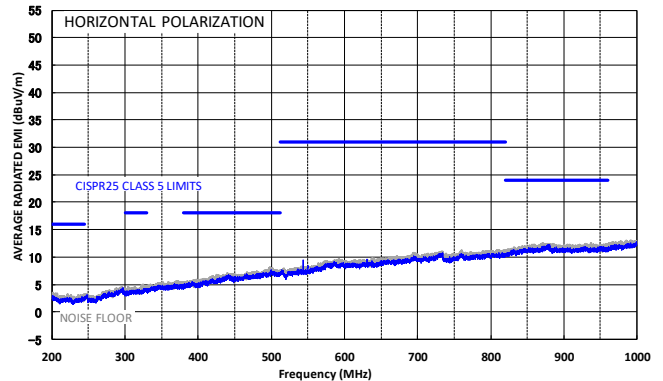
Vertical, 30MHz to 200MHz


**CISPR25 Class 5 Peak Radiated Emissions <sup>(10)</sup>**

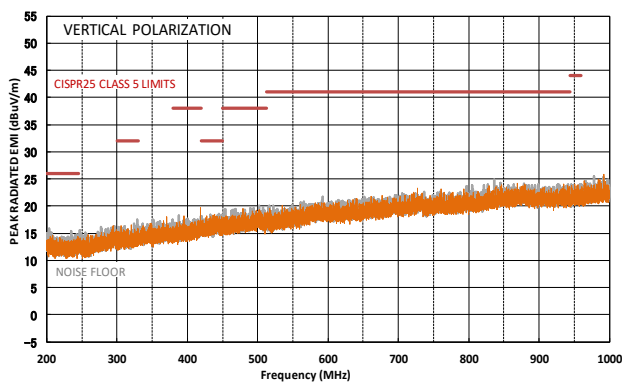
Horizontal, 200MHz to 1GHz


**CISPR25 Class 5 Average Radiated Emissions <sup>(10)</sup>**

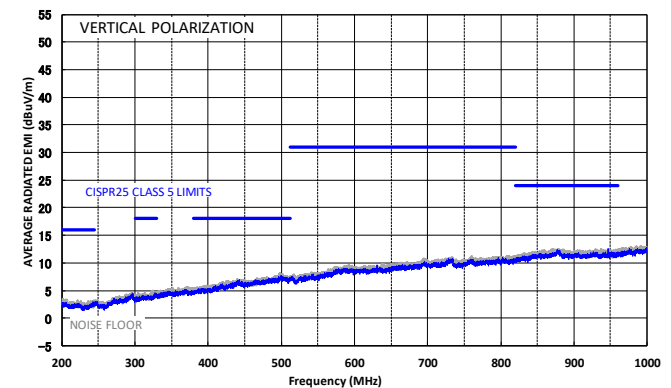
Horizontal, 200MHz to 1GHz


**CISPR25 Class 5 Peak Radiated Emissions <sup>(10)</sup>**

Vertical, 200MHz to 1GHz


**CISPR25 Class 5 Average Radiated Emissions <sup>(10)</sup>**

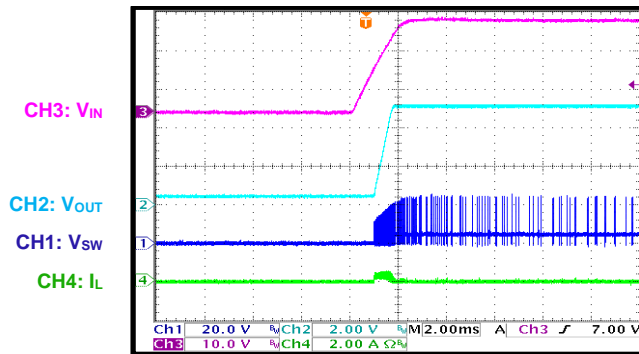
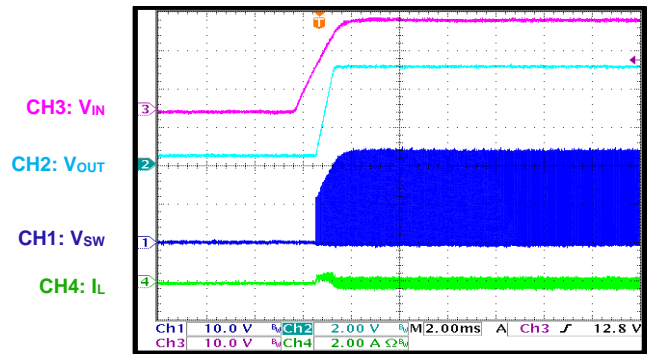
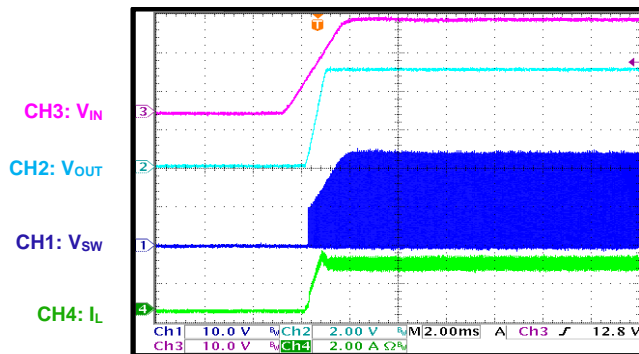
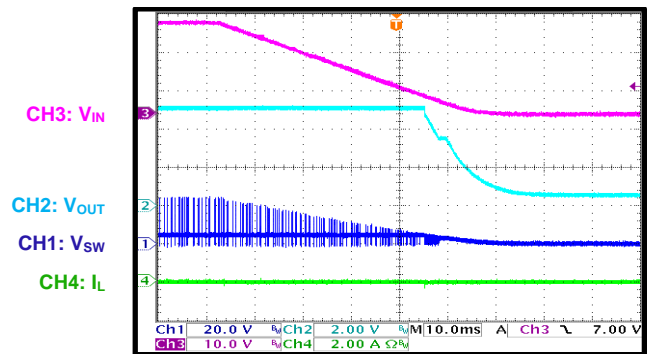
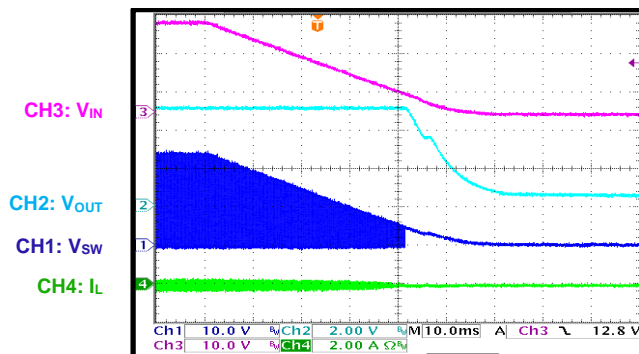
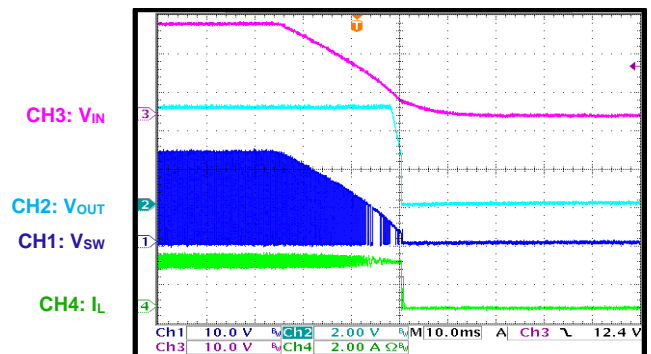
Vertical, 200MHz to 1GHz


**Note:**

10) EMC test results are based on the typical application circuit with an EMI filter (see Figure 9 on page 31), and are tested on the EV4573-QB-00A evaluation board. The inductor used for EMI testing is XAL4040-103MEB.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

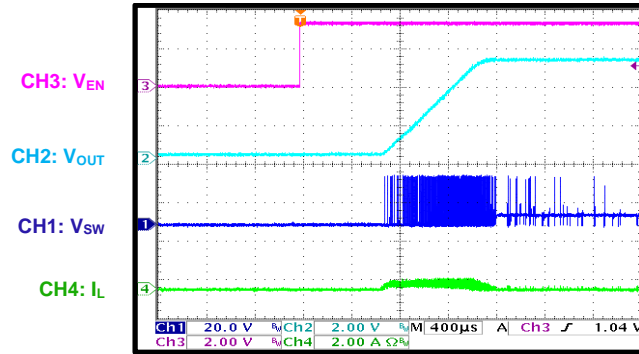
**Start-Up through VIN**
 $I_{OUT} = 0A$ , AAM

**Start-Up through VIN**
 $I_{OUT} = 0A$ , FCCM

**Start-Up through VIN**
 $I_{OUT} = 2.5A$ 

**Shutdown through VIN**
 $I_{OUT} = 0A$ , AAM

**Shutdown through VIN**
 $I_{OUT} = 0A$ , FCCM

**Shutdown through VIN**
 $I_{OUT} = 2.5A$ 


### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

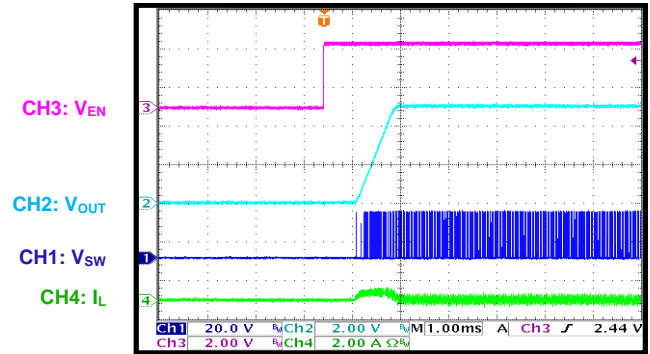
**Start-Up through EN**

$I_{OUT} = 0A$ , AAM



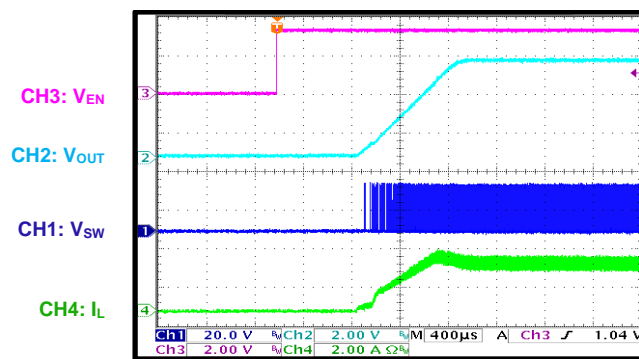
**Start-Up through EN**

$I_{OUT} = 0A$ , FCCM



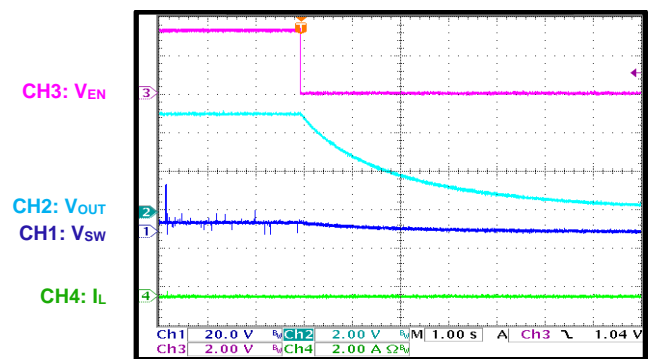
**Start-Up through EN**

$I_{OUT} = 2.5A$



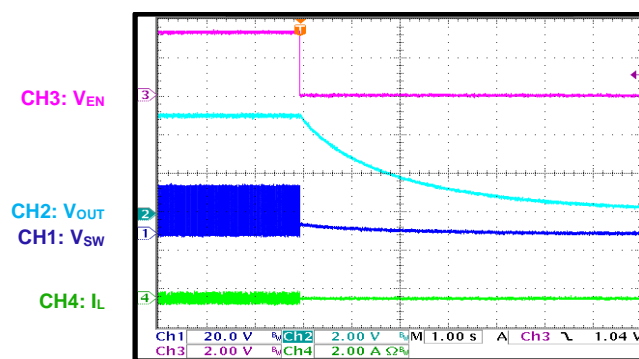
**Shutdown through EN**

$I_{OUT} = 0A$ , AAM



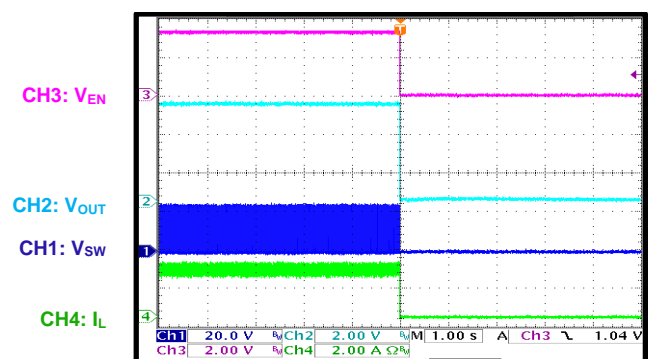
**Shutdown through EN**

$I_{OUT} = 0A$ , FCCM

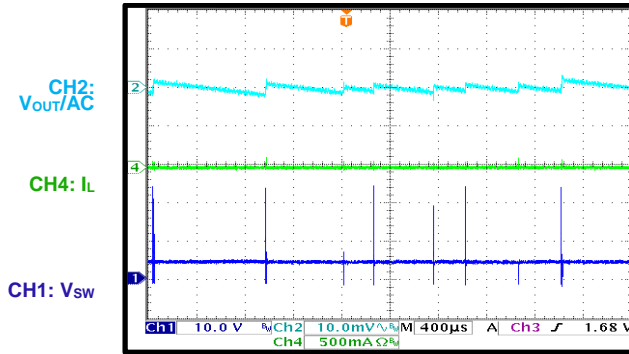
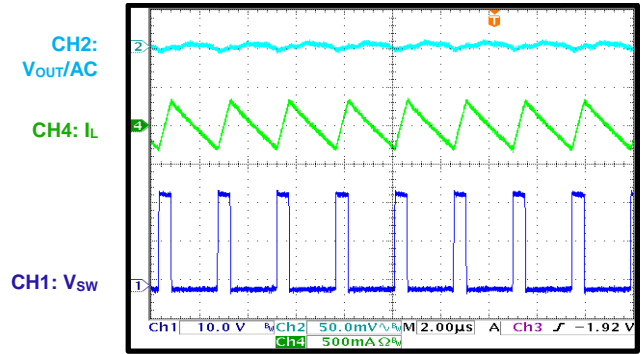
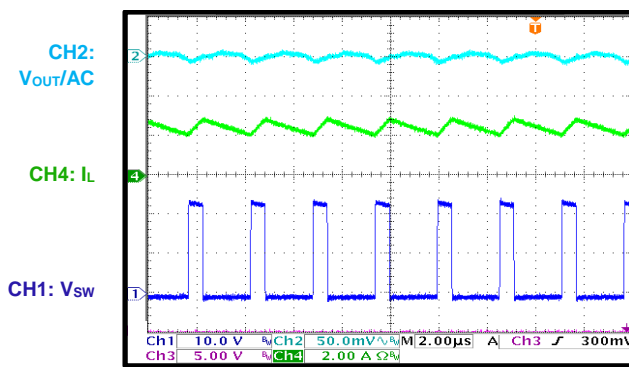
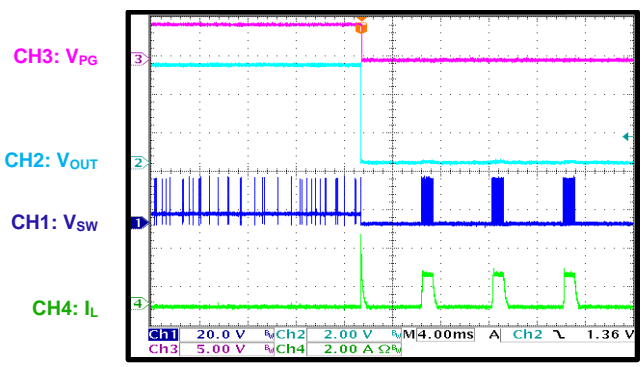
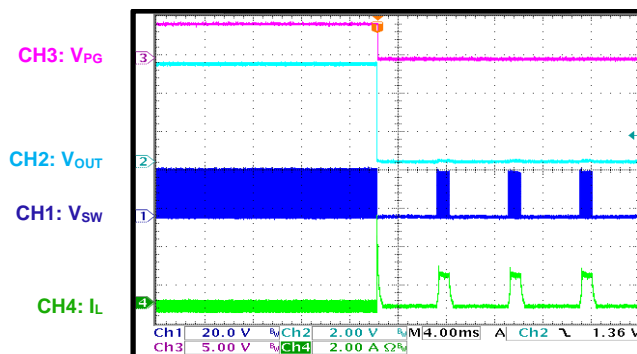
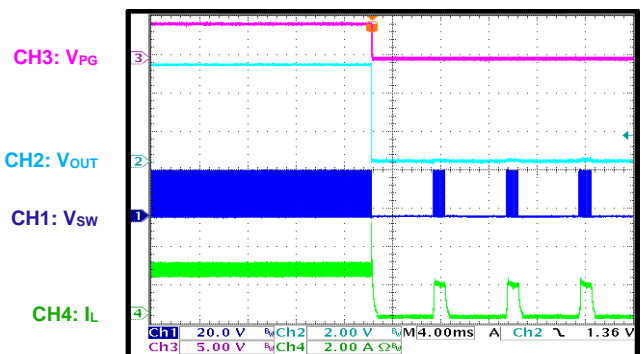


**Shutdown through EN**

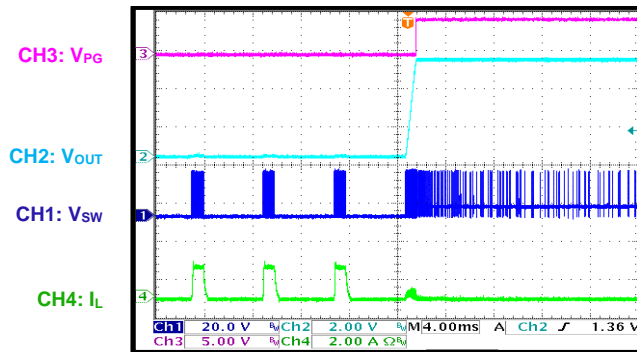
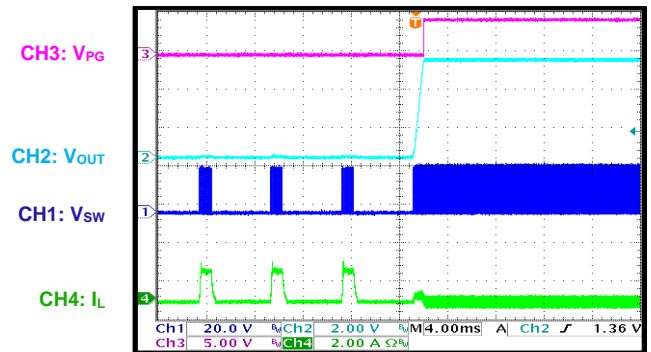
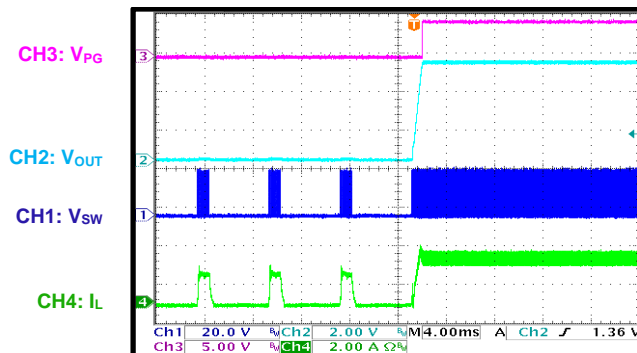
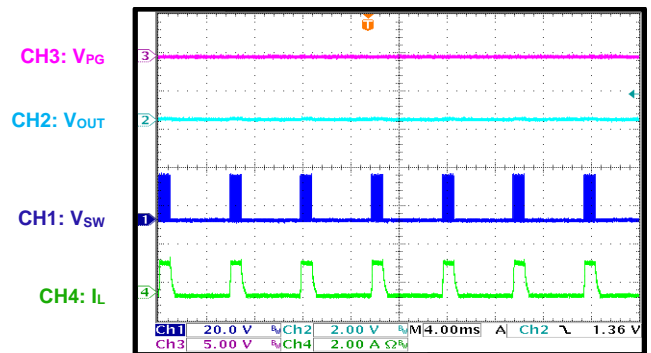
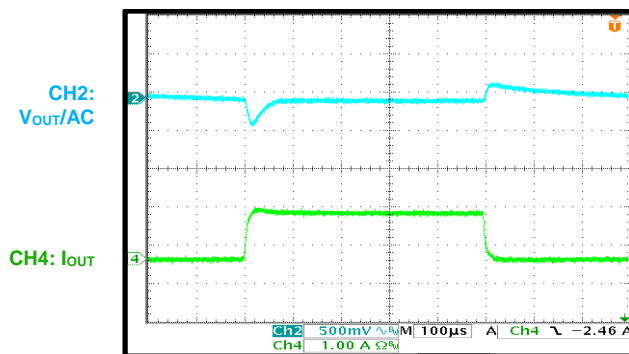
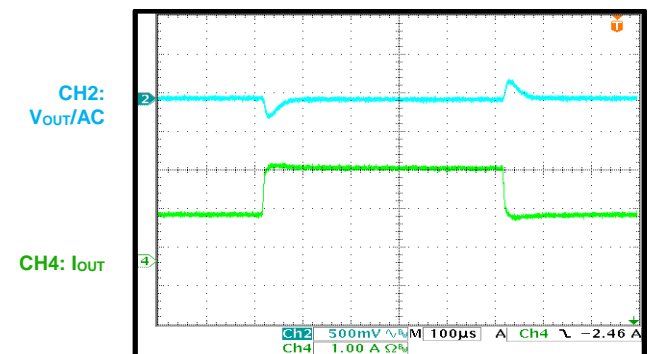
$I_{OUT} = 2.5A$



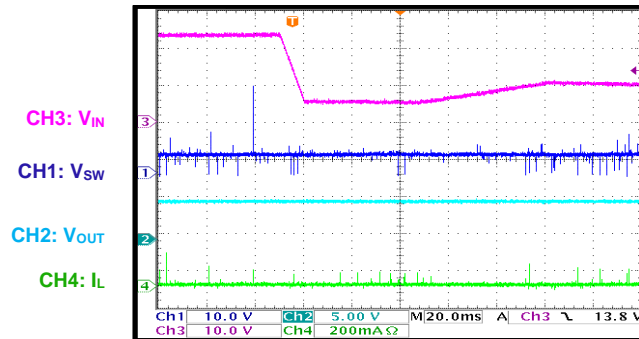
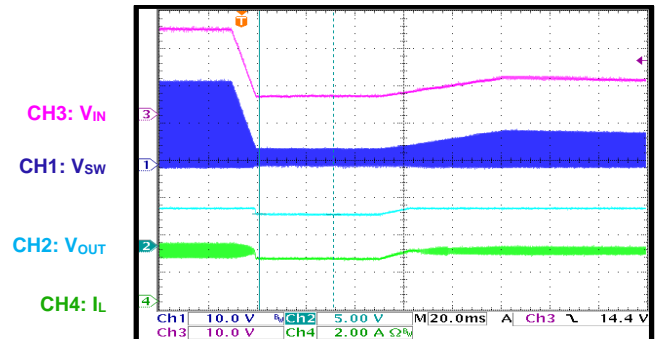
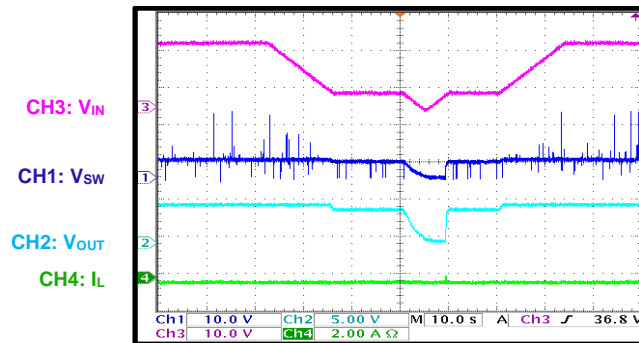
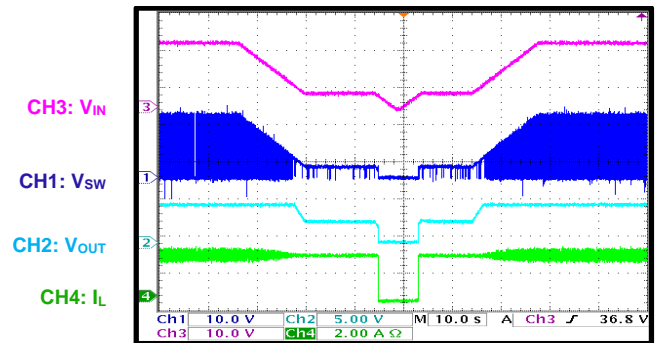
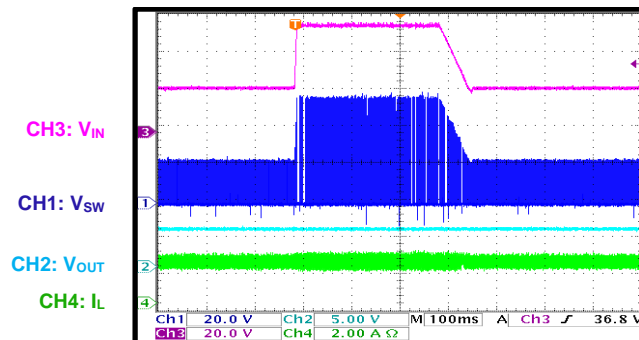
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V, V_{OUT} = 5V, L = 15\mu H, f_{sw} = 400kHz, T_A = 25^\circ C$ , unless otherwise noted.

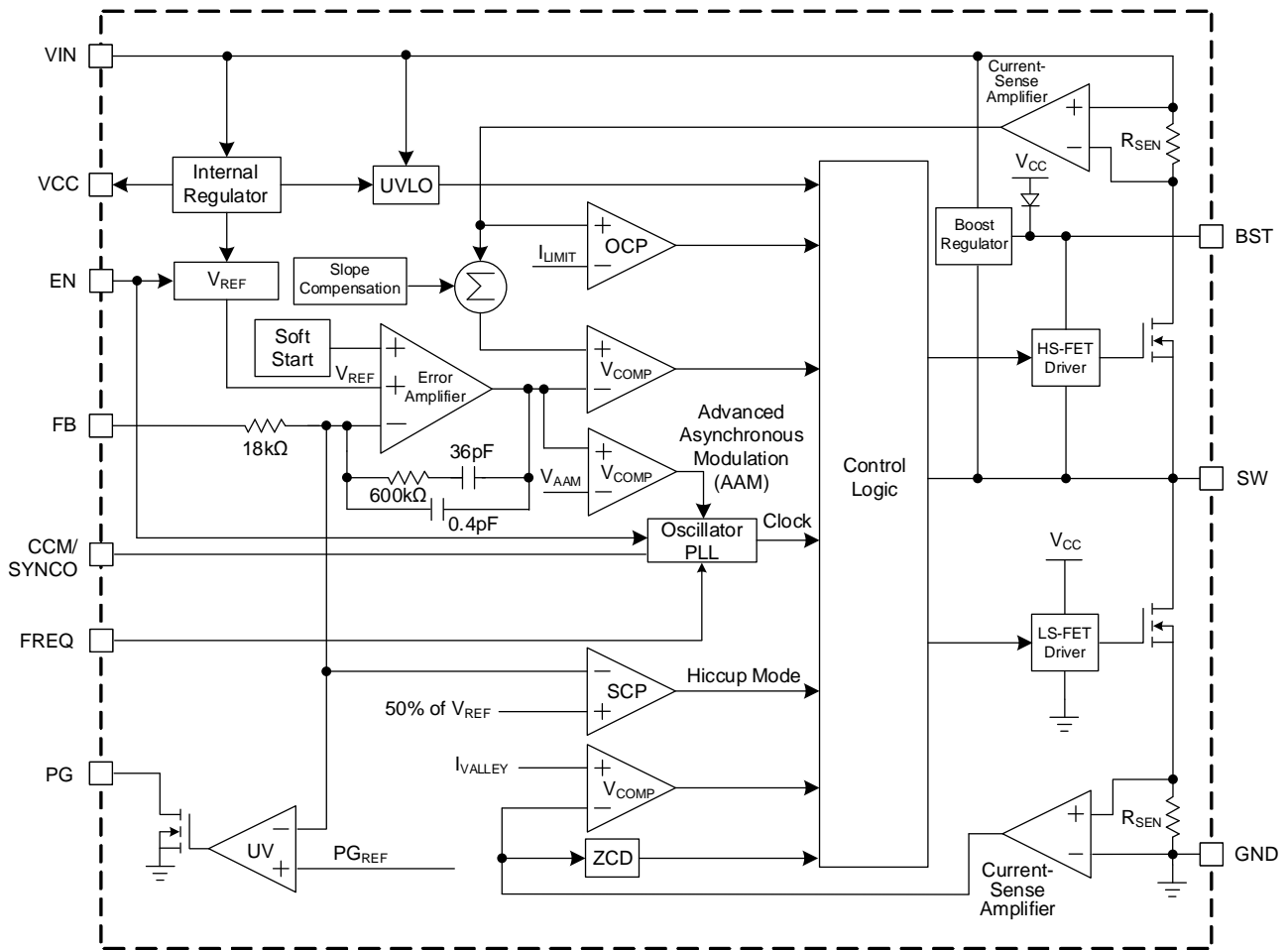
**Output Ripple**
 $I_{OUT} = 0A, AAM$ 

**Output Ripple**
 $I_{OUT} = 0A, FCCM$ 

**Output Ripple**
 $I_{OUT} = 2.5A$ 

**SCP Entry**
 $I_{OUT} = 0A, AAM$ 

**SCP Entry**
 $I_{OUT} = 0A, FCCM$ 

**SCP Entry**
 $I_{OUT} = 2.5A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**SCP Recovery**
 $I_{OUT} = 0A$ , AAM

**SCP Recovery**
 $I_{OUT} = 0A$ , FCCM

**SCP Recovery**
 $I_{OUT} = 2.5A$ 

**SCP Steady State**

**Load Transient**
 $I_{OUT} = 0A$  to  $1.5A$ , AAM

**Load Transient**
 $I_{OUT} = 1A$  to  $2.5A$ , AAM


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $L = 15\mu H$ ,  $f_{sw} = 400kHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Cold Crank**
 $V_{IN} = 24V$  to  $6V$  to  $10V$ ,  $I_{OUT} = 0A$ 

**Cold Crank**
 $V_{IN} = 24V$  to  $6V$  to  $10V$ ,  $I_{OUT} = 2.5A$ 

 **$V_{IN}$  Ramps Down and Up**
 $V_{IN} = 18V$  to  $4.5V$  to  $0V$  to  $4.5V$  to  $18V$ ,  
 $I_{OUT} = 0A$ 

 **$V_{IN}$  Ramps Down and Up**
 $V_{IN} = 18V$  to  $4.5V$  to  $0V$  to  $4.5V$  to  $18V$ ,  
 $I_{OUT} = 2.5A$ 

**Load Dump**
 $V_{IN} = 24V$  to  $58V$  to  $24V$ ,  $I_{OUT} = 2.5A$ 


**FUNCTIONAL BLOCK DIAGRAM**

**Figure 1: Functional Block Diagram**

## OPERATION

The MP4573 is a fully integrated, synchronous, rectified, non-isolated, switch-mode step-down converter. It can achieve up to 2.5A of continuous output current ( $I_{OUT}$ ) across a wide 4.5V to 60V input supply range, with excellent load and line regulation across an ambient temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Pulse-Width Modulation (PWM) Control

The MPQ4573 operates in fixed-frequency, peak current control mode to regulate the output voltage ( $V_{OUT}$ ) at moderate to high output currents.

An internal clock initiates the pulse-width modulation (PWM) cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on and the inductor current ( $I_L$ ) rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the value set by the COMP voltage ( $V_{COMP}$ ), which is the output of the internal error amplifier (EA).  $V_{COMP}$  is based on the difference between the output feedback voltage ( $V_{FB}$ ) and internal high-precision reference.  $V_{COMP}$  determines the amount of energy that should be transferred to the load. The higher the load current, the higher  $V_{COMP}$  will be. Once the HS-FET turns on, it remains on for a minimum of 90ns.

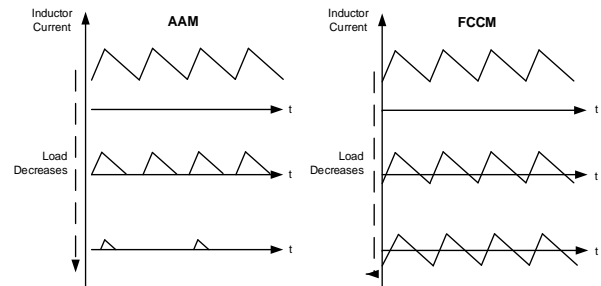
If the HS-FET is off, the low-side MOSFET (LS-FET) turns on and remains on until the clock initiates the next cycle. During this time,  $I_L$  flows through the LS-FET. Once the LS-FET is on, it remains on for a minimum of 100ns before the next cycle begins. To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from being turned on simultaneously.

If the current in the HS-FET does not reach  $V_{COMP}$  within one PWM cycle, the HS-FET remains on, saving a shutdown cycle.

### Light-Load Operation

The MP4573 features configurable forced continuous conduction mode (FCCM) and asynchronous advanced modulation (AAM) mode. FCCM maintains a constant switching frequency ( $f_{SW}$ ) and smaller output ripple, but has low efficiency under light-load conditions. AAM mode is set by the CCM/SYNCO pin, and

achieves high efficiency under light-load conditions (see Figure 2). To force the device into FCCM, connect the CCM/SYNCO pin to ground using a 10k $\Omega$  to 300k $\Omega$  resistor.



**Figure 2: AAM and FCCM**

In FCCM, the converter operates at a fixed frequency across a no-load to full-load range. Under light-load conditions, float CCM/SYNCO to force the device into AAM mode. The device cannot change modes once it is turned on; the desired mode must be selected before start-up.

In AAM mode,  $f_{SW}$  scales down according to  $V_{COMP}$ . The MP4573 enters AAM mode as  $I_L$  reaches 0A. If the load decreases further or there is no load,  $V_{COMP}$  drops below the internally set AAM voltage ( $V_{AAM}$ ). At this point, the MP4573 enters sleep mode and consumes a low quiescent current ( $I_Q$ ) to improve light-load efficiency.

In sleep mode, the internal clock is blocked, causing the MP4573 to skip pulses.  $V_{FB}$  drops below  $V_{REF}$ , and  $V_{COMP}$  ramps up until it exceeds  $V_{AAM}$ . Then the internal clock resets and the crossover time is used as a benchmark for the next clock cycle. This control scheme improves efficiency by scaling down the frequency to reduce switching and gate driver losses.

As  $I_{OUT}$  increases from light load, both  $V_{COMP}$  and  $f_{SW}$  rise. If  $I_{OUT}$  exceeds  $V_{COMP}$ 's set critical level, the MP4573 enters discontinuous conduction mode (DCM) or continuous conduction mode (CCM). CCM has a constant  $f_{SW}$ .

### Enable (EN) Control

The MP4573 can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with a positive logic, which is compatible with popular logic devices.

Positive logic indicates whether the input voltage ( $V_{IN}$ ) has exceeded the under-voltage lockout (UVLO) threshold (about 4V). Pull the EN pin above 1.45V to enable the converter; pull EN below 1.12V to disable the converter. To shut down the converter, float EN via an internal resistor from EN to GND ( $R_{EN}$ ). If enable (EN) control is on, then  $R_{EN} = 2.8M\Omega$ . If EN control is off, then  $R_{EN} = 1.8M\Omega$ .

### Synchronous Output (SYNCO)

The MP4573 has a SYNCO pin for synchronous output. During start-up, SYNCO remains low and outputs a 180° phase-shifted clock to the internal oscillator once soft start (SS) is ready. SYNCO's falling edge is a 180° phase shift from the rising edge of the internal oscillator. This synchronous output function allows two devices to operate at the same frequency, but 180° out of phase. This reduces the total input current ripple and allows for the use of a smaller input bypass capacitor.

### Internal Regulator

A 4.9V internal regulator powers most of the MP4573's internal circuitries. This regulator takes  $V_{IN}$  and operates across the full  $V_{IN}$  range. If  $V_{IN}$  exceeds 4.9V, the regulator's output is in full regulation. A lower  $V_{IN}$  results in a lower  $V_{OUT}$ . If  $V_{IN}$  exceeds its UVLO threshold and EN is high, the regulator turns on. During an EN shutdown, the internal VCC regulator turns off to reduce power dissipation.

### Configurable and Foldback Frequency

The MP4573's switching frequency ( $f_{SW}$ ) can be configured via an external frequency resistor ( $R_{FREQ}$ ).  $R_{FREQ}$  should be placed between the FREQ and GND pins, as close to the IC as possible. Choose an appropriate  $R_{FREQ}$  value, which can be calculated with Equation (1):

$$R_{FREQ} (M\Omega) = \frac{30}{f_{SW} (kHz)} \quad (1)$$

A bench test may be required to fine-tune the calculated resistance. Due to the HS-FET's limited minimum on time, it is not possible to use a high  $f_{SW}$  with a high  $V_{IN}$ . The MP4573's control loop sets the maximum  $f_{SW}$  automatically to match the set frequency. This reduces excessive power loss in the IC.  $V_{OUT}$  is regulated by varying the HS-FET off time. Varying the duration of the off time automatically reduces  $f_{SW}$ .

Compliance with the minimum HS-FET on time is guaranteed. This allows the device to operate at the desired  $f_{SW}$  for as long as possible. A correction is only made if  $V_{IN}$  is high. For more details, see the Switching Frequency vs. Input Voltage curve on page 14, where  $R_{FREQ} = 12.1kHz$ .

Table 1 shows the relationship between  $f_{SW}$  and  $R_{FREQ}$ .

**Table 1:  $f_{SW}$  vs.  $R_{FREQ}$**

$R_{FREQ} (k\Omega)$	$f_{SW} (kHz)$	$R_{FREQ} (k\Omega)$	$f_{SW} (kHz)$
100	300	24.3	1150
91.9	330	22	1250
82.5	360	20	1350
76.8	400	18.2	1500
68.1	430	16.2	1650
61.9	475	15	1750
56	520	14	1900
47	600	13	2050
39	700	12.1	2200
34.8	800	11.5	2250
30	940	11	2350
28	1000	10	2500

### Internal Soft Start (SS)

To avoid overshoot during start-up, the MP4573 has built-in soft start (SS). During SS,  $V_{OUT}$  ramps up at a controlled slew rate once EN goes high. If the soft-start voltage ( $V_{SS}$ ) drops below the internal reference voltage ( $V_{REF}$ ),  $V_{SS}$  overrides  $V_{REF}$  as the EA reference. If  $V_{SS}$  exceeds  $V_{REF}$ ,  $V_{REF}$  acts as the reference. Once SS is complete, the MP4573 enters steady state operation.

The soft-start time ( $t_{SS}$ ) is set internally to 0.45ms. If  $V_{OUT}$  shorts to GND,  $V_{FB}$  is pulled low and  $V_{SS}$  discharges. Once the short is removed and the MPQ4573 returns to a normal state, the device initiates another SS.

### Pre-Biased Start-Up

If  $V_{FB}$  exceeds  $V_{SS}$  during start-up, the output has a pre-biased voltage and neither the HS-FET or LS-FET turns on until  $V_{SS}$  exceeds  $V_{FB}$ . This capability is only available when the device is in AAM mode.

### Power Good (PG) Indicator

The MP4573 has power good (PG) indication. The PG pin is the open drain of a MOSFET. A resistor (e.g. 100k $\Omega$ ) is required to connect PG to a voltage source. In the presence of  $V_{IN}$ , this



MOSFET turns on and PG is pulled down to GND before SS is ready. If  $V_{OUT}$  is between 90% and 108% of the nominal voltage after a 70 $\mu$ s delay, PG goes high. If  $V_{OUT}$  is above 116% or below 84% of the nominal voltage after a 25 $\mu$ s delay, PG goes low.

### Under-Voltage Lockout (UVLO) Protection

The MP4573 includes  $V_{IN}$  under-voltage lockout protection (UVLO) to ensure reliable output power. If EN control is on, the MP4573 starts up once  $V_{IN}$  exceeds the UVLO rising threshold. If  $V_{IN}$  drops below the UVLO falling threshold, the device shuts down. This prevents the device from operating at an insufficient supply voltage.  $V_{IN}$  UVLO is a non-latch protection.

### Over-Current Protection (OCP)

The MP4573 has a 3.9A peak current limit. If  $I_L$  exceeds the current limit, the HS-FET turns off and the LS-FET turns on to discharge the energy, reducing  $I_L$ . The HS-FET does not turn on again until  $I_L$  drops below the valley current limit threshold. Over-current protection (OCP) prevents  $I_L$  runaway that can damage the components.

### Short-Circuit Protection (SCP)

If a short-circuit condition occurs, the MP4573 reaches its peak current limit and  $V_{OUT}$  drops until  $V_{FB}$  is below 50% of  $V_{REF}$ . The device recognizes this as an output dead short, and triggers hiccup short-circuit protection (SCP) with hiccup mode to periodically restart the part.

In hiccup mode, the MP4573 disables the output power stage and slowly discharges the soft-start capacitor ( $C_{SS}$ ), then initiates another SS. If the short-circuit condition remains after SS finishes, the device repeats this operation until the short circuit disappears and  $V_{OUT}$  returns to its regulation level. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator.

### Negative Current Protection

The MP4573 has a -1.3A negative current limit. If  $I_L$  drops below the negative current limit, the LS-FET turns off and the HS-FET turns on. This prevents the negative current from dropping too low and potentially damaging the components.

### Thermal Shutdown

To improve thermal protection, the MP4573 monitors the IC temperature internally. This prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the thermal shutdown threshold (about 170°C), the device shuts down. Thermal shutdown is a non-latch protection, and has a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device initiates SS and resumes normal operation.

### Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor powers the floating HS-FET driver. There are two methods to charge the BST capacitor ( $C_{BST}$ ).

The first method is to use a diode from  $V_{CC}$  as the main charging circuit to charge the capacitor. If the HS-FET is on, the SW voltage ( $V_{SW}$ ) should be about equal to  $V_{IN}$ , but exceed  $V_{CC}$ . In this scenario,  $C_{BST}$  is not charged. The ideal charging period occurs when the LS-FET is on, and ( $V_{CC} - V_{SW}$ ) is at its maximum. When there is no  $I_L$  present,  $V_{SW}$  equals  $V_{OUT}$ , and  $V_{CC}$  can only charge  $C_{BST}$  when  $V_{OUT}$  is very small.

The second method is to charge the capacitor via the auxiliary charging circuit from  $V_{IN}$ . If the difference between the BST voltage ( $V_{BST}$ ) and  $V_{SW}$  drops below the internal 5V BST regulator voltage, a P-channel MOSFET pass transistor (M1) turns on to charge  $C_{BST}$ . This charging current is much smaller than the charging current from  $V_{CC}$ , but as long as  $V_{IN}$  exceeds  $V_{SW}$ ,  $C_{BST}$  can be charged from  $V_{IN}$ . This charging method is useful in sleep mode, where on/off switching does not always occur. Figure 3 shows the internal BST charging circuit.

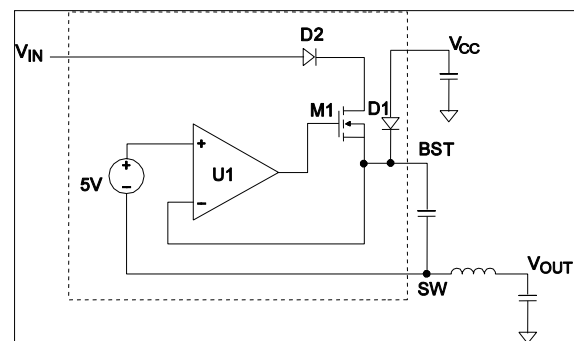


Figure 3: Internal BST Charging Circuit

**Low-Dropout (LDO) Mode (BST Refresh)**

To improve dropout, the MP4573 is designed to operate at close to 100% duty cycle, so long as the voltage between BST and SW exceeds 1.4V. If this voltage drops below 1.34V, the HS-FET turns off via a UVLO circuit. This allows the LS-FET to conduct and refresh the charge on  $C_{BST}$ . If  $V_{IN}$  drops, the HS-FET continues to operate at as close to 100% duty as possible to maintain output regulation, unless the voltage between BST and SW falls below 1.34V.

Since the supply current sourced from  $C_{BST}$  is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. This means the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is primarily influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

**Start-Up and Shutdown**

If both  $V_{IN}$  and the EN voltage ( $V_{EN}$ ) exceed their respective thresholds, the device starts up. First, the reference block turns on and generates a stable current and  $V_{REF}$ . Then the internal regulator turns on. The regulator provides a stable supply for the remaining circuitry.

While the internal supply rail is up, an internal timer keeps the power MOSFET off for about 50 $\mu$ s to blank any start-up glitches. When the soft-start block turns on, it keeps  $V_{SS}$  low to ensure all circuitries are ready. Then  $V_{SS}$  slowly ramps up.

Three events can shut down the chip: EN going low,  $V_{IN}$  UVLO, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any accidental fault triggering, then  $V_{COMP}$  and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

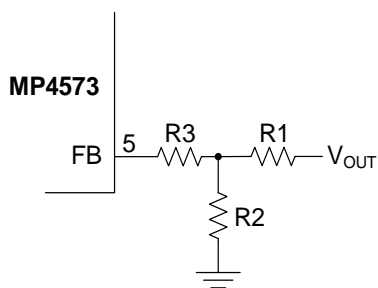
## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider connected to the FB pin sets  $V_{OUT}$  (see the Typical Application Circuits section on page 31). The feedback resistor (R1) must account for both stability and dynamic response, and therefore must not be too large or too small. Choose an R1 value of about 40k $\Omega$ . Then R2 can be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8} - 1} \quad (2)$$

Figure 4 shows the recommended T-type feedback network.



**Figure 4: Feedback Network**

$R3 + R1$  sets the loop bandwidth. A higher  $R3 + R1$  indicates a lower bandwidth. To ensure loop stability, it is recommended to limit the bandwidth below 10% of  $f_{SW}$ , and no higher than 100kHz.

The calculated resistance may require fine-tuning via bench testing. Table 2 lists the recommended feedback divider resistor values for common output voltages. Use check loop analysis before using the device in an application, and change the resistance of R3 for loop stability if necessary.

**Table 2: Recommended Resistor Values for Common  $V_{OUT}$**

$V_{OUT}$ (V)	R1 (k $\Omega$ )	R2 (k $\Omega$ )	R3 (k $\Omega$ )
3.3	41.2	13	20
5.0	41.2	7.68	20
8	41.2	4.53	20
12	41.2	2.98	20

### Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching  $V_{IN}$ . For the highest efficiency, choose an

inductor with a low DC resistance. A larger-value inductor offers less ripple current and lower output ripple voltage; however, it also results in a physically larger inductor, higher series resistance, and lower saturation current.

To determine the ideal inductance, it is recommended to allow the inductor ripple current to be approximately 30% of the maximum load current. Ensure that the peak inductor current ( $I_{LP}$ ) is below the device's peak current limit. The inductance (L) can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak inductor current.  $I_{LP}$  can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

### Selecting the Input Capacitor ( $C_{IN}$ )

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC to the converter while maintaining the DC  $V_{IN}$ . For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. Other capacitors, such as Y5V and Z5U, should not be used since they lose too much capacitance with frequency, temperature, and bias voltage.

Place the input capacitor ( $C_{IN}$ ) as close to the  $V_{IN}$  pin as possible. For most applications, a 22 $\mu$ F capacitor is sufficient. For higher  $V_{OUT}$ , use a 47 $\mu$ F capacitor to improve system stability. To maintain a small solution size, choose a properly sized capacitor that has a voltage rating compliant with the input specifications.

Since  $C_{IN}$  absorbs the input switching current, it requires an adequate ripple current rating. The ripple current rating should not exceed the converter's maximum input ripple current. The

input ripple current ( $I_{CIN}$ ) can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose a  $C_{IN}$  with an RMS current rating greater than half of the maximum load current.

$C_{IN}$  can be electrolytic, tantalum, or ceramic. If using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (0.1 $\mu$ F) as close to the IC as possible. The input capacitance determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose a  $C_{IN}$  that meets the relevant specifications.

The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

### Selecting the Output Capacitor ( $C_{OUT}$ )

The output capacitor ( $C_{OUT}$ ) maintains the DC  $V_{OUT}$ . Ceramic capacitors with low ESR are recommended for their small size and low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}\right) \quad (9)$$

Where  $R_{ESR}$  is the equivalent series resistance of  $C_{OUT}$ .

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

Another consideration for output capacitance is the allowable  $V_{OUT}$  overshoot if the load is suddenly removed. In this case, energy stored in the inductor is transferred to  $C_{OUT}$ , causing its voltage to rise. To achieve a desired overshoot relative to the regulated voltage,  $C_{OUT}$  can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times \left(\left(\frac{V_{OUTMAX}}{V_{OUT}}\right)^2 - 1\right)} \quad (12)$$

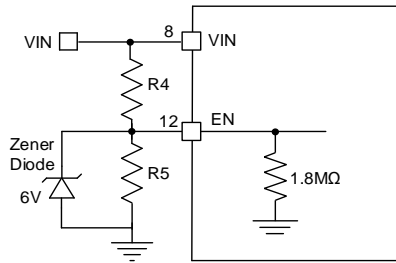
Where  $V_{OUTMAX} / V_{OUT}$  is the allowable maximum overshoot.

After calculating the capacitance required for both ripple and overshoot needs, choose the larger value.

The characteristics of  $C_{OUT}$  also affect the stability of the regulation system. The MP4573 can be optimized for a wide range of capacitance and ESR values.

### Setting $V_{IN}$ Under-Voltage Lockout (UVLO)

The MP4573 has an internal, fixed UVLO threshold. The rising threshold is 4V, and the falling threshold is about 3.5V. For applications that require a higher UVLO point, place an external resistor divider between EN and  $V_{IN}$  to obtain a higher equivalent UVLO threshold (see Figure 5 and Figure 6 on page 29). If the EN pin is connected to  $V_{IN}$  through a resistor, add a 6V Zener diode between EN and GND.

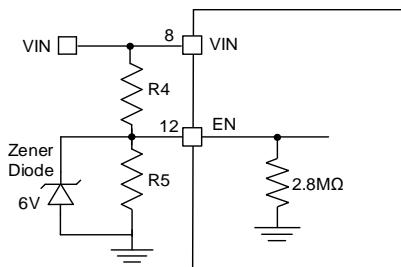


**Figure 5: Adjustable UVLO via the EN Divider if  $V_{EN}$  Rises**

When  $V_{EN}$  is rising, the UVLO threshold can be calculated with Equation (13):

$$V_{IN\_UV\_RISING} = \left(1 + \frac{R4}{1.8M\Omega // R5}\right) \times V_{EN\_RISING} \quad (13)$$

Where  $V_{EN\_RISING} = 1.45V$ .



**Figure 6: Adjustable UVLO via the EN Divider if  $V_{EN}$  Falls**

When  $V_{EN}$  is falling, the UVLO threshold can be calculated with Equation (14):

$$V_{IN\_UV\_FALLING} = \left(1 + \frac{R4}{2.8M\Omega // R5}\right) \times V_{EN\_FALLING} \quad (14)$$

Where  $V_{EN\_FALLING} = 1.12V$ .

Choose an  $R4$  that is big enough to limit the current flowing into EN to below  $100\mu A$ .

### Bootstrap (BST) Resistor and Capacitor

A resistor ( $R_{BST}$ ) in series with  $C_{BST}$  can reduce SW's rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at high input voltages. A higher resistance is better for SW spike reduction, but can compromise efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep  $R_{BST}$  below  $20\Omega$ . The recommended  $C_{BST}$  value is between  $0.1\mu F$  and  $1\mu F$ .

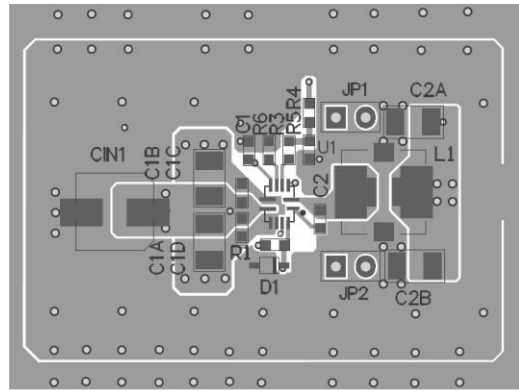
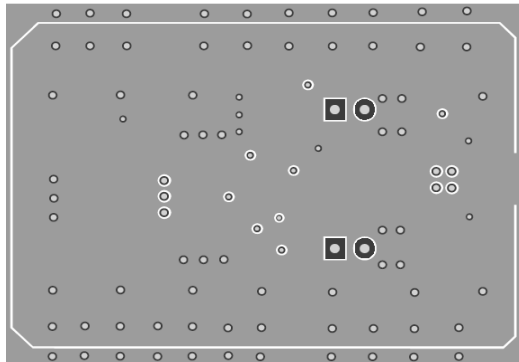
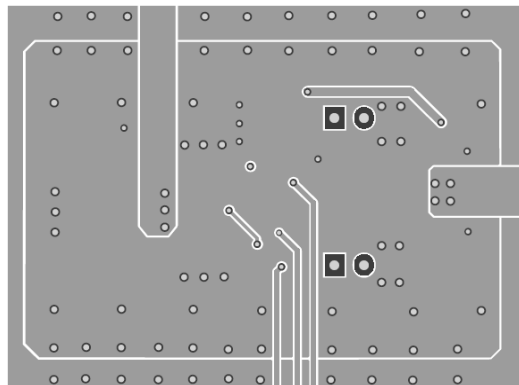
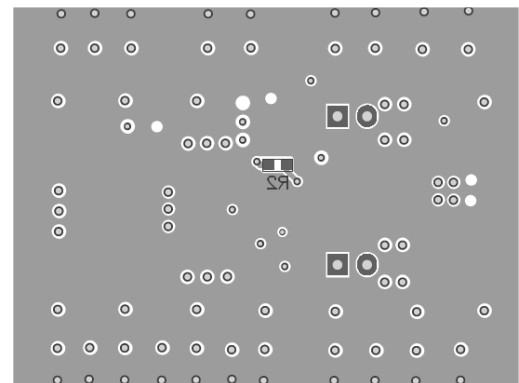
**PCB Layout Guidelines <sup>(11)</sup>**

Efficient PCB layout is critical for stable operation. It is strongly recommended to use a 4-layer PCB layout to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. To minimize high-frequency noise, place the ceramic input capacitors as close to VIN and GND as possible.
4. To ensure that the FB trace is as short as possible, place the T-type FB resistors as close to the FB pin as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Use multiple vias to connect the power planes to internal layer.

**Note:**

11) The recommended PCB layout is based on Figure 8 (see the Typical Application Circuits section on page 31).


**Top Silk and Top Layer**

**Mid-Layer 1**

**Mid-Layer 2**

**Bottom Layer and Bottom Silk**
**Figure 7: Recommended PCB Layout**

### TYPICAL APPLICATION CIRCUITS

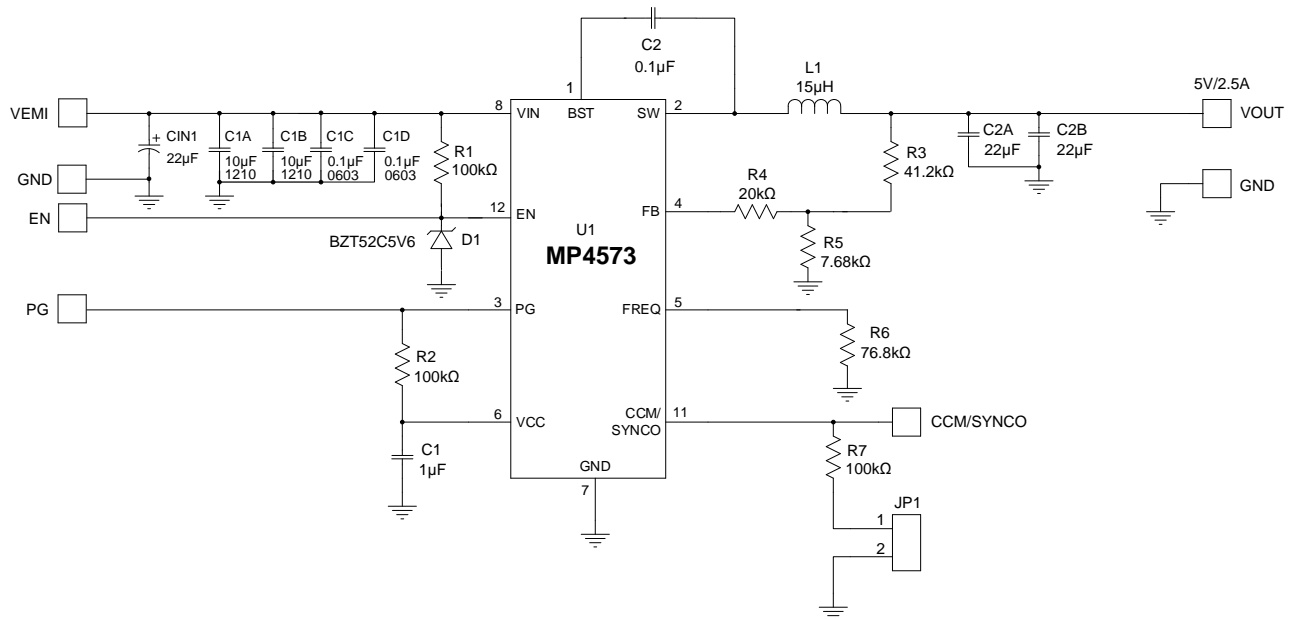


Figure 8: Typical Application Circuit

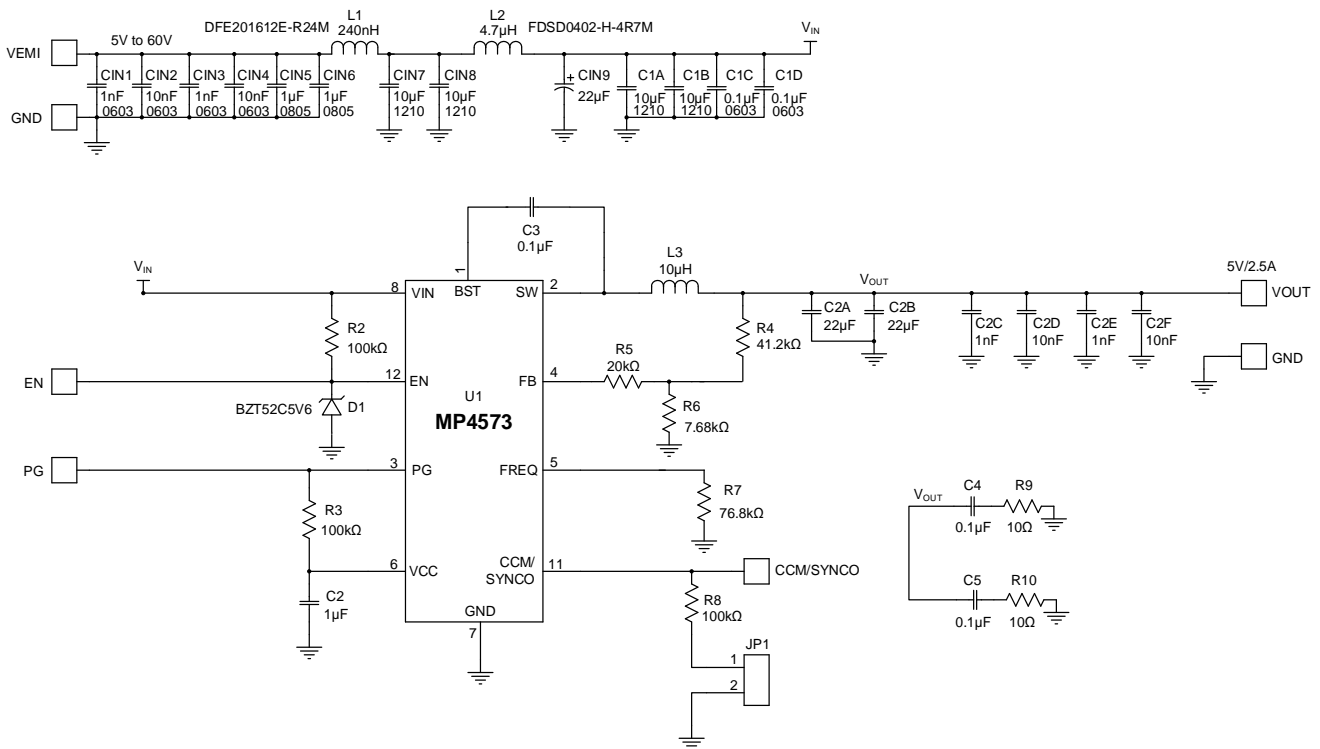
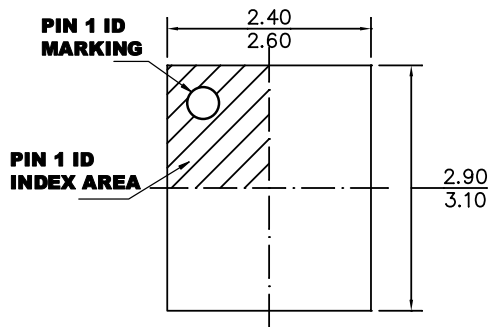


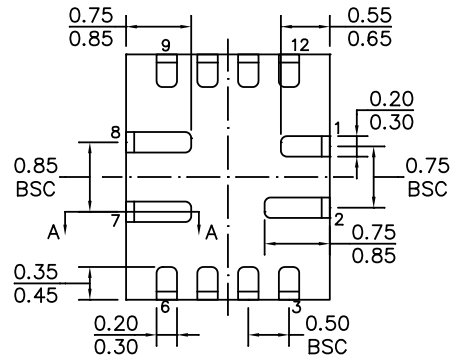
Figure 9: Typical Application Circuit with EMI Filters

## PACKAGE INFORMATION

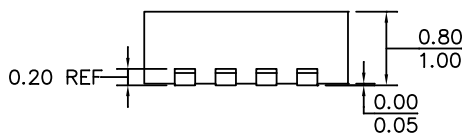
### QFN-12 (2.5mmx3mm) Wettable Flank



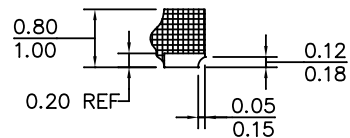
**TOP VIEW**



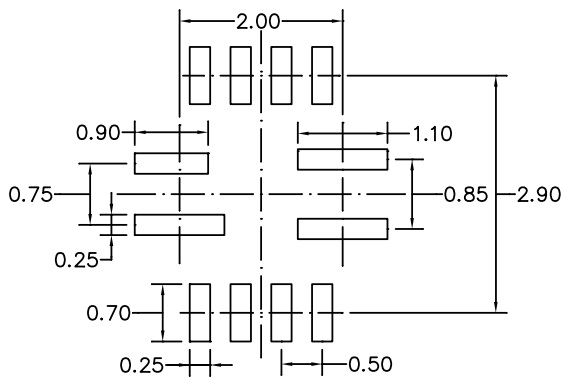
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**

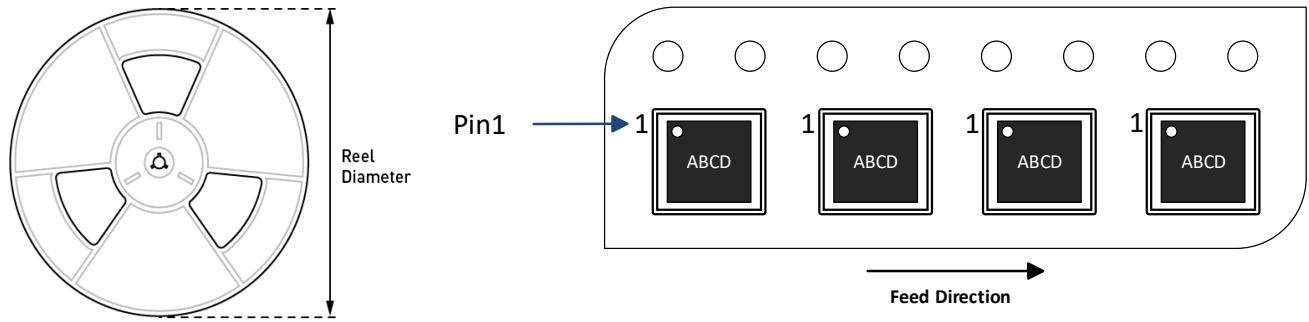


**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) THE LAND PATTERNS OF PINS 2, 7, AND 8 HAVE THE SAME LENGTH AND WIDTH.
- 3) ALL DIMENSIONS ARE IN MILLIMETERS.
- 4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-220.
- 6) DRAWING IS NOT TO SCALE.



**CARRIER INFORMATION**


Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4573GQBE-Z	QFN-12 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm



## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/29/2021	Initial Release	-

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