MPQ2123

6V, 2A, Configurable Frequency, Synchronous Buck Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2123 is a configurable frequency (300kHz to 2.2MHz), synchronous step-down converter. It can achieve up to 2A of continuous output current with peak current control for excellent transient response and efficiency. It operates from a 2.7V to 6V input voltage range, and can generate an output voltage as low as 0.606V. The MPQ2123 is ideal for a wide range of applications, including automotive infotainment systems, clusters, telematics, and portable instruments.

The MPQ2123 integrates a 40mΩ high-side MOSFET (HS-FET) and a 30mΩ synchronous rectifier for high efficiency without an external Schottky diode. The MPQ2123 can be configured to operate in advanced asynchronous modulation (AAM) mode or forced continuous conduction mode (FCCM) under light-load conditions. AAM provides high efficiency by reducing switching losses at light load, while FCCM offers controllable frequency and a lower output ripple.

The MPQ2123 features soft start (SS), an external sync clock, enable (EN) control, and a power good (PG) indicator.

Full protection features include over-current protection (OCP) with valley current detection to avoid current runaway, short-circuit protection (SCP), input under-voltage lockout (UVLO), output over-voltage protection (OVP), and thermal shutdown.

With internal compensation, the MPQ2123 requires a minimal number of readily available, standard external components. It is available in a QFN-11 (2mmx3mm) package.

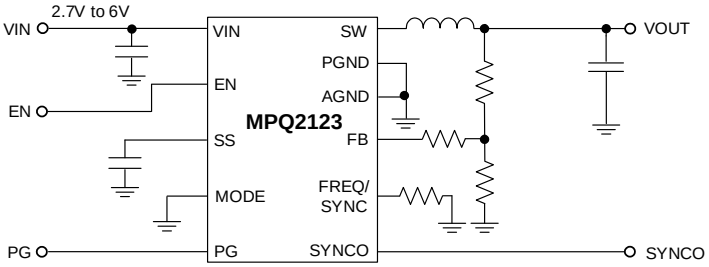
FEATURES

- 2.7V to 6V Operating Input Range
- Adjustable Output from 0.606V
- Up to 2A Continuous Output Current
- High-Efficiency Synchronous Mode Control
- 40mΩ and 30mΩ Internal Power MOSFETs
- Up to 2.2MHz Configurable Frequency
- Up to 2.2MHz External Sync Clock
- 45μA Quiescent Current (I_Q)
- Low Shutdown Current (I_{SD})
- 100% Duty Cycle Operation
- Internal Compensation Mode
- Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM)
- External Soft Start (SS)
- Remote Enable (EN) Control
- Power Good (PG) Indicator
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- V_{IN} Under-Voltage Lockout (UVLO)
- V_{OUT} Over-Voltage Protection (OVP)
- Thermal Shutdown
- Available in a QFN-11 (2mmx3mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

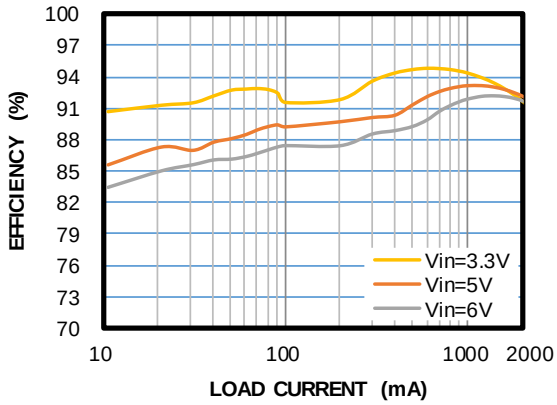
- Automotive Infotainment Systems
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 1µH, f_{SW} = 2.1MHz, AAM mode



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2123GD-AEC1	QFN-11 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ2123GD-AEC1–Z).

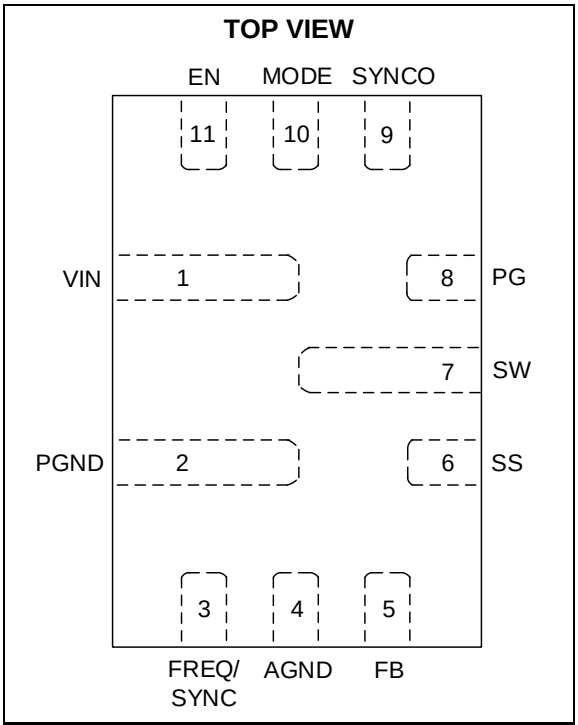
** Moisture Sensitivity Level Rating

TOP MARKING

BVF
YWW
LLLL

BVF: Product code of MPQ2123GD-AEC1
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input supply.** The VIN pin supplies power to the converter. To reduce switching spikes at the input, place a decoupling capacitor from VIN to ground, as close to the IC as possible.
2	PGND	**Power ground.** Connect the large copper areas of PGND to the negative terminals of the input and output capacitors.
3	FREQ/ SYNC	**Configurable switching frequency (f_{SW}) and synchronization input.** To set f_{SW}, connect a resistor to ground. The FREQ/SYNC pin can synchronize f_{SW} via an external clock.
4	AGND	**Analog ground.** Ground for the internal logic and signal circuit.
5	FB	**Feedback point.** The FB pin is the negative input of the error amplifier (EA). To set the regulation voltage, connect FB to the tap of an external resistor divider between the output and GND. In addition, the power good (PG) and under-voltage lockout (UVLO) circuits use FB to monitor the output voltage (V_{OUT}).
6	SS	**Soft start.** To set the soft-start time externally, place a capacitor from the SS pin to ground. Float this pin to activate the internal, default 1ms soft-start setting.
7	SW	**Switch output.** Connect the SW pin internally to the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). Connect SW externally to the output inductor.
8	PG	**Power good indicator.** The PG pin is an open-drain output that connects to VIN via an internal pull-up resistor. If the FB voltage (V_{FB}) is within 15% of the regulation voltage, PG is pulled up to VIN. If V_{FB} is outside of the regulation voltage range, PG is pulled low.
9	SYNCO	**Synchronization output.** The SYNCO pin outputs a 180° out-of-phase clock to the other devices that require a synchronized signal.
10	MODE	**Mode selection.** For forced continuous conduction mode (FCCM), connect the MODE pin to logic high or the input voltage (V_{IN}). For advanced asynchronous modulation (AAM) mode, connect MODE to logic low or ground. Do not float MODE.
11	EN	**Enable input.** Pull the EN pin high to turn the converter on; pull EN to ground or float EN to turn the converter off.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 6.5V
V_{SW} ..... -0.3V (-3V for <10ns) to +6.5V (7V for <10ns)
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-11 (2mmx3mm) 1.78W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}) ..... 2.7V to 6.0V
Output voltage (V_{OUT}) ..... 0.606V to V_{IN}
Load current range ..... 0A to 2A
Operating junction temp (T_J) -40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-11 (2mmx3mm)		
JESD51-7 (4)	70	15 °C/W
EV2123-D-00A (5)	42	13.5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device may be able to support an operating junction temperature above 125°C. Contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on standard EVB (6.35cmx6.35cm), thick 2oz copper, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and Under-Voltage Lockout (UVLO)						
Quiescent current	I_Q	AAM mode, V_{EN} = 2V, no load, R_{FREQ} = 1MΩ, T_J = 25°C		45	50	μA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	AAM mode, V_{EN} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			20	
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$		2.3	2.5	2.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2	2.15	2.3	V
V_{IN} UVLO hysteresis threshold	$V_{IN\_UVLO\_HYS}$			350		mV
Output and Regulation						
Regulated feedback (FB) voltage	V_{FB}	T_J = 25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.591		0.621	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Power MOSFETs and Frequency						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{IN} = 5V, I_{OUT} = 200mA		40	70	mΩ
Low-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{IN} = 5V, I_{OUT} = 200mA		30	70	mΩ
HS-FET SW leakage current	$I_{SW\_LKG\_HS}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 6V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			30	
LS-FET SW leakage current	$I_{SW\_LKG\_LS}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			10	
Switching frequency	f_{SW}	R_{FREQ} = 499kΩ	380	450	520	kHz
		R_{FREQ} = 75kΩ	1800	2100	2400	
SYNC frequency range	f_{SYNC}		0.3		2.2	MHz
SYNC high-voltage threshold	V_{SYNC_HIGH}	V_{IN} = 2.7V (6)	1.5			V
		V_{IN} = 3.6V	1.8			
		V_{IN} = 6V (6)	3.2			
SYNC low-voltage threshold	V_{SYNC_LOW}	V_{IN} = 2.7V (6)			0.8	V
		V_{IN} = 3.6V			1.1	
		V_{IN} = 6V (6)			1.6	
Maximum duty cycle	D_{MAX}			100		%
Minimum on time (6)	t_{ON_MIN}			50		ns
Minimum off time (6)	t_{OFF_MIN}			95		ns
Power Good (PG)						
PG current sink	V_{PG_SINK}	1mA sink			300	mV
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V	4.5			V
PG delay time	t_{PG_DELAY}	V_{OUT} rising edge	40	100	180	μs
		V_{OUT} falling edge	5	20	30	μs
PG upper rising threshold	$V_{PG\_UP\_RISING}$	As a percentage of V_{FB}	108	115	122	%
PG upper hysteresis	$V_{PG\_UP\_HYS}$	As a percentage of V_{FB}		5		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
PG lower rising threshold	$V_{PG\_LOW\_RISING}$	As a percentage of V_{FB}	80	85	90	%
PG lower hysteresis	$V_{PG\_LOW\_HYS}$	As a percentage of V_{FB}		5		%
Enable (EN)						
EN rising threshold	V_{EN_RISING}		1.2			V
EN falling threshold	$V_{EN\_FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2	5	µA
		V_{EN} = 0V		0	0.5	µA
MODE and Soft Start (SS)						
MODE rising threshold	V_{MODE_FCCM}	FCCM	1.2			V
MODE falling threshold	V_{MODE_AAM}	AAM mode			0.4	V
MODE leakage current	I_{MODE_LKG}	Pulled up to 6V			1	µA
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	4	6	µA
Default soft-start time	$t_{SS\_DEFAULT}$			1		ms
Protections						
Peak current limit	I_{LIMIT_PEAK}	Sourcing, duty cycle = 40%	4	5.5	8.6	A
Valley current limit	I_{LIMIT_VALLEY}			4		A
OCP timer (6)	t_{OCP}			100		µs
Zero-cross threshold	I_{ZCD}			100		mA
Output over-voltage protection (OVP) limit	V_{OVP_LIMIT}	As a percentage of V_{FB}		115		%
Thermal shutdown (6)	T_{SD}	Temperature rising		170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			25		°C

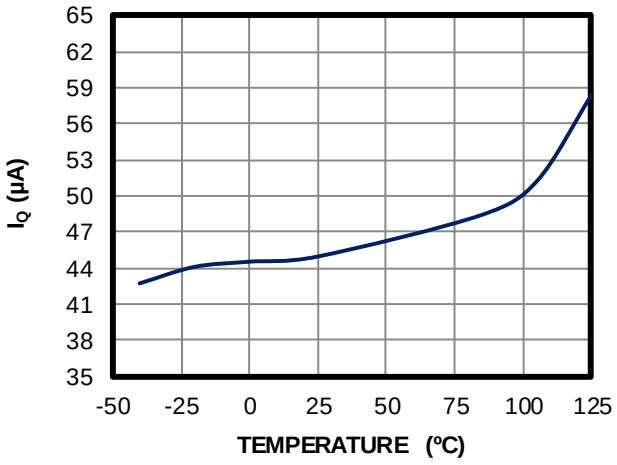
Note:

6) Not tested in production. Guaranteed by design and characterization.

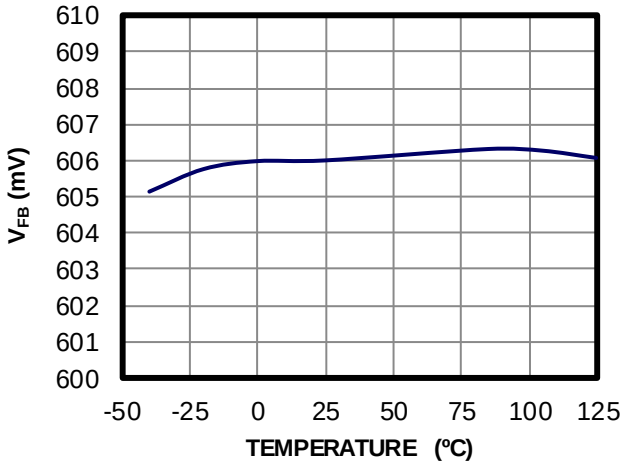
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

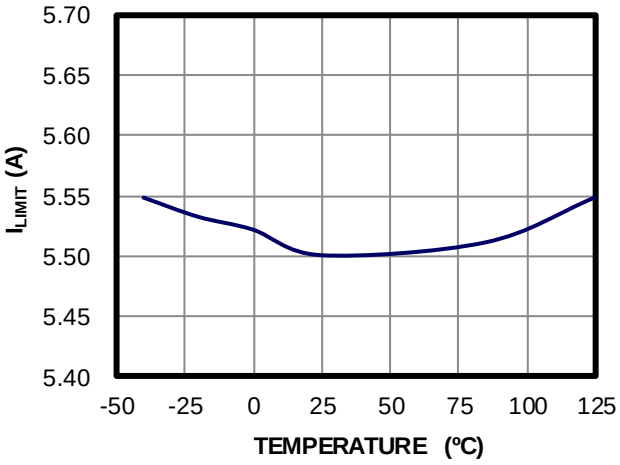
Quiescent Current vs. Temperature



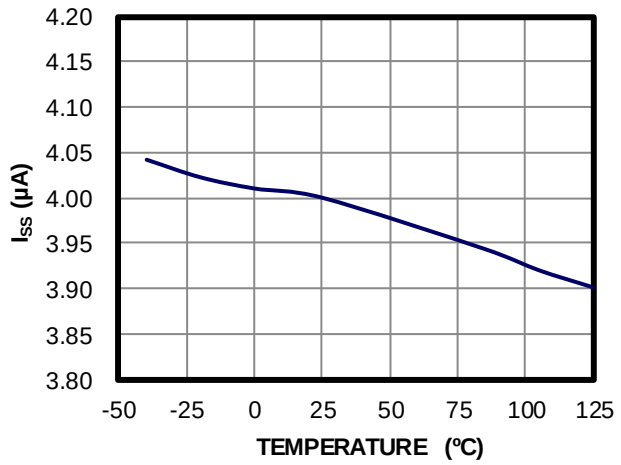
Feedback Voltage vs. Temperature



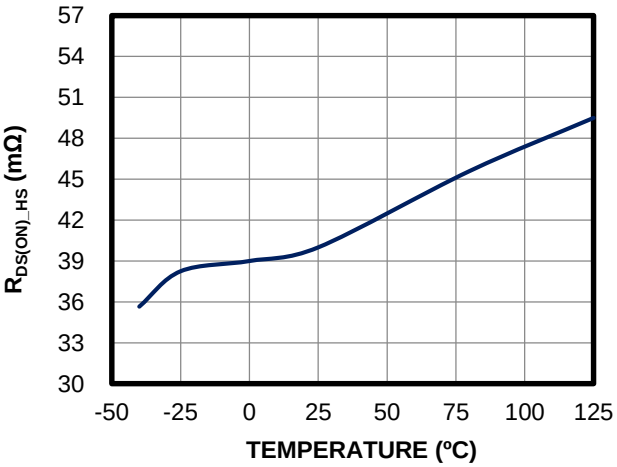
Current Limit vs. Temperature



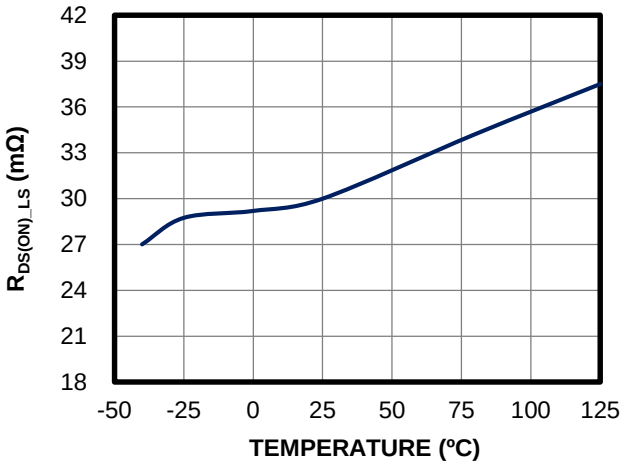
Soft-Start Current vs. Temperature



HS-FET On Resistance vs. Temperature



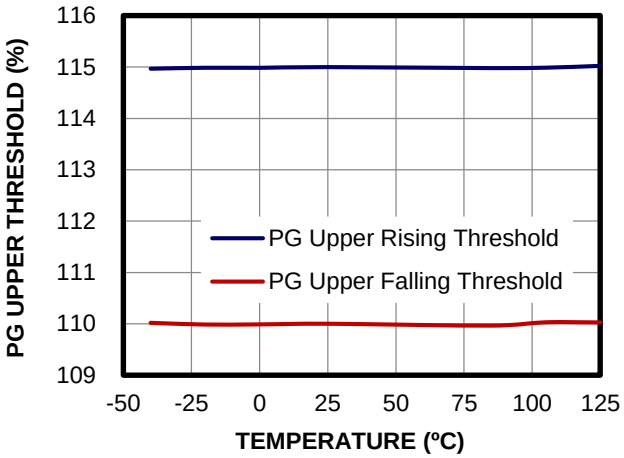
LS-FET On Resistance vs. Temperature



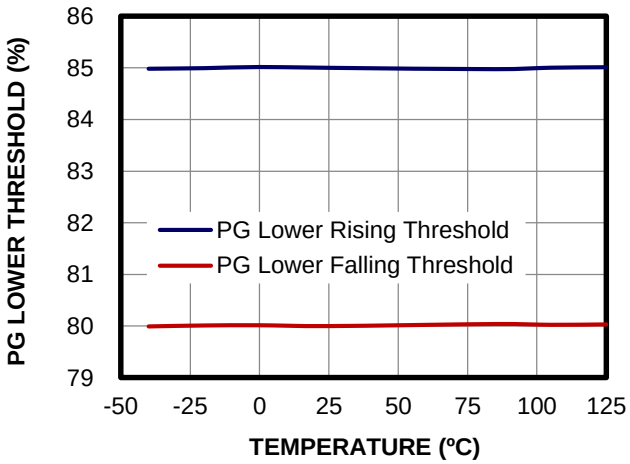
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

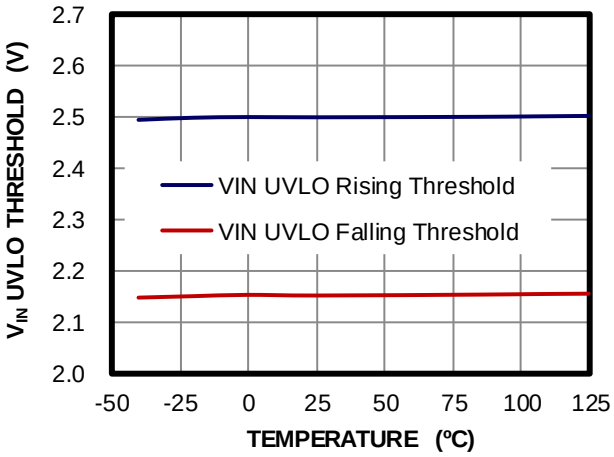
PG Upper Threshold vs. Temperature



PG Lower Threshold vs. Temperature



V_{IN} UVLO Threshold vs. Temperature

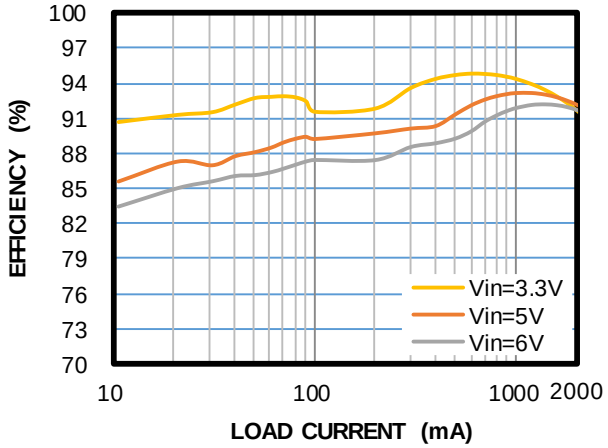


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

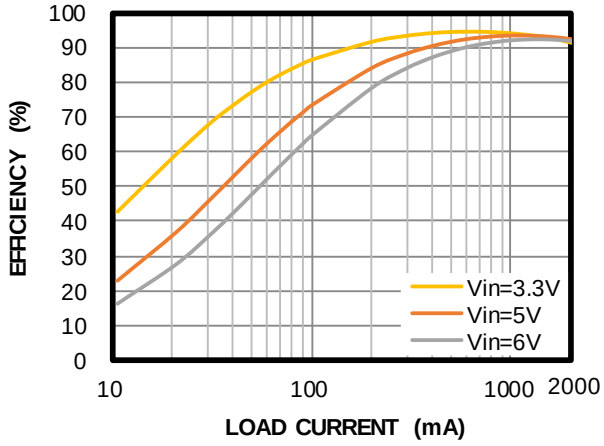
Efficiency vs. Load Current

V_{OUT} = 1.8V, AAM mode



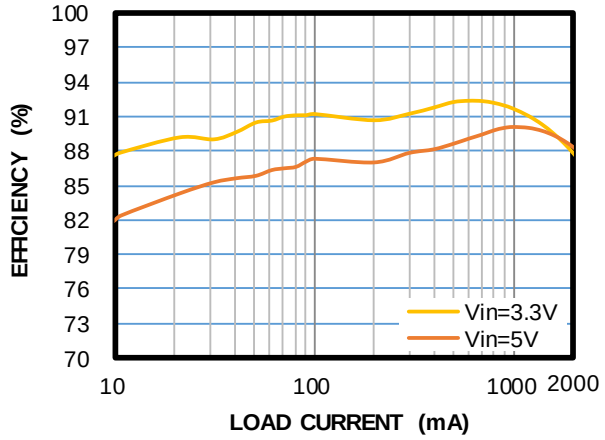
Efficiency vs. Load Current

V_{OUT} = 1.8V, FCCM



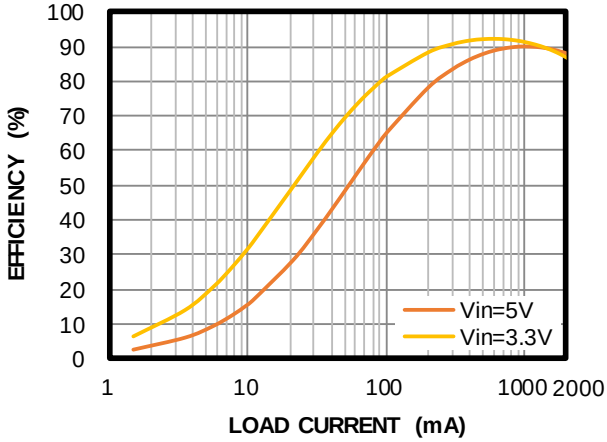
Efficiency vs. Load Current

V_{OUT} = 1.2V, AAM mode



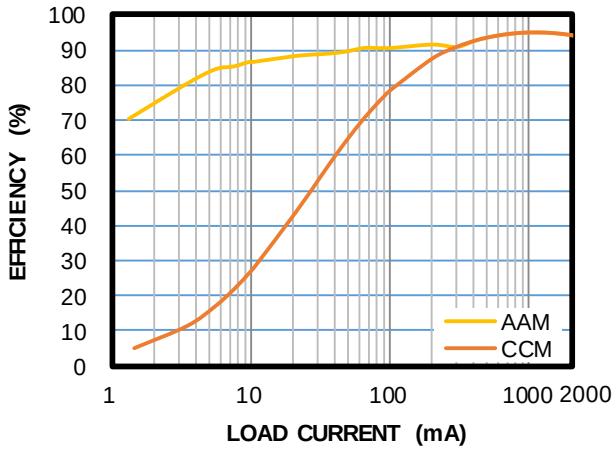
Efficiency vs. Load Current

V_{OUT} = 1.2V, FCCM



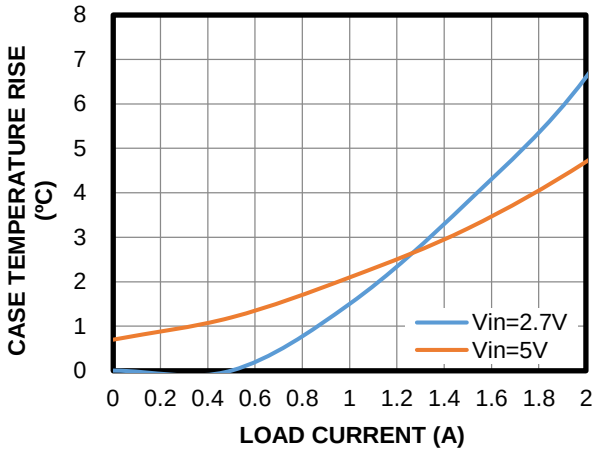
Efficiency vs. Load Current

V_{IN} = 5V, V_{OUT} = 2.5V



Case Temperature Rise vs. Load Current

V_{OUT} = 1.8V, AAM mode

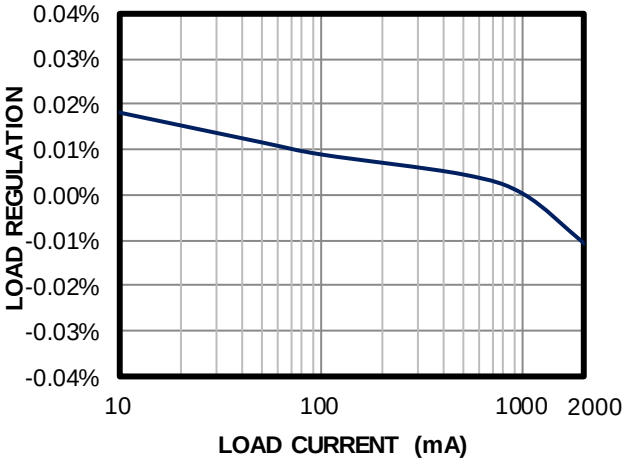


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

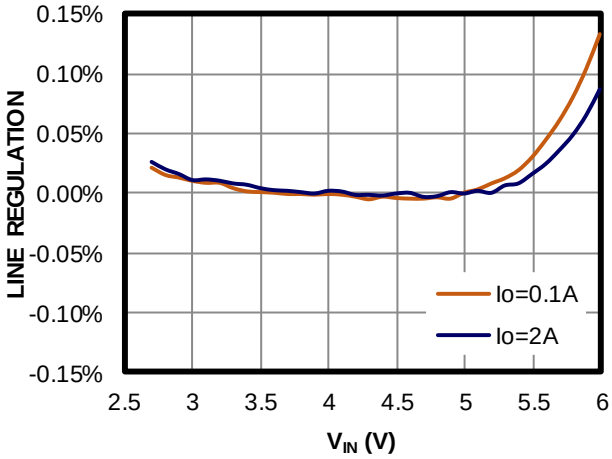
Load Regulation

V_{OUT} = 1.8V

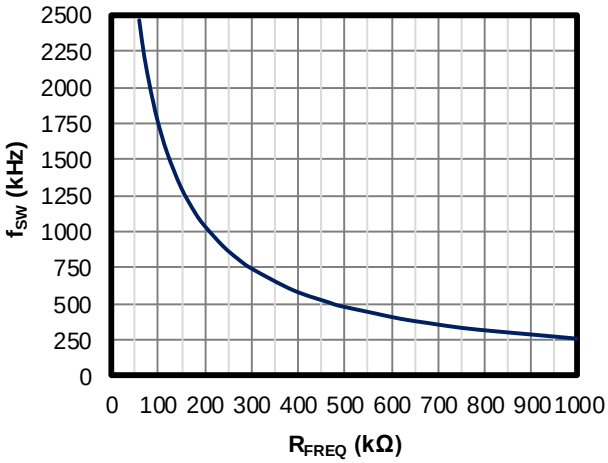


Line Regulation

V_{OUT} = 1.8V, AAM mode



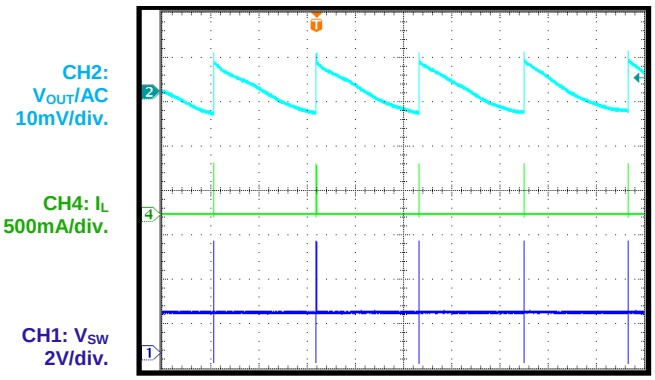
Switching Frequency vs. Frequency Resistance



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

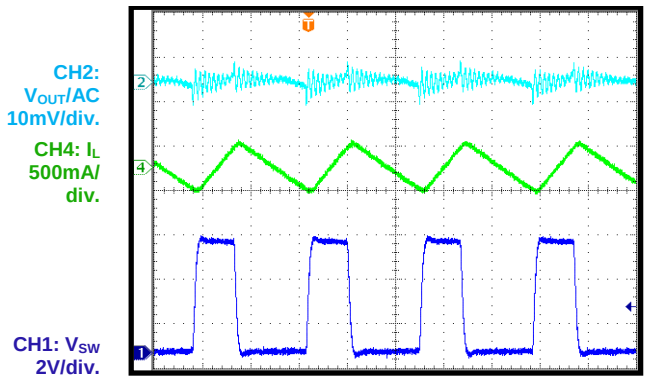
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Steady State
I_{OUT} = 0A, AAM mode



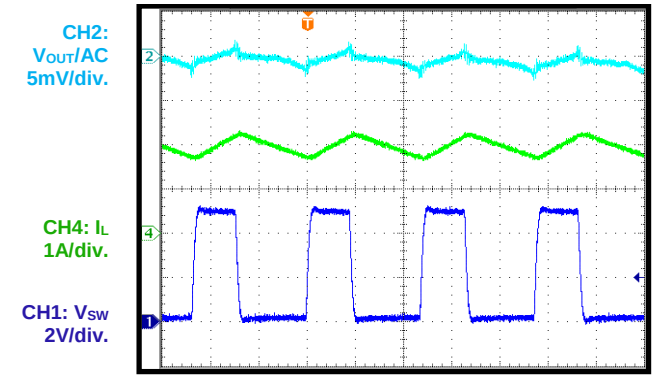
10ms/div.

Steady State
I_{OUT} = 0A, FCCM



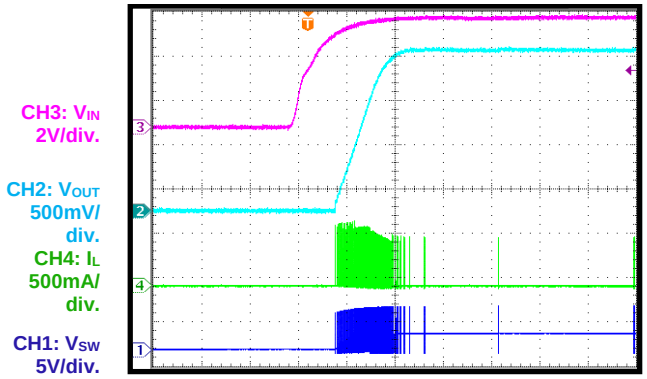
200ns/div.

Steady State
I_{OUT} = 2A



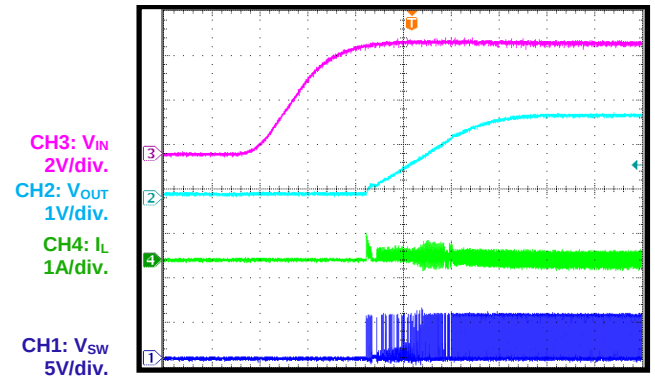
200ns/div.

Start-Up through VIN
I_{OUT} = 0A, AAM mode



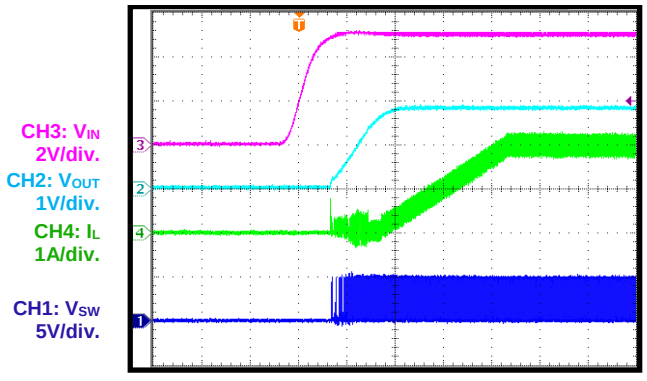
1ms/div.

Start-Up through VIN
I_{OUT} = 0A, FCCM



400µs/div.

Start-Up through VIN
I_{OUT} = 2A



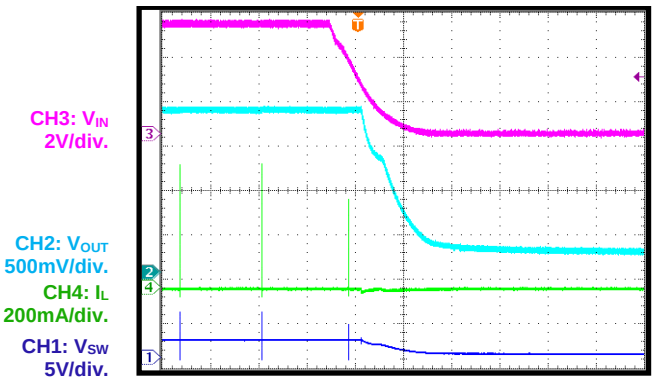
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

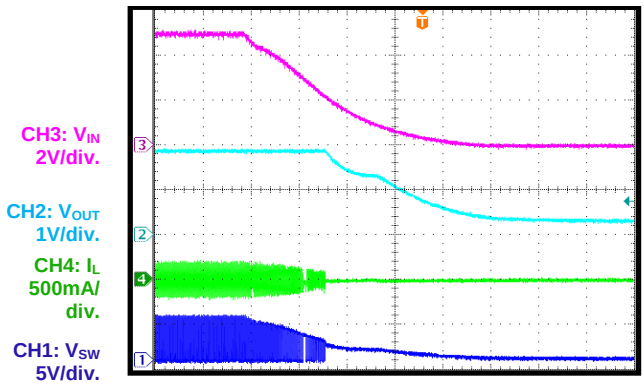
I_{OUT} = 0A, AAM mode



10ms/div.

Shutdown through VIN

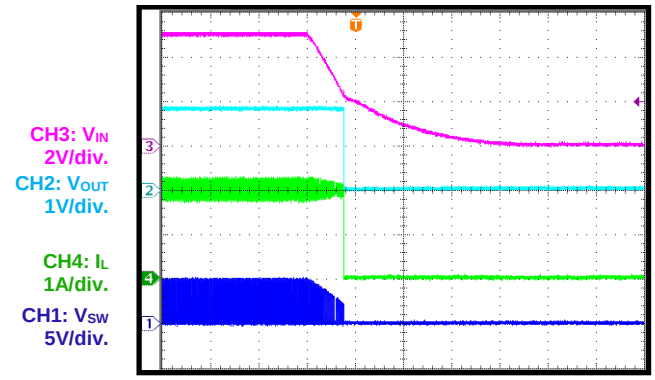
I_{OUT} = 0A, FCCM



4ms/div.

Shutdown through VIN

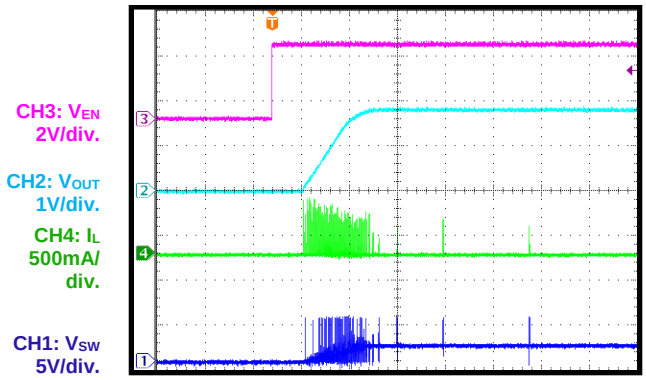
I_{OUT} = 2A



4ms/div.

Start-Up through EN

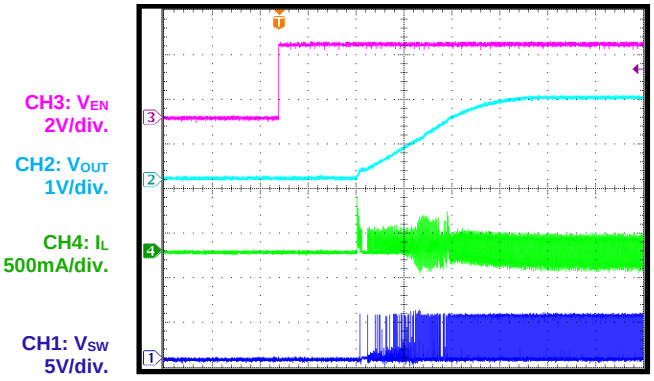
I_{OUT} = 0A, AAM mode



1ms/div.

Start-Up through EN

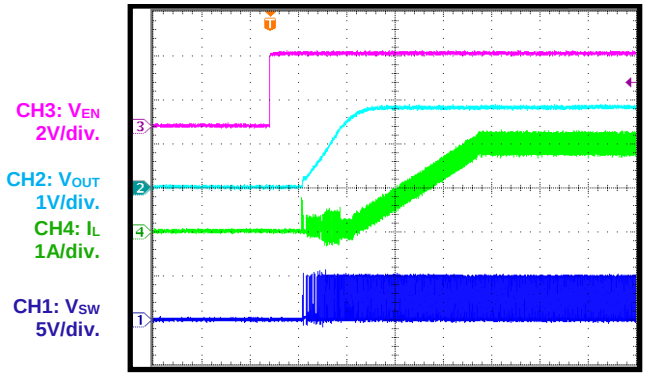
I_{OUT} = 0A, FCCM



400µs/div.

Start-Up through EN

I_{OUT} = 2A



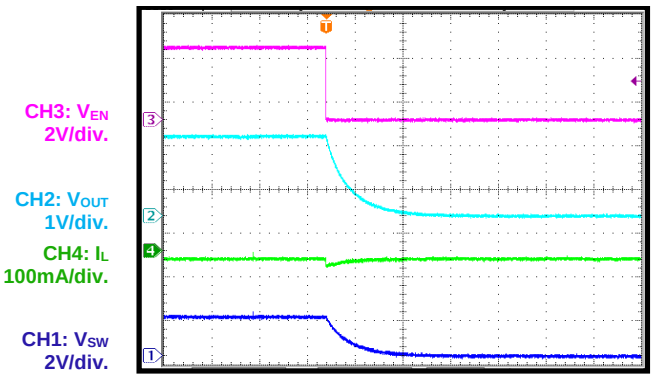
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through EN

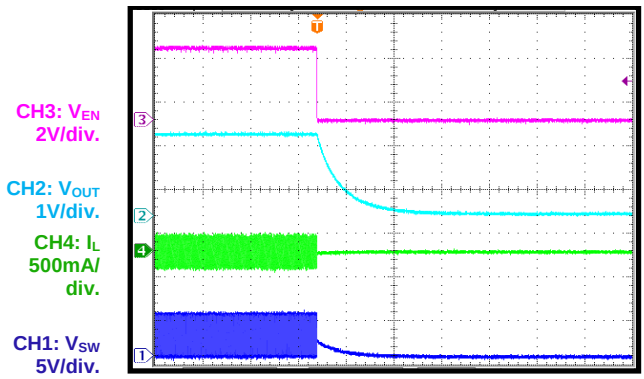
I_{OUT} = 0A, AAM mode



10ms/div.

Shutdown through EN

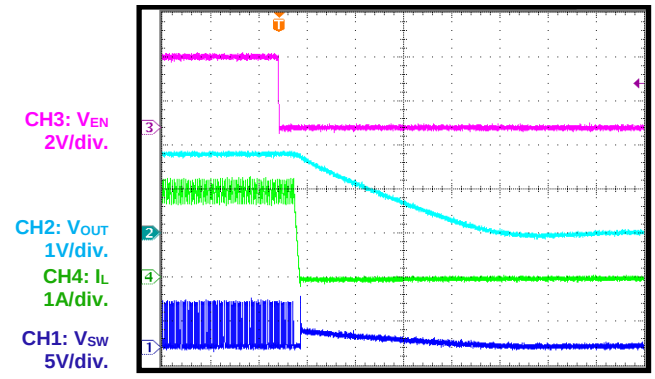
I_{OUT} = 0A, FCCM



10ms/div.

Shutdown through EN

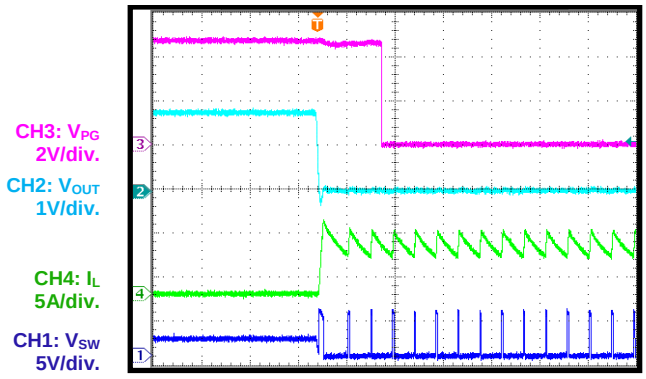
I_{OUT} = 2A



10µs/div.

SCP Entry

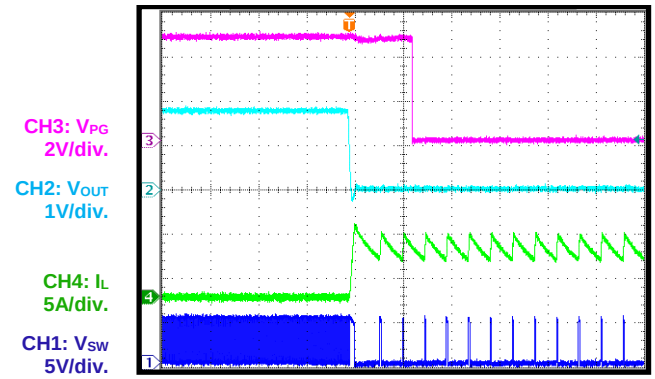
I_{OUT} = 0A, AAM mode



20µs/div.

SCP Entry

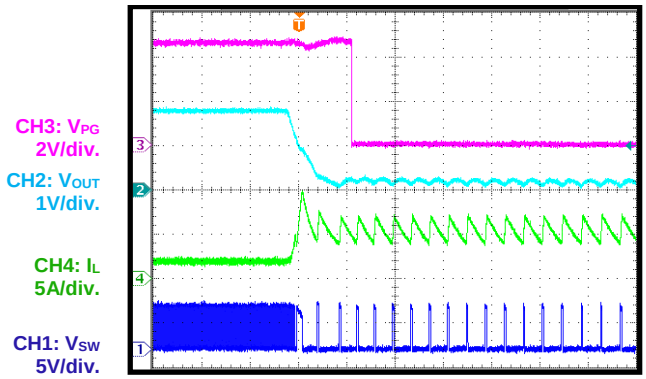
I_{OUT} = 0A, FCCM



20µs/div.

SCP Entry

I_{OUT} = 2A



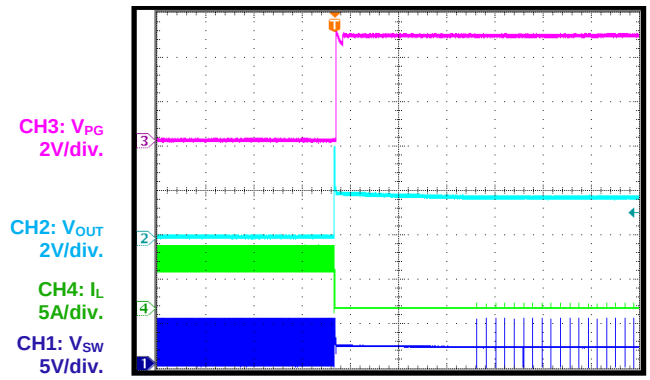
20µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

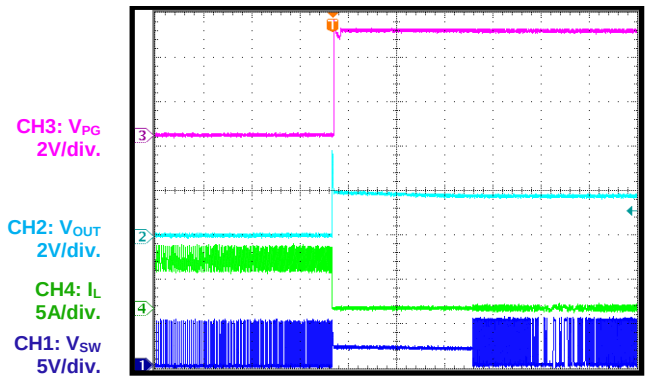
SCP Recovery

I_{OUT} = 0A, AAM mode



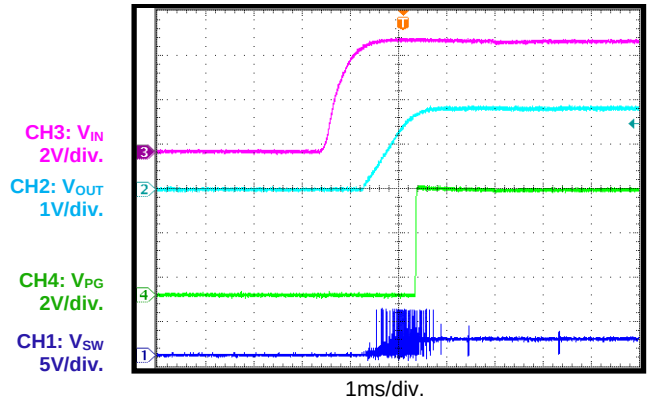
SCP Recovery

I_{OUT} = 0A, FCCM



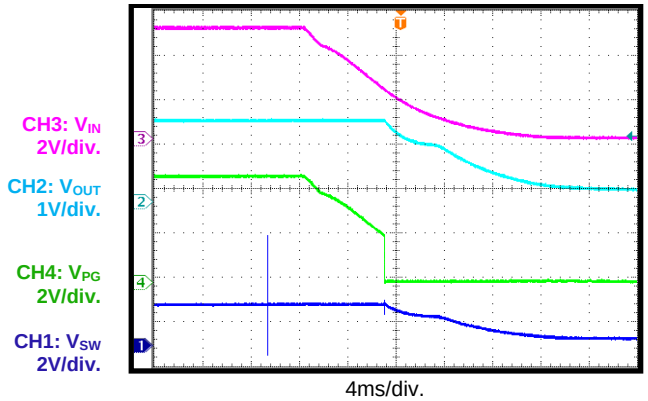
PG Start-Up through VIN

I_{OUT} = 0A, AAM mode



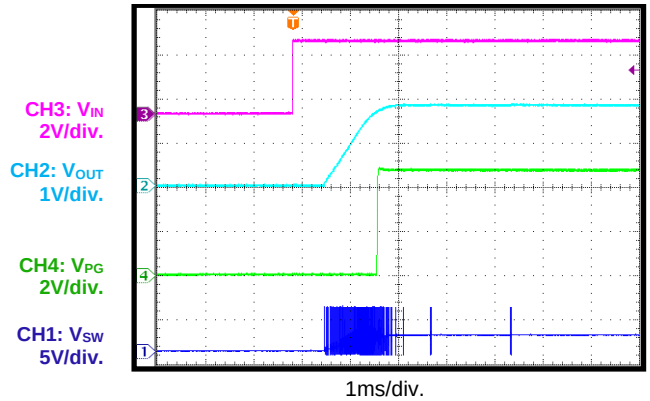
PG Shutdown through VIN

I_{OUT} = 0A, AAM mode



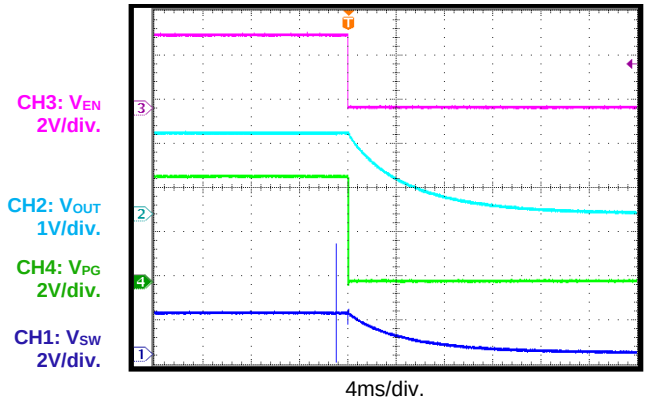
PG Start-Up through EN

I_{OUT} = 0A, AAM mode



PG Shutdown through EN

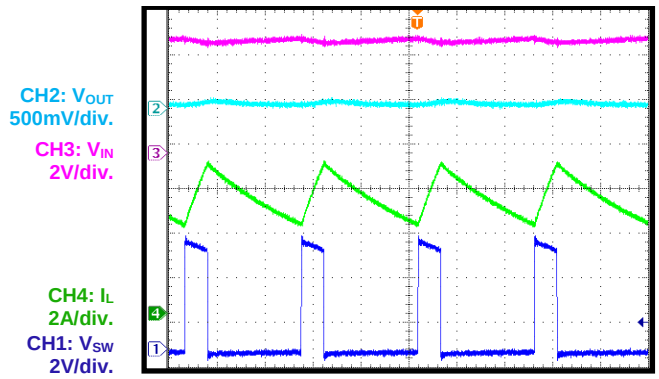
I_{OUT} = 0A, AAM mode



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

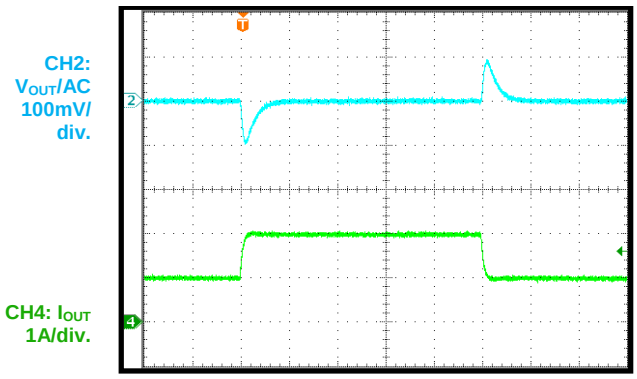
SCP Steady State



2µs/div.

Load Transient

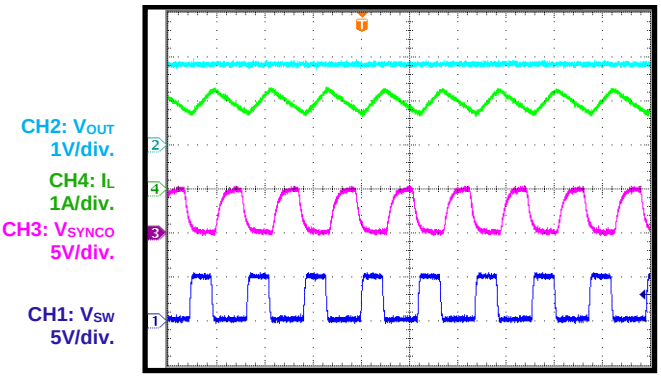
IOUT = 1A to 2A, 1.6A/µs



100µs/div.

SYNCO

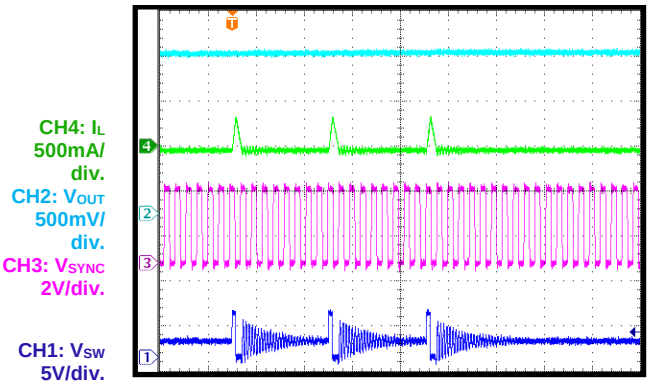
IOUT = 2A



400ns/div.

SYNC Input

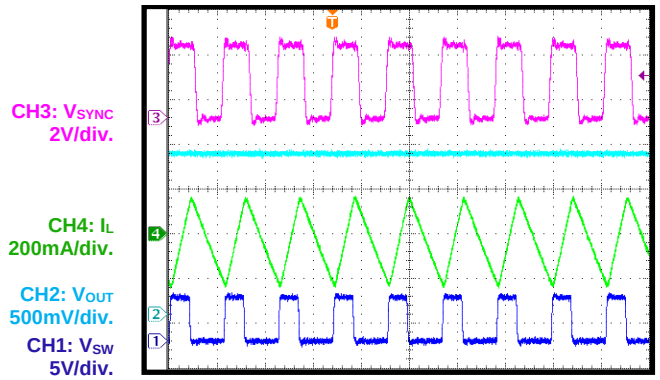
IOUT = 0A, SYNC clock = 2.2MHz, AAM mode



2µs/div.

SYNC Input

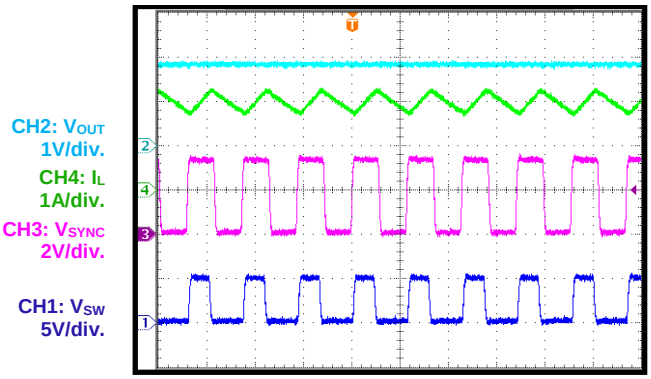
IOUT = 0A, SYNC clock = 2.2MHz, FCCM



400ns/div.

SYNC Input

IOUT = 2A



400ns/div.

FUNCTIONAL BLOCK DIAGRAM

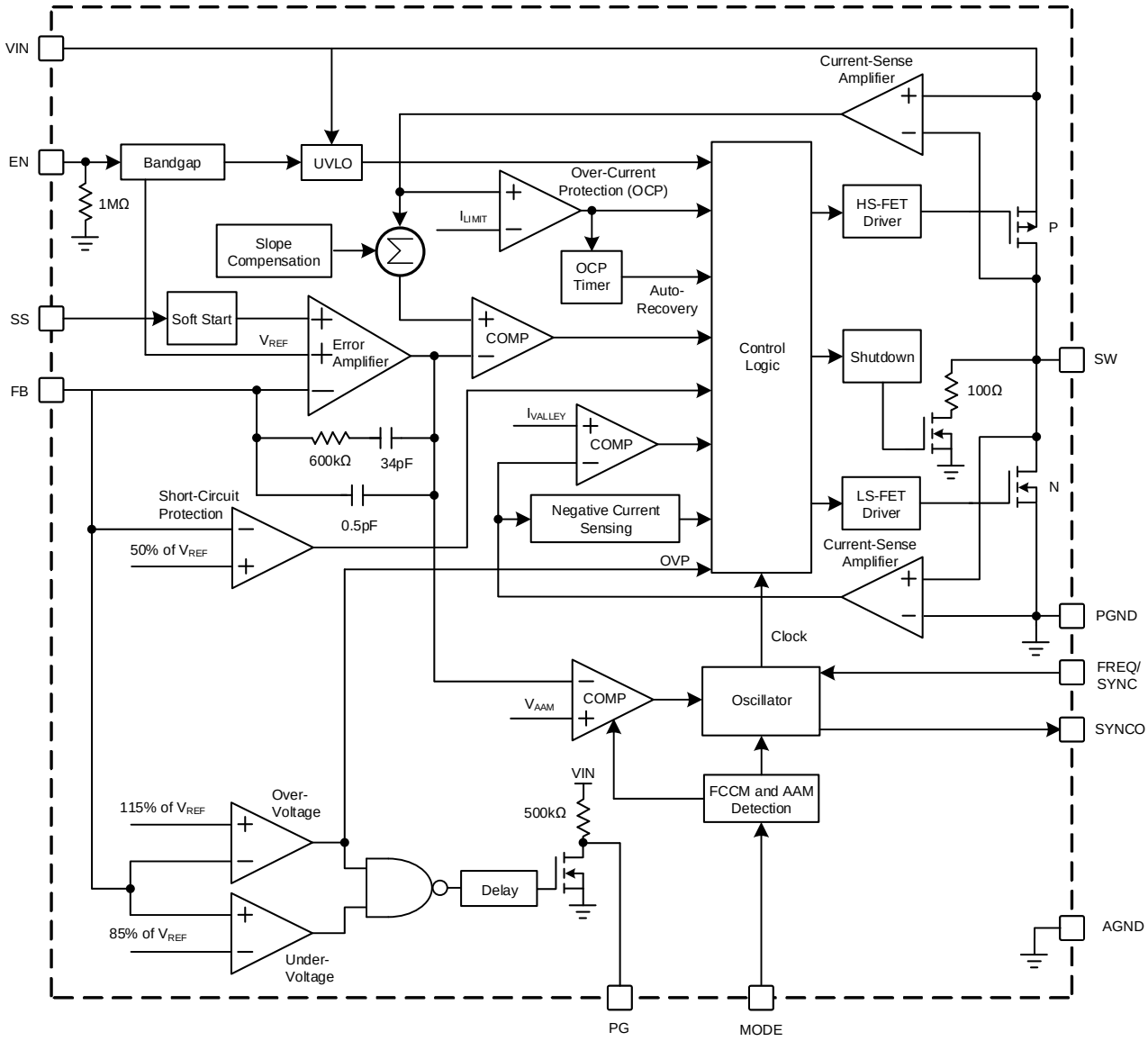


Figure 1: Functional Block Diagram

OPERATION

The MPQ2123 is a fully integrated, synchronous, rectified, non-isolated, switch-mode step-down converter. It can achieve up to 2A of continuous output current (I_{OUT}) across a 2.7V to 6V input voltage (V_{IN}) range, with excellent load and line regulation across an ambient temperature range of -40°C to +125°C. The output voltage (V_{OUT}) can be regulated to as low as 0.606V.

The MPQ2123 employs peak current control mode and internal compensation for fast transient response and cycle-by-cycle current limiting.

The MPQ2123 is ideal for low-voltage portable applications where efficiency and small size are critical. It can operate at a switching frequency (f_{SW}) up to 2.2MHz. This allows a smaller inductor to be used, while also providing high efficiency. In advanced asynchronous modulation (AAM) mode, the MPQ2123 provides efficient high power conversion under light-load conditions.

Forced Continuous Conduction Mode (FCCM)

To make the converter operate in forced continuous conduction mode (FCCM), pull the MODE pin above 1.2V. To regulate V_{OUT} during FCCM, the MPQ2123 operates in fixed-frequency peak current control mode, regardless of I_{OUT}.

An internal clock initiates the FCCM cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on and the inductor current (I_L) rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier (EA). V_{COMP} is determined by the difference between the feedback voltage (V_{FB}) and the internal, high-precision reference voltage (V_{REF}). V_{COMP} determines how much energy should be transferred to the load. The higher the load current, the higher V_{COMP} will be.

If the HS-FET is off, then the low-side MOSFET (LS-FET) turns on and remains on until the next clock cycle starts. While the LS-FET is on and the HS-FET is off, I_L flows through the LS-FET.

To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from being turned on at the same time. For each on/off period in an FCCM cycle, the HS-FET remains on or off for the minimum on time (t_{ON}).

Advanced Asynchronous Modulation (AAM) Mode

To force the converter into advanced asynchronous modulation (AAM) mode, pull the MODE pin below 0.4V. There is an internally fixed AAM threshold voltage (V_{AAM}). Under light-load conditions, V_{COMP} is lower than V_{AAM}.

If V_{COMP} exceeds V_{AAM}, then the MPQ2123 enters discontinuous conduction mode (DCM) with a fixed frequency until I_L reaches 0A. If the load decreases further or there is no load to force V_{COMP} below V_{AAM}, then the internal clock is blocked and the MPQ2123 skips pulses. During this time, V_{FB} drops below V_{REF}, and V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset and the crossover time is used as the benchmark for the next clock. This control scheme improves efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As I_{OUT} increases under light-load conditions, both f_{SW} and V_{COMP} increase.

If I_{OUT} exceeds the critical level once V_{COMP} exceeds V_{AAM}, then the MPQ2123 resumes FCCM (see Figure 2).

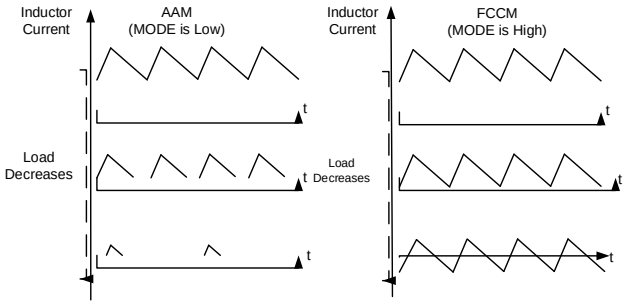


Figure 2: AAM and FCCM Modes

Enable (EN) Control

The EN pin enables and disables the entire chip. EN is a remote signal referenced to ground. The remote EN control operates with a positive logic that is compatible with popular logic devices. Positive logic implies that if V_{IN} exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), then pulling EN above 1.2V turns the converter on. Pull EN to ground or float EN

to turn the converter off. There is an internal 1MΩ resistor connected between EN and ground.

Oscillator and SYNC Function

The MPQ2123's oscillating frequency can be configured via an external frequency resistor (R_{FREQ}). R_{FREQ} should be placed between the FREQ pin and ground, as close to the device as possible.

To select the R_{FREQ} value, see the Switching Frequency vs. Frequency Resistance curve in the Typical Performance Characteristics section on page 10.

The FREQ pin can also synchronize the internal oscillator rising edge to an external clock's falling edge. The amplitude of the SYNC clock determines the internal logic. Choose a proper amplitude for the SYNC clock to drive the internal logic (see the Electrical Characteristics section on page 5). It is recommended to keep the external SYNC frequency between 300kHz and 2.2MHz. There is no pulse width requirement; however, there is always parasitic capacitance on the pad. Therefore, if the pulse width is too short, then a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application. Be sure to add the external SYNC clock (300kHz to 2.2MHz) before the device starts up, and to keep the SYNC clock on until the device shuts down. During operation, the SYNC signal must not be constant high, constant low, or in a transition from high to low or vice versa.

The MPQ2123 also has a SYNCO pin that can output a 180° phase-shifted clock. The SYNCO signal can be used to synchronize other devices to the same operation frequency but the opposite phase. This reduces the total input current ripple.

Soft Start (SS) and Output Discharge

The MPQ2123 has soft start (SS). To avoid overshoot during start-up, SS ramps up V_{OUT} in a controlled slew rate as EN goes high.

Once SS begins, an internal current source charges the external soft-start capacitor (C_{SS}). If the SS voltage (V_{SS}) drops below V_{REF}, then V_{SS} overrides V_{REF} as the EA reference. If V_{SS} exceeds V_{REF}, then V_{REF} acts as the reference. Once SS is complete, the MPQ2123 enters steady state and begins normal operation. The SS pin can be used for tracking and sequencing.

The soft-start time (t_{SS}) set by C_{SS} can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external soft-start capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the 4μA internal soft-start charge current.

If the SS pin is floating, then the soft-start time follows the internally set default 1ms time ($t_{SS\_DEFAULT}$).

If the MPQ2123 shuts down, then V_{OUT} is discharged to GND via a 100Ω internal resistor that is in parallel with the LS-FET.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up (which means the output has a pre-biased voltage), then the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

100% Duty Cycle

The MPQ2123 can operate with 100% duty cycle, which can extend battery life. If V_{IN} is too low to maintain output regulation, then the HS-FET turns on to achieve the maximum V_{OUT}.

Power Good (PG) Indicator

The MPQ2123 has power good (PG) indication. The PG pin is the open drain of a MOSFET. In the presence of V_{IN}, the MOSFET turns on so that PG is pulled to ground before SS is ready. If V_{OUT} is within ±15% of the rated voltage set by FB, then PG is pulled up to V_{IN} via an internal resistor after a delay time. If V_{FB} moves outside the ±15% range with a hysteresis, then the device pulls PG low to indicate an output failure status.

Over-Current Protection (OCP)

The MPQ2123 features cycle-by-cycle peak current limit control. I_L is monitored while the HS-FET is on. Once I_L reaches the current limit, the HS-FET turns off. Then the LS-FET turns on to discharge the energy and I_L decreases. The HS-FET does not turn on again until I_L falls below the valley current limit threshold. This prevents I_L from running away and potentially damaging the

components.

If the valley current limit is triggered, then the over-current protection (OCP) timer begins. The OCP timer is set at 100µs.

Short-Circuit Protection (SCP)

If the valley current limit is reached within one cycle of the 100µs time period, then short-circuit protection (SCP) is triggered. If a short circuit occurs, then the MPQ2123 immediately reaches its current limit. Meanwhile, V_{OUT} drops until V_{FB} is below 50% of V_{REF} (0.606V). The device considers this an output dead short, and triggers SCP.

In SCP, I_L is monitored while the HS-FET is on. Once I_L reaches the current limit, the HS-FET turns off. Then the LS-FET turns on to discharge the energy and I_L decreases. The HS-FET does not turn on again until I_L falls below the valley current limit threshold. The device repeats this operation until the short circuit disappears and the output returns to the regulation level. SCP prevents I_L from running away and potentially damaging the components.

Over-Voltage Protection (OVP)

The MPQ2123 monitors V_{OUT} through FB to detect any output over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF} (0.606V), then over-voltage protection (OVP) is triggered and the LS-FET turns on to discharge V_{OUT} until I_L drops to 0A. Then LS-FET turns off, and the output is discharged via a 100Ω internal resistor connected in parallel with the LS-FET. The HS-FET remains off during this operation. The device does not begin switching again until the output is within regulation again.

Under-Voltage Lockout Protection (UVLO)

The MPQ2123 includes input under-voltage lockout (UVLO) protection to ensure there is always reliable output power. Assuming EN is active, the MPQ2123 starts up once V_{IN} exceeds the UVLO rising threshold.

The device shuts down once V_{IN} drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient supply voltage. V_{IN} UVLO is a non-latch protection.

Thermal Shutdown

The MPQ2123 employs thermal shutdown. The IC's junction temperature (T_J) is monitored internally. Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If T_J exceeds the maximum temperature threshold (typically 170°C), then the converter shuts down. Thermal shutdown is a non-latch protection. There is a 25°C hysteresis. Once T_J drops to about 145°C, the MPQ2123 initiates an SS and resumes normal operation.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, then the MPQ2123 starts up. The reference block starts up first, generating a stable V_{REF} and current. Then the internal regulator turns on to provide a stable supply for the remaining circuitries.

To blank any start-up errors, an internal timer keeps the power MOSFET off for about 50µs while the internal supply rail is pulled up. If the soft-start (SS) block is on, then the soft-start output is held low to ensure the rest of the circuitries are ready, at which point it slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} UVLO, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is turned off.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets V_{OUT} (see Figure 3). The feedback resistor (R4) must account for both stability and dynamic response, so it cannot be too large or too small. R4 is about 100kΩ. R5 can be calculated with Equation (2):

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

It is highly recommended to use a T-type feedback network (see Figure 3).

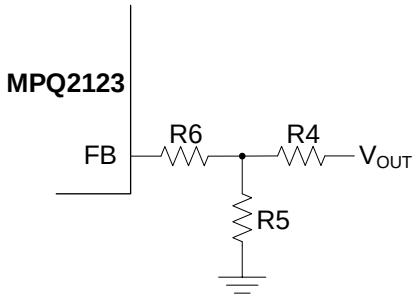


Figure 3: T-Type Feedback Network

R6 and R4 are used to set the loop bandwidth. A greater (R6 + R4) value leads to a lower bandwidth. To ensure loop stability, it is recommended to limit the bandwidth to about 10% of the switching frequency (f_{SW}).

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. Change the resistance of R_T for loop stability if necessary.

Table 1: Resistor Values for Typical Output Voltages

V_{OUT} (V)	R6 (kΩ)	R4 (kΩ)	R5 (kΩ)
1.2	100	100 (1%)	100 (1%)
1.5	100	100 (1%)	66.5 (1%)
1.8	100	100 (1%)	49.9 (1%)
2.5	100	100 (1%)	31.6 (1%)
3.3	100	100 (1%)	22.1 (1%)

Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching input voltage. For a default 2.1MHz application, a 0.47µH to 1.5µH inductor is recommended. For improved efficiency, choose an inductor with a small DC resistance (below 15mΩ).

When setting the frequency or SYNC function, the inductance may need to be increased as the frequency decreases. A larger-value inductor results in less ripple current and lower output ripple voltage. However, a larger-value inductor is physically larger, and has a higher series resistance and lower saturation current. A good rule for determining the inductance is to have the inductor ripple current be approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. The inductance (L) can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current (I_{LP}) can be estimated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. Other capacitors, including Y5V and Z5U, must not be used as these types of capacitors lose too much capacitance with frequency, temperature, and bias voltage.

Place the input capacitors as close to VIN as possible. For most applications, a 22µF capacitor is sufficient. For applications with a higher V_{OUT}, use a 47µF capacitor to improve system stability. For a small solution size, it is better to choose a proper package size capacitor with a voltage rating that is compliant with the

with a voltage rating that is compliant with the input specifications.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The ripple current rating should exceed the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality 0.1µF ceramic capacitor, placed as close to the IC as possible. The input capacitance determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Low-ESR ceramic capacitors are recommended for their smaller size and ability to keep the output voltage ripple low.

Electrolytic and polymer capacitors may also be used. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Another consideration regarding the output capacitance is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT}, which causes its voltage to rise. To achieve an appropriate overshoot relative to the regulated voltage, the output capacitance (C_{OUT}) can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

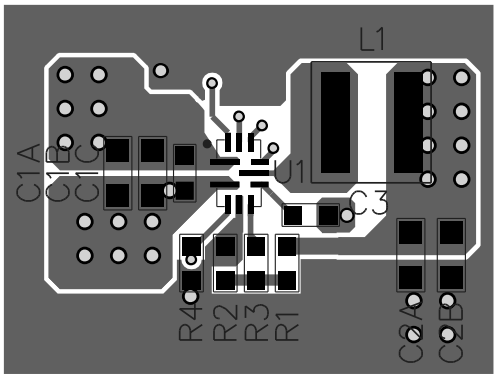
Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot. After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2123 can be optimized for a wide range of capacitance and ESR values.

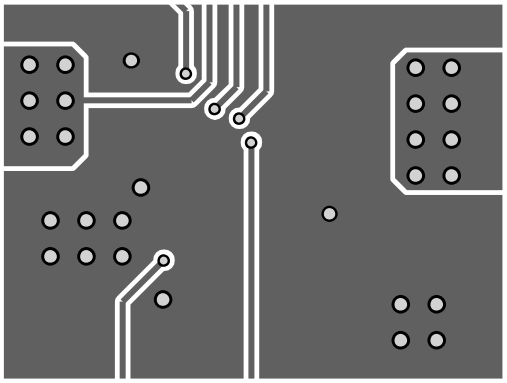
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

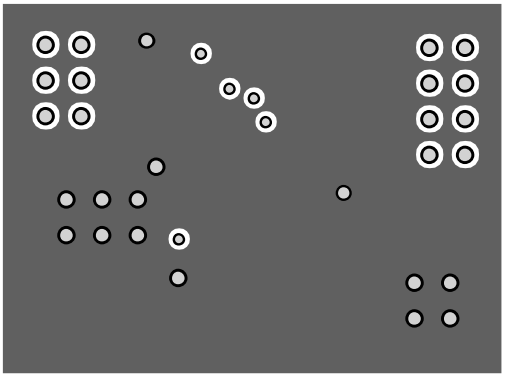
1. Connect the high-current paths (GND, VIN, and SW) with short, direct, and wide traces, placed as close to the device as possible.
2. Place input capacitors as close to VIN as possible to minimize high-frequency noise.
3. Place the feedback resistor divider as close to FB as possible.
4. Route the FB trace away from the switching node.
5. To improve thermal performance, connect the bottom VIN and SW pads to a large copper area.
6. To minimize conduction loss and thermal stress, use the large copper areas as power planes (VIN, SW, OUT, and GND).
7. Use multiple vias to connect the power planes to the internal layers.



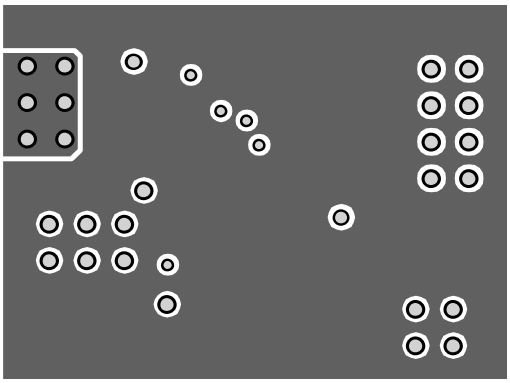
Top Silk and Top Layer



Mid-Layer 2



Mid-Layer 1



Bottom Layer and Bottom Silk

Figure 4: Recommended PCB Layout (7)

Note:

7) The recommended PCB layout is based on the Typical Application Circuit (see Figure 5 on page 23).

TYPICAL APPLICATION CIRCUITS

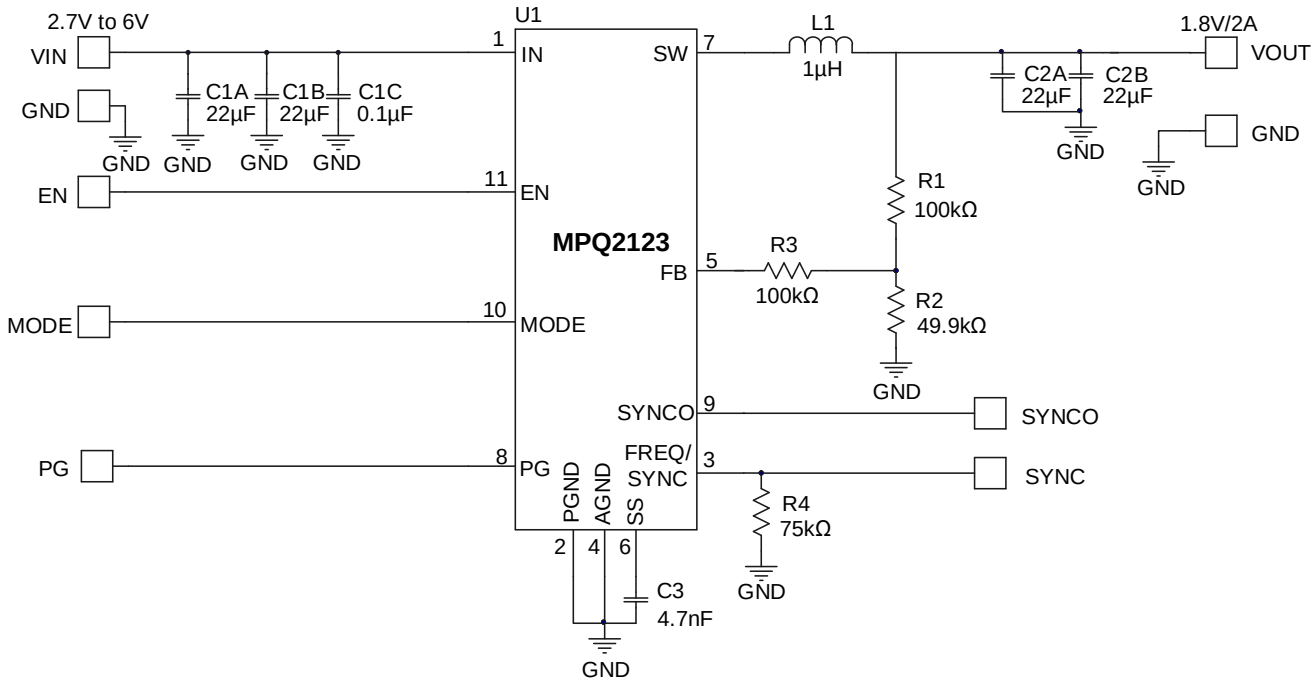


Figure 5: Typical Application Circuit, V_{OUT} = 1.8V, I_{OUT} = 2A

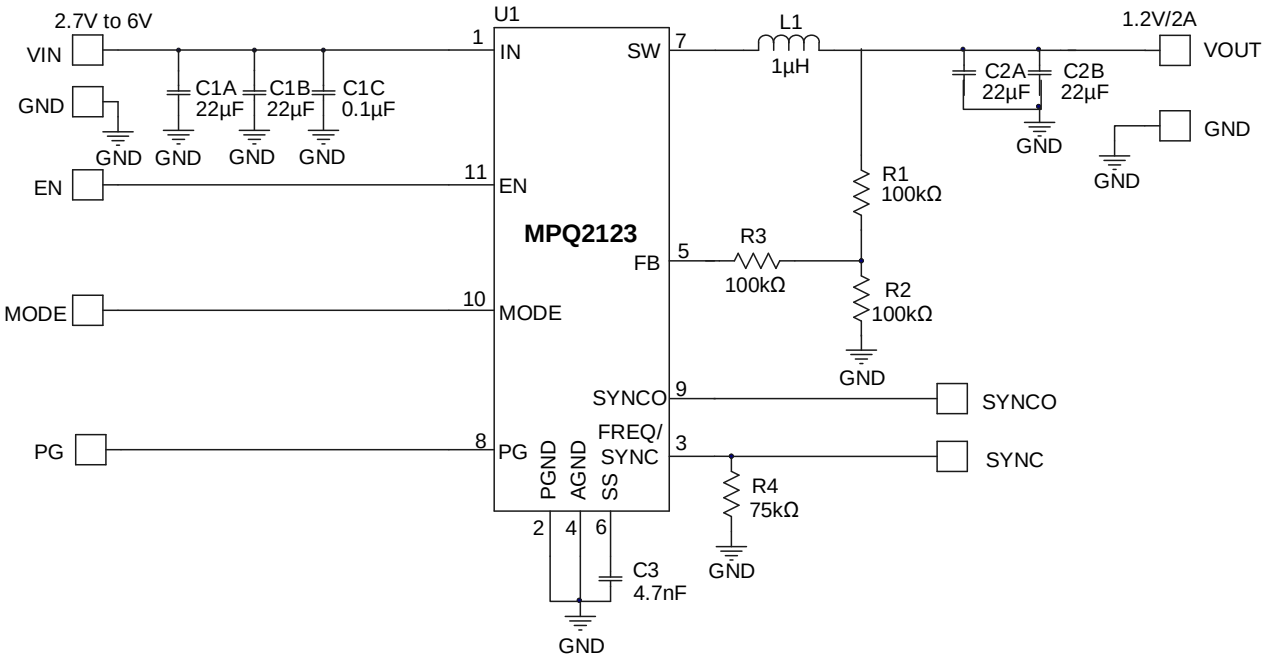
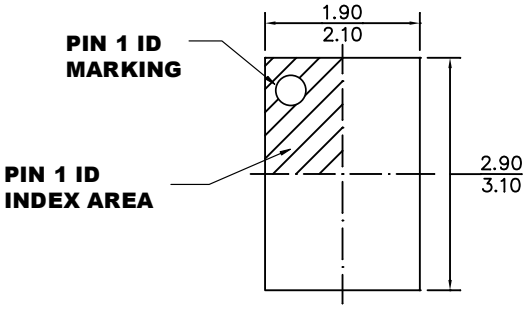


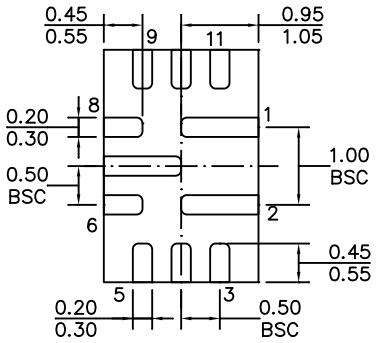
Figure 6: Typical Application Circuit, V_{OUT} = 1.2V, I_{OUT} = 2A

PACKAGE INFORMATION

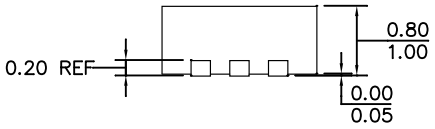
QFN-11 (2mmx3mm)



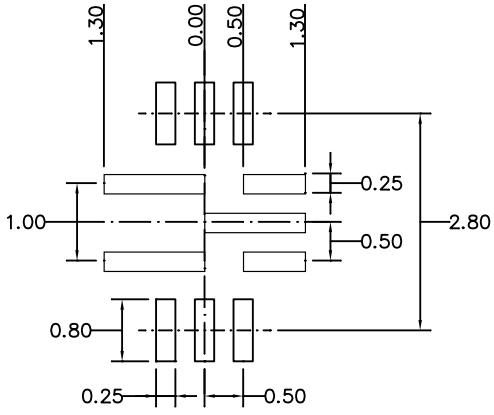
TOP VIEW



BOTTOM VIEW



SIDE VIEW

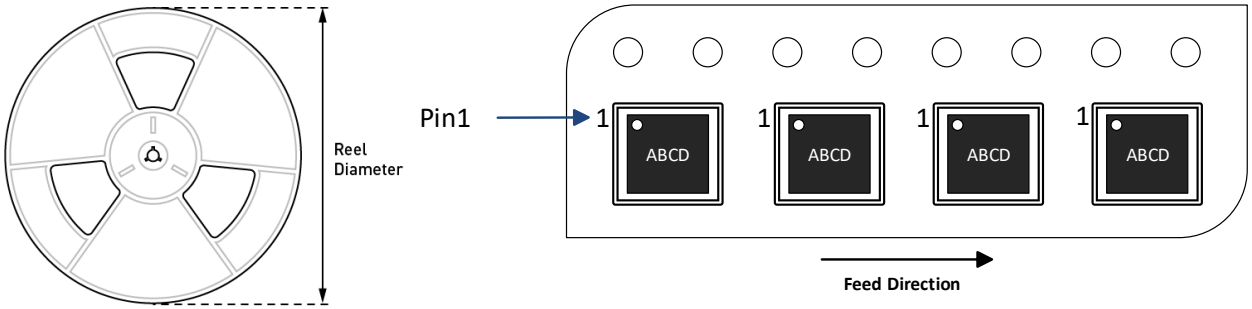


RECOMMENDED LAND PATTERN

NOTE:

1) THE LAND PATTERNS OF PINS 1, 2, AND 7 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.1 MILLIMETERS MAXIMUM.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2123GD-AEC1–Z	QFN-11 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/20/2021	Initial Release	-