



## Product Change Notification / SYST-05KSKC077

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### Date:

06-Jan-2022

### Product Category:

8-bit Microcontrollers

### PCN Type:

Document Change

### Notification Subject:

ERRATA - ATtiny424/426/427/824/826/827 Silicon Errata and Data Sheet Clarification

### Affected CPNs:

[SYST-05KSKC077\\_Affected\\_CPN\\_01062022.pdf](#)

[SYST-05KSKC077\\_Affected\\_CPN\\_01062022.csv](#)

### Notification Text:

SYST-05KSKC077

Microchip has released a new Product Documents for the ATtiny424/426/427/824/826/827 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [ATtiny424/426/427/824/826/827 Silicon Errata and Data Sheet Clarification](#).

### Notification Status: Final

**Description of Change:** 1. Editorial update: Notes

2. Updated errata:

- Silicon revision B does not apply to this device. Silicon revision A is the initial release:
  - Removed silicon revision B from Silicon Issues Summary and all Affected Versions tables.
  - Replaced errata applicable to silicon revision B by errata applicable to silicon revision A.

3. Added Erratum: ADC: 2.2.1. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 06 January 2022

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[ATtiny424/426/427/824/826/827 Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

ATTINY424-SSF  
ATTINY824-SSF  
ATTINY424-XF  
ATTINY824-XF  
ATTINY426-XF  
ATTINY826-XF  
ATTINY426-SF  
ATTINY826-SF  
ATTINY426-MF  
ATTINY826-MF  
ATTINY427-MF  
ATTINY827-MF  
ATTINY424-SSU  
ATTINY824-SSU  
ATTINY424-XU  
ATTINY824-XU  
ATTINY426-XU  
ATTINY826-XU  
ATTINY426-SU  
ATTINY826-SU  
ATTINY426-MU  
ATTINY826-MU  
ATTINY427-MU  
ATTINY827-MU  
ATTINY424-SSUR  
ATTINY824-SSUR  
ATTINY424-XUR  
ATTINY824-XUR  
ATTINY426-XUR  
ATTINY826-XUR  
ATTINY426-SUR  
ATTINY826-SUR  
ATTINY426-MUR  
ATTINY826-MUR  
ATTINY427-MUR  
ATTINY827-MUR  
ATTINY424-SSFR  
ATTINY824-SSFR  
ATTINY424-XFR  
ATTINY824-XFR  
ATTINY426-XFR  
ATTINY826-XFR  
ATTINY426-SFR  
ATTINY826-SFR  
ATTINY426-MFR  
ATTINY826-MFR

ATTINY427-MFR

ATTINY827-MFR



# ATtiny424/426/427/824/826/827

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## Silicon Errata and Data Sheet Clarifications

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The ATtiny424/426/427/824/826/827 devices you have received conform functionally to the current device data sheet ([www.microchip.com/DS40002311](http://www.microchip.com/DS40002311)), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny424/426/427/824/826/827 devices.

**Notes:**

- This document summarizes all the silicon errata issues from all the silicon revisions, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet ([www.microchip.com/DS40002311](http://www.microchip.com/DS40002311)) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

## 1. Silicon Issue Summary

### Legend

- Erratum is not applicable.

X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
ADC	2.2.1. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode	X
CCL	2.3.1. The CCL Must be Disabled to Change the Configuration of a Single LUT	X
TCA	2.4.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.5.1. CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.6.1. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X

## 2. Silicon Errata Issues

### 2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

### 2.2 ADC - Analog-to-Digital Converter

#### 2.2.1 ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode

If the Low Latency bit (LOWLAT in ADCn.CTRLA) is '1', the ADC stays active when the device enters Power-Down or Standby sleep modes. If the Free-Running bit (FREERUN in ADCn.CTRLF) is '1', the ADC continues to run in Standby sleep mode even if the Run in Standby bit (RUNSTDBY in ADCn.CTRLA) is '0'. In both cases, the interrupts will not trigger when the device enters Power-Down or Standby sleep mode.

##### Work Around

None.

##### Affected Silicon Revisions

Rev. A
X

### 2.3 CCL - Configurable Custom Logic

#### 2.3.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

##### Work Around

None

##### Affected Silicon Revisions

Rev. A
X

### 2.4 TCA - 16-Bit Timer/Counter Type A

#### 2.4.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMode in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

##### Work Around

None.

**Affected Silicon Revisions**

Rev. A
X

**2.5 TCB - 16-Bit Timer/Counter Type B****2.5.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode**

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

**Work Around**

Use 16-bit register access. Refer to the data sheet for further information.

**Affected Silicon Revisions**

Rev. A
X

**2.6 USART - Universal Synchronous and Asynchronous Receiver and Transmitter****2.6.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode**

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

**Work Around**

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

**Affected Silicon Revisions**

Rev. A
X



### 3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet ([www.microchip.com/DS40002311](http://www.microchip.com/DS40002311)).

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

#### 3.1 None

There are no known data sheet clarifications as of this publication date.

## 4. Document Revision History

**Note:** The document revision is independent of the silicon revision.

### 4.1 Revision History

Doc. Rev.	Date	Comments
B	01/2022	<ul style="list-style-type: none"><li>• Editorial update:<ul style="list-style-type: none"><li>– <a href="#">Notes</a></li></ul></li><li>• Updated errata:<ul style="list-style-type: none"><li>– Silicon revision B does not apply to this device. Silicon revision A is the initial release:<ul style="list-style-type: none"><li>• Removed silicon revision B from <i>Silicon Issues Summary</i> and all <i>Affected Versions</i> tables</li><li>• Replaced errata applicable to silicon revision B by errata applicable to silicon revision A</li></ul></li></ul></li><li>• Added Erratum:<ul style="list-style-type: none"><li>– ADC: <a href="#">2.2.1. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode</a></li></ul></li></ul>
A	04/2021	Initial document release

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