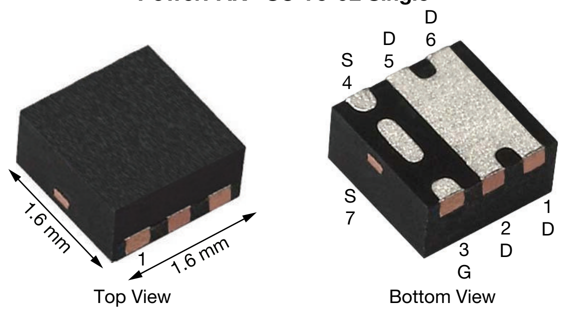
P-Channel 30 V (D-S) MOSFET

PowerPAK® SC-75-6L Single



Marking code: BP

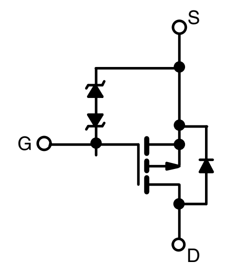
FEATURES

- Thermally enhanced PowerPAK® SC-75 package
  - Small footprint area
  - Low on-resistance
  - Thin 0.75 mm profile
- Typical ESD protection (MOSFET): 1500 V (HBM)
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs, and mobile computing
  - Battery charger switch
  - Buck converter
  - Power management
  - Load switch



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.065
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.080
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.125
Q_g typ. (nC)	6.6
I_D (A) [a]	-4.5
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SC-75
Lead (Pb)-free and halogen-free	SiB4317EDK-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 12	V
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	-4.5 [a]	A
	T_C = 70 °C		-4.5 [a]	
	T_A = 25 °C		-4.3 [b, c]	
	T_A = 70 °C		-3.5 [b, c]	
Pulsed drain current (t = 300 μs)		I_{DM}	-15	
Continuous source-drain diode current (MOSFET diode conduction)	T_C = 25 °C	I_S	-4.5 [a]	
	T_A = 25 °C		-1.63 [b, c]	
Maximum power dissipation	T_C = 25 °C	P_D	10	W
	T_C = 70 °C		6.4	
	T_A = 25 °C		1.95 [b, c]	
	T_A = 70 °C		1.25 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

Notes

a. Package limited

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum junction-to-ambient [a, b]	$t \leq 5$ s	R_{thJA}	51	64	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	10	12.5	

Notes

a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 100 °C/W

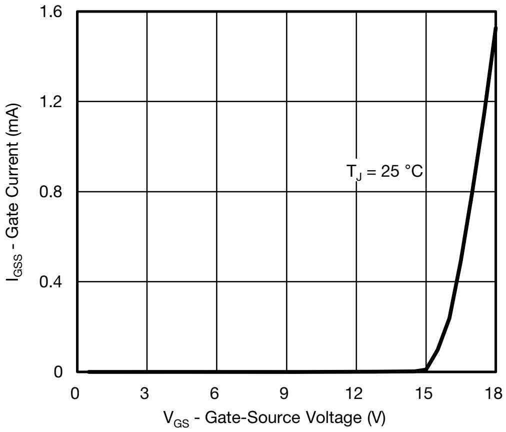
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-23	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = -250 µA	-0.6	-	-1.3	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 0.5	µA
		V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 10	
Zero gate voltage drain current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	-	-	-1	
		V_{DS} = -30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -3 A	-	0.054	0.065	Ω
		V_{GS} = -4.5 V, I_D = -2 A	-	0.065	0.080	
		V_{GS} = -2.5 V, I_D = -1 A	-	0.095	0.125	
Forward transconductance [a]	g_{fs}	V_{DS} = -10 V, I_D = -3 A	-	9	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	-	600	-	pF
Output capacitance	C_{oss}		-	55	-	
Reverse transfer capacitance	C_{rss}		-	50	-	
Total gate charge	Q_g	V_{DS} = -15 V, V_{GS} = -10 V, I_D = -4.2 A	-	14	23	nC
		V_{DS} = -5 V, V_{GS} = -4.5 V, I_D = -4.2 A	-	6.6	10	
Gate-source charge	Q_{gs}		-	1.3	-	
Gate-drain charge	Q_{gd}		-	2	-	
Gate resistance	R_g	f = 1 MHz	1.1	5.5	11	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 4.4 Ω $I_D \cong$ -3.4 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	20	40	ns
Rise time	t_r		-	20	40	
Turn-off delay time	$t_{d(off)}$		-	23	45	
Fall time	t_f		-	10	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 4.4 Ω $I_D \cong$ -3.4 A, V_{GEN} = -10 V, R_g = 1 Ω	-	10	20	
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	25	50	
Fall time	t_f		-	7	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	-4.5	A
Pulse diode forward current	I_{SM}		-	-	-15	
Body diode voltage	V_{SD}	I_S = -3.4 A, V_{GS} = 0 V	-	-0.9	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -3.4 A, di/dt = 100 A/µs, T_J = 25 °C	-	16	30	ns
Body diode reverse recovery charge	Q_{rr}		-	8	15	nC
Reverse recovery fall time	t_a		-	9	-	ns
Reverse recovery rise time	t_b		-	7	-	

Notes

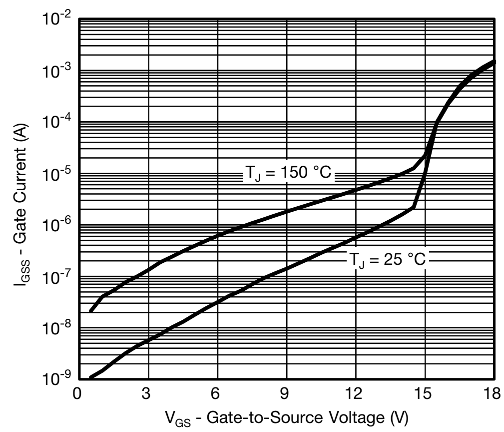
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

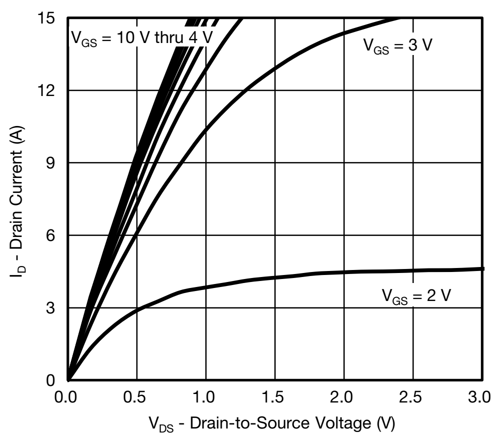
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



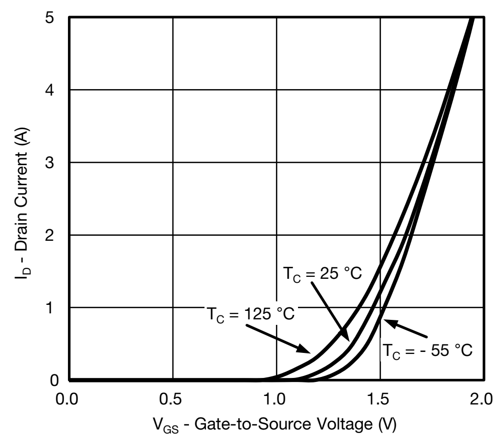
Gate-Source Voltage vs. Gate Current



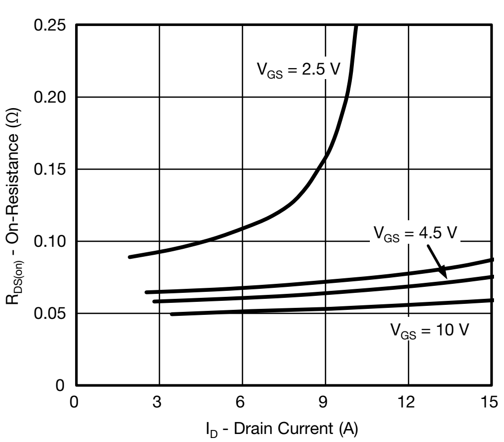
Gate-Source Voltage vs. Gate Current



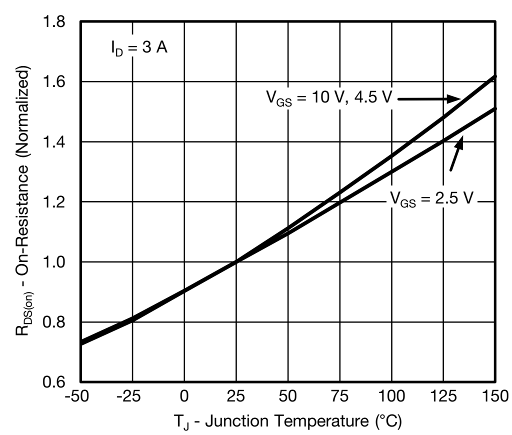
Output Characteristics



Transfer Characteristics

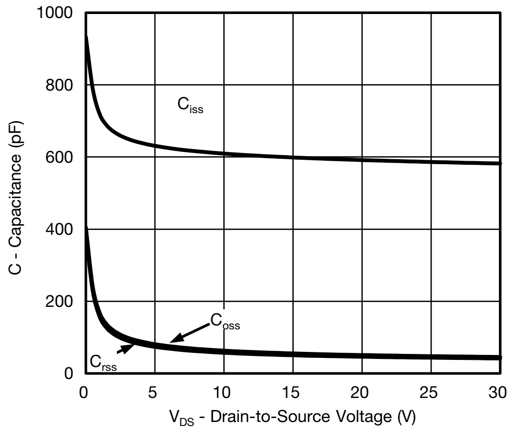


On-Resistance vs. Drain Current and Gate Voltage

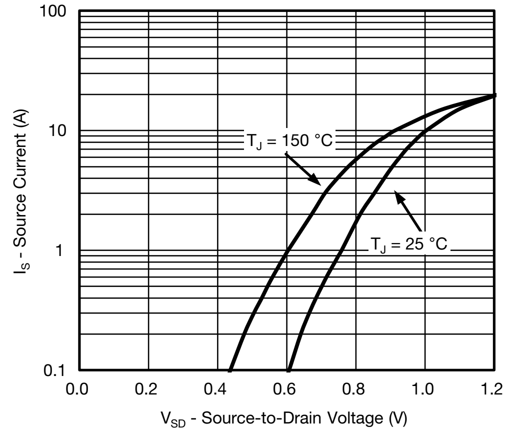


On-Resistance vs. Junction Temperature

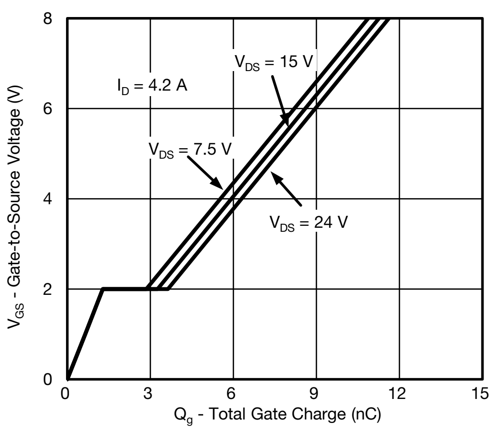
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



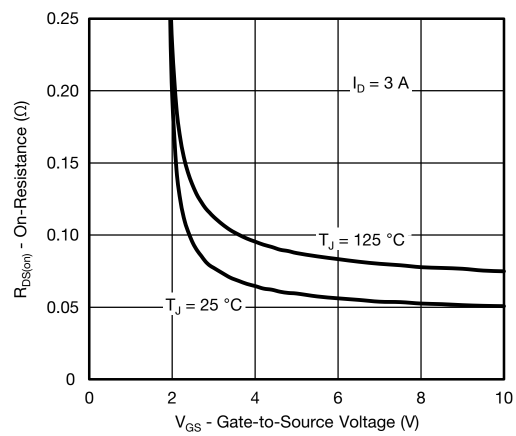
Capacitance



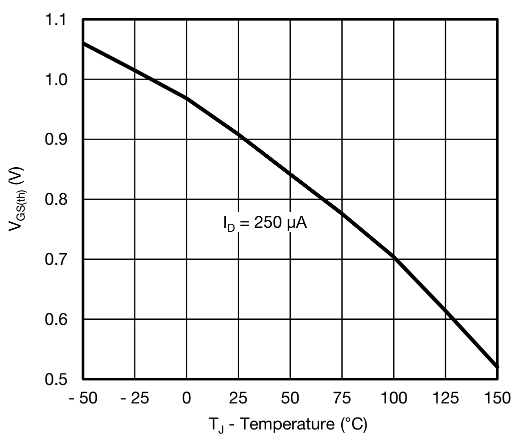
Source-Drain Diode Forward Voltage



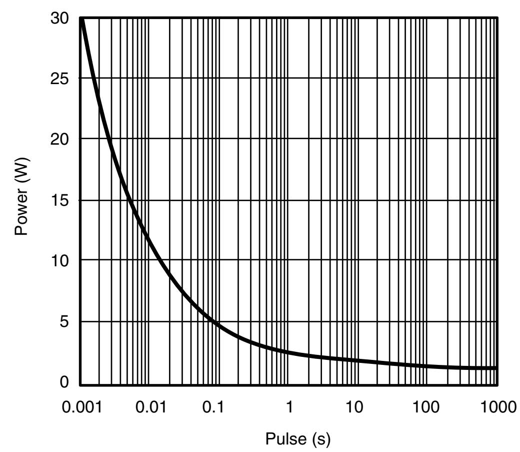
Gate Charge



On-Resistance vs. Gate-to-Source Voltage

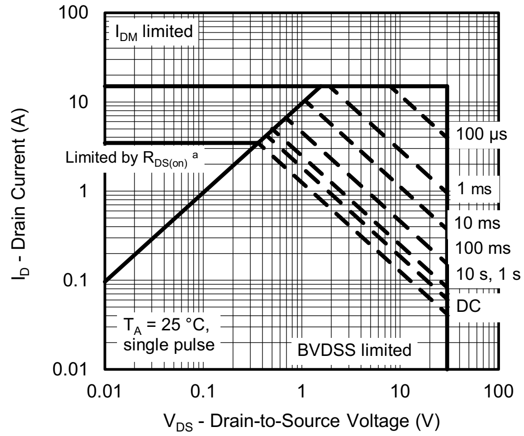


Threshold Voltage

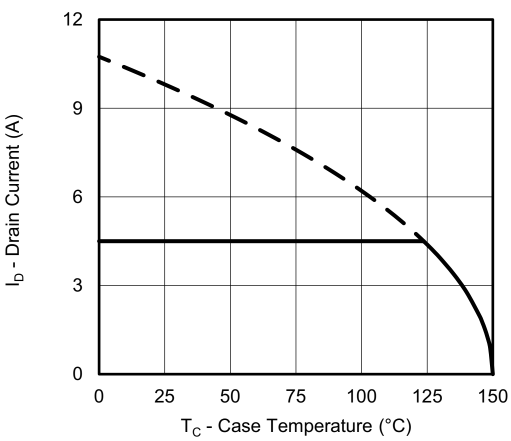


Single Pulse Power, Junction-to-Ambient

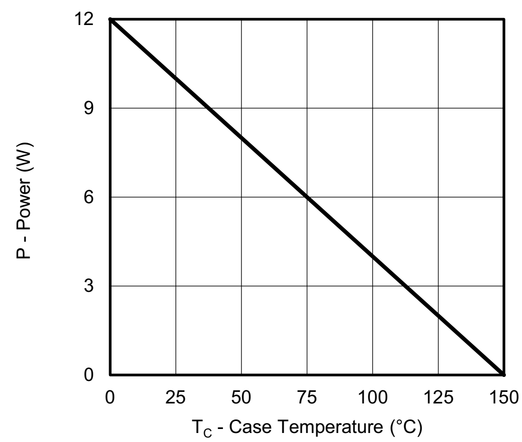
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Case



Current Derating [a]

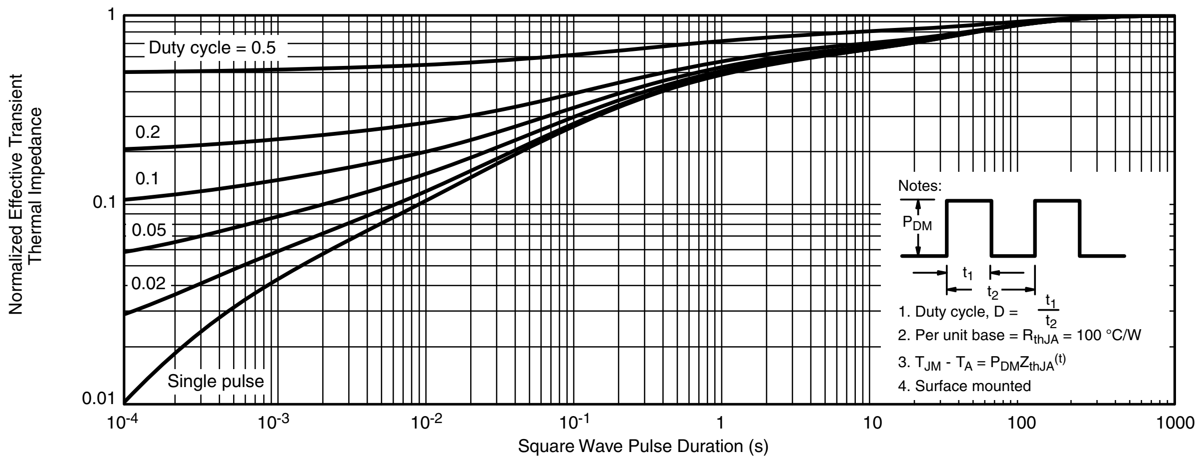


Power Derating

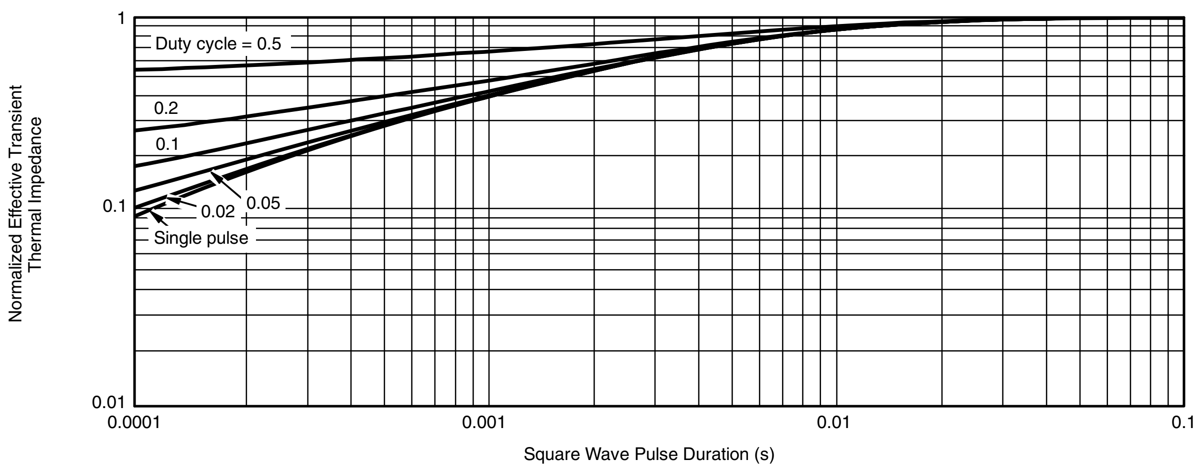
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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