ICP-20100

High Accuracy, Low Power, Barometric Pressure and Temperature Sensor IC

GENERAL INFORMATION

The ICP-20100 pressure sensor provides a high-accuracy, low power, barometric pressure and temperature sensor solution, that integrates a capacitive pressure sensor for monitoring pressure changes in the range of 30 to 110 kPa.

The ICP-20100 integrates a DSP module for on-chip calibration with an Analog-to-Digital converter (ADC), digital filtering, a FIFO and has I²C, I3C℠, and SPI interfaces available. The solution can be configured to achieve ultra-low noise or ultra-low power performance and is flexible to perform anywhere in-between. Additionally, the filters can be enabled to allow even lower noise performance or activate features such as filtering of pressure glitches (e.g. opening/closing a window).

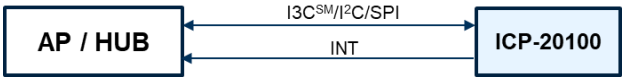
The ICP-20100 is available in a closed package with a vent hole.

DEVICE INFORMATION

PART NUMBER	PACKAGE	LID OPENING	MSL**
ICP-20100*	2x2x0.8mm LGA-10L	1-Hole	1

* Denotes RoHS and Green-Compliant Package
** Moisture Sensitivity Level of the package

BLOCK DIAGRAM



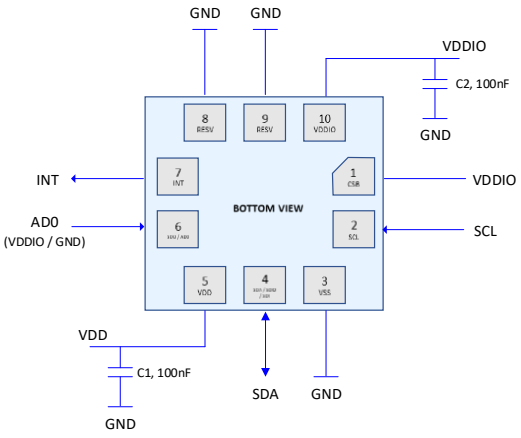
APPLICATIONS

- Smartphones and Tablets
- Wearable Sensors
- Home and Building Automation
- Weather Stations

FEATURES

- Digital-output pressure and temperature sensors, with programmable output: all-pressure, all-temperature or pressure & temperature
- Programmable noise performance down to 0.5 Parms through programmable Oversampling Ratio (OSR)
- Digital filtering for pressure signals
  - Finite Impulse Response (FIR) filter for improved noise performance
  - Infinite Impulse Response (IIR) filter for e.g. filtering of pressure glitches
- Package dimensions 2x2x0.8 mm (10-pin LGA)
- 96-byte FIFO buffer enables the application processor to read up to 16 pressure-temperature pairs in a burst
- User-programmable Interrupt
- Host interface: 12 MHz SPI/1 MHz I²C/12.5 MHz I3C℠
- Temperature operating range: -40°C to 85°C
- Main Supply voltage: 1.8V ±10% or 3.3V ±10%
- I/O supply voltage externally applied (1.2V ±10%, 1.8V ±10% or 3.3V* ±10%) *available only when main supply voltage equals 3.3V ±10%
- RoHS and Green compliant

TYPICAL OPERATING CIRCUIT



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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a preliminary product specification, providing a description, specifications, and design related information for the ICP-20100 Pressure Sensor.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon.

1.2 PRODUCT OVERVIEW

The ICP-20100 is a high accuracy, low power, barometric pressure and temperature sensor solution that integrates a capacitive pressure sensor for monitoring pressure changes in the range of 30 to 110kPa.

The ICP-20100 pressure and temperature sensor device combines TDK InvenSense 2nd generation (20k-series) capacitive pressure sensors.

Other industry-leading features include up to 20-bits output data, programmable digital filters, an embedded temperature sensor, calibration, FIFO, and programmable interrupts. The device features I^2C, $I3C^{SM}$, and SPI serial interfaces, a VDD operating range of 1.8V ±10% or 3.3V ±10%, and an externally applied VDDIO operating range of 1.2V ±10%, 1.8V ±10% or 3.3V* ±10% (*available only when VDD voltage equals 3.3V ±10%).

The host interface can be configured to support SPI slave or I^2C/ $I3C^{SM}$ slave modes. The SPI interface supports speeds up to 12 MHz, the I^2C interface supports speeds up to 1 MHz, and the $I3C^{SM}$ interface supports speeds up to 12.5 MHz.

The MEMS sensor consists of a capacitive pressure sensor whose capacitance changes according to the pressure applied. An integrated temperature sensor on the same MEMS sensor allows for accurate temperature measurements.

2 PRESSURE AND TEMPERATURE SENSOR SPECIFICATIONS

2.1 OPERATION RANGES

PARAMETER	VALUE	UNITS
Functional Pressure Range	30 to 110	kPa
Operating Temperature Range	-40 to 85	°C

Table 1. Operation Ranges

2.2 OPERATION MODES

The sensor can be operated in the following measurement modes to satisfy different requirements for power consumption vs. noise, accuracy, and measurement frequency.

Operation mode can be selected using register field MEAS_CONFIG in register MODE_SELECT. Modes 0 to 3 are pre-defined while Mode 4 is user configurable. Please refer to "AN-000238: ICP-20100 and ICP-20132 User Configurable Operation Mode and IIR Filter" for details on how to configure MODE4.

PARAMETER	BW (HZ)	ODR (HZ)	PRESSURE NOISE (PARMS)	CURRENT CONSUMPTION (µA)	IIR FILTER ENABLED	FIR FILTER ENABLED
			TYP	TYP		
MODE0	6.25	25	0.5	211	No	Yes
MODE1	30	120	1	222	No	Yes
MODE2	10	40	2.5	49	No	Yes
MODE3	0.5	2	0.5	23	No	Yes
MODE4*	12.5	25	0.3	250	No	No

Table 2. Operation Modes

Note: MODE4 is user configurable as explained in the application note "AN-000238: ICP-20100 and ICP-20132 User Configurable Operation Mode and IIR Filter". MODE4 functionality shown is default device calibration, user can modify MODE4 configuration as explained in AN-000238.

2.3 PRESSURE SENSOR SPECIFICATIONS

Pressure sensor specifications are given in Table 3. Default conditions of 25 °C, VDD = 1.8V and VDDIO = 1.8V apply, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Functional pressure range		30	70	110	kPa	
Absolute Accuracy	Valid from -20°C to 65°C		±20		Pa	1
Relative Accuracy	Any step ≤ 1 kPa at 25°C		±1		Pa	1
Temperature Coefficient of Offset (TCO)	P = 100 kPa 25°C … 45°C		±0.4		Pa/°C	1
Long-Term Drift (during 1 year)			±10		Pa	2
Solder Drift	Board-level specification		±0.4		hPa	3, 4
Resolution			20		bits	

Table 3. Pressure Sensor Specifications

Notes:

1. Parameter specifications shown are component-level. They may be different at the board-level and may depend on PCB characteristics including but not limited to PCB material, number of layers, PCB thickness. They may also depend on usage conditions.
2. Determined based on HTOL data.
3. Derived from validation or characterization of parts, not tested in production.
4. Board-level spec values depend on specific board design. For design information of boards used for device characterization, that forms the basis of the spec values reported here, please contact your local TDK InvenSense FAE.

2.4 TEMPERATURE SENSOR SPECIFICATIONS

Specifications of the temperature sensor are shown in Table 4.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Temperature accuracy			±0.5		°C	
Output Data rate			ODR		Hz	1

Table 4. Temperature Sensor Specifications

Notes:

1. Temperature ODR = Pressure ODR for selected mode

3 ELECTRICAL SPECIFICATIONS

3.1 ELECTRICAL CHARACTERISTICS

Default conditions of 25 °C, VDD = 1.8V and VDDIO = 1.8V apply to values in Table 5 and Table 6, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
Main Supply Voltage	V_{DD}		1.62	1.8	1.98	V	
			2.97	3.3	3.63	V	
I/O Supply Voltage	V_{DDIO}		1.08	1.2	1.32	V	Externally supplied
			1.62	1.8	1.98	V	
			2.97	3.3	3.63	V	
Supply current	I_{DD}	standby	-	2.65	-	µA	

Table 5. Electrical Supplies

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		10	ms	2
Power Supply Noise				50	mV peak-peak	2
TEMPERATURE SENSOR						
Operating Range	Ambient	-20		65	°C	2
ADC Resolution		15			bits	1
ODR				800	Hz	1
I2C ADDRESS						
I2C ADDRESS	AD0 = 0 AD0 = 1		0x63 0x64			
DIGITAL INPUTS						
VIH, High Level Input Voltage		0.7*VDDIO			V	2
VIL, Low Level Input Voltage				0.3*VDDIO	V	
DIGITAL OUTPUTS						
VOH, High Level Output Voltage		0.75*VDDIO			V	2
VOL, Low-Level Output Voltage				0.25*VDDIO	V	
Drive strength for VDDIO = 1.2V		0.5 2 3 4	2 4 6 8	4 6 9 12	mA	
Drive strength for VDDIO = 1.8V/3.3V		1 2 4 8	2 4 8 12	4 8 12 16	mA	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Low clock frequency 8kHz	-2		+2	%	2
	Main clock frequency 1.9MHz	-3.125		+3.125	%	2

Table 6. Electrical Specifications

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not guaranteed in production

3.2 ABSOLUTE MAXIMUM RATINGS

Stress levels beyond those listed in Table 7 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions cannot be guaranteed. Exposure to the absolute maximum rating conditions for extended periods may affect the reliability of the device.

PARAMETER	RATING
Supply voltage, VDD	-0.3V to +4.0V
Supply Voltage, SCL & SDA	-0.3V to VDDIO+0.3V
Operating temperature range	-40°C to +85°C
Storage temperature range	-40°C to +85°C
ESD HBM	1.5 kV
ESD CDM	500V
Radiated EMI immunity	4kV/m
Conducted EMI immunity	2Vrms

Table 7. Absolute Maximum Ratings

3.3 SENSOR SYSTEM TIMING

Default conditions of 25 °C, VDD = 1.8V and VDDIO = 1.8V apply to TYP values listed in Table 8, unless otherwise stated. MAX values apply over the specified operating range of VDD and over the operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
Power-up time	t_{PU}		-	2	-	ms	Time between V_{DD} reaching V_{PU} and sensor entering idle state; V_{PU} is the power-up voltage, the minimum V_{DD} at which start-up time is guaranteed, it has a value of 1.56V.

Table 8. System Timing Specifications

3.4 I²C TIMING CHARACTERIZATION

Default conditions of 25 °C, VDD = 1.8V and VDDIO = 1.8V apply to values in Table 9, unless otherwise stated.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		260			ns	1
t_{LOW}, SCL Low Period		500			ns	1
t_{HIGH}, SCL High Period		260			ns	1
$t_{SU.STA}$, Repeated START Condition Setup Time		260			ns	1
$t_{HD.DAT}$, SDA Data Hold Time		5			ns	1
$t_{SU.DAT}$, SDA Data Setup Time		55			ns	1
t_r, SDA and SCL Rise Time [2]	C_b bus cap. From 10 to 400 pF	20*(VDD/5.5V)		120	ns	1
t_f, SDA and SCL Fall Time [2]	C_b bus cap. From 10 to 400 pF	20*(VDD/5.5V)		120	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		260			ns	1
t_{BUF}, Bus Free Time Between STOP and START Condition		500			ns	1
C_b, Capacitive Load for each Bus Line				550	pF	1
$t_{VD.DAT}$, Data Valid Time				450	ns	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				450	ns	1

Table 9. I²C Parameters Specification

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

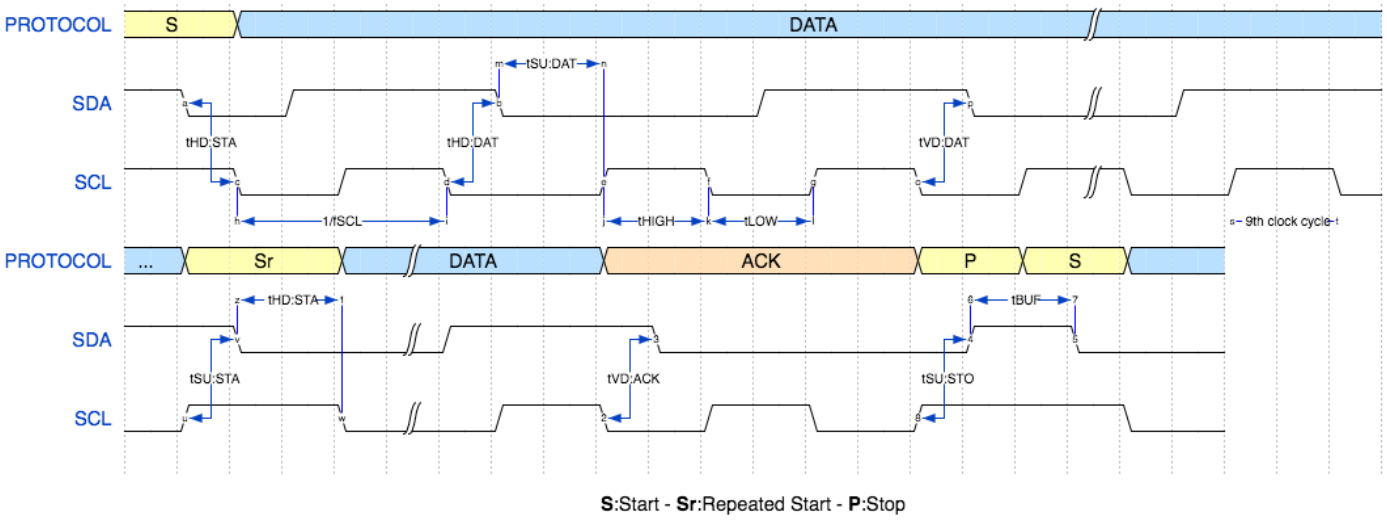


Figure 1. I²C Bus Timing Diagram

3.5 I3C^{SM} TIMING CHARACTERIZATION

Default conditions of 25 °C, VDD = 1.8V and VDDIO = 1.8V apply to values in Table 10, unless otherwise stated.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I3C^{SM} TIMING	**I3C^{SM} SDR mode**					
f_{SCL}, SCL Clock Frequency			12.5	12.9	MHz	
t_{LOW}, SCL Low Period	From 30% to 30%	24			ns	
t_{DIG_L}, SCL Low Period (to high transition)	From 30% to 70%	32			ns	
t_{HIGH_MIXED}, SCL High Period for Mixed Bus	From 70% to 70%	24			ns	
$t_{DIG\_H\_MIXED}$, SCL High Period for Mixed Bus	From 70% to 30%	32		45	ns	
t_{HIGH}, SCL High Period	From 70% to 70%	24			ns	
t_{DIG_H}, SCL High Period	From 70% to 30%	32			ns	
t_{SCO}, Clock in to Data Out for Slave				12	ns	
t_{CR}, SCL Rise Time	Capped at 60			12	ns	
t_{CF}, SCL Fall Time	Capped at 60			12	ns	
t_{HD_PP}, SDA Signal Data Hold in Push-Pull mode	Slave	0			ns	
t_{SU_PP}, SDA Signal Data Setup in Push-Pull mode		3			ns	
C_b, Capavitive Load per Bus Line	SDA/SCL			50	pF	

Table 10. I3C^{SM} Parameters Specification

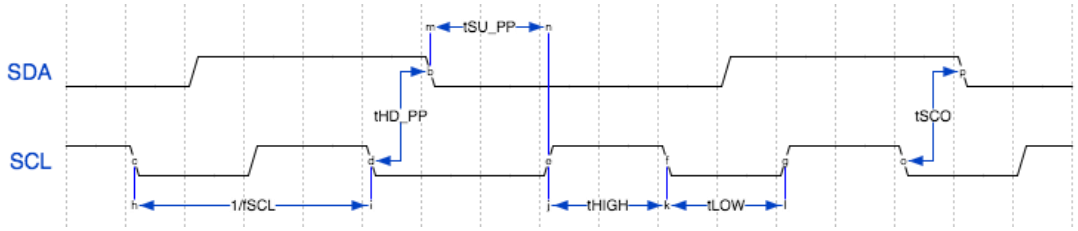


Figure 2. I3C^{SM} Bus Timing Diagrams

3.6 SPI 4-WIRE MODE TIMING CHARACTERIZATION

Default conditions of 25°C and 1.8V supply voltage apply to values in Table 11, unless otherwise stated.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCL Clock Frequency				12	MHz	1
t_{LOW}, SCL Low Period		40			ns	1
t_{HIGH}, SCL High Period		40			ns	1
$t_{SU.CS}$, CS Setup Time		20			ns	1
$t_{HD.CS}$, CS Hold Time		20			ns	1
$t_{SU.SDI}$, SDI Setup Time		5			ns	1
$t_{HD.SDI}$, SDI Hold Time		20			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 50 pF			32	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 50 pF	5			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				25	ns	1
t_{Fall}, SCLK Fall Time				5	ns	2
t_{Rise}, SCLK Rise Time				5	ns	2

Table 11. SPI 4-Wire Mode Parameters Specification

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

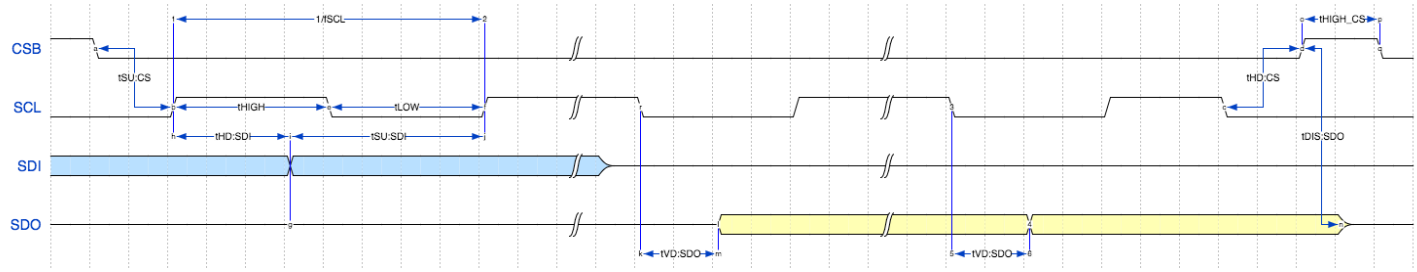


Figure 3. SPI 4-Wire Mode Bus Timing Diagram

3.7 SPI 3-WIRE MODE TIMING CHARACTERIZATION

Default conditions of 25°C and 1.8V supply voltage apply to values in Table 12, unless otherwise stated.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCL Clock Frequency				12	MHz	1
t_{LOW}, SCL Low Period		40			ns	1
t_{HIGH}, SCL High Period		40			ns	1
$t_{SU.CS}$, CS Setup Time		20			ns	1
$t_{HD.CS}$, CS Hold Time		20			ns	1
$t_{SU.SDI}$, SDI Setup Time		5			ns	1, 3
$t_{HD.SDI}$, SDI Hold Time		20			ns	1, 3
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 50 pF			32	ns	1, 3
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 50 pF	5			ns	1, 3
$t_{DIS.SDO}$, SDO Output Disable Time				25	ns	1, 3
t_{Fall}, SCLK Fall Time				5	ns	2
t_{Rise}, SCLK Rise Time				5	ns	2

Table 12. SPI 3-Wire Mode Parameters Specification

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values
3. Separate SDI and SDO times are provided to account for input and output transactions on the SDIO interface for 3-wire SPI mode

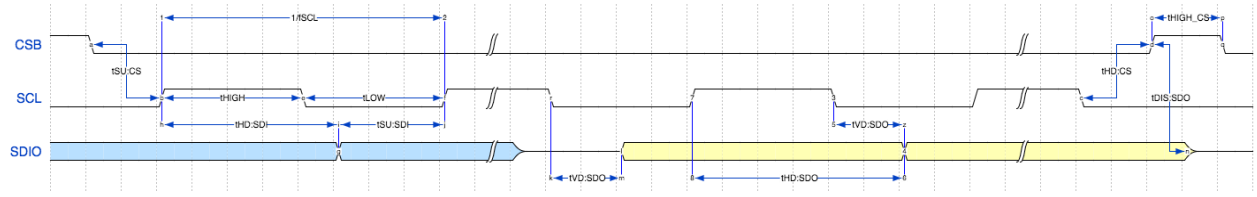


Figure 4. SPI 3-Wire Mode Bus Timing Diagram

4 INTERFACE SPECIFICATIONS

The ICP-20100 supports I3C^{SM}, I^{2}C, SPI host-interface options. The ICP-20100 always operates as a slave when connected to the host. Selection between SPI and I3C^{SM}/I^{2}C is done with the CSB pin. If the pin is pulled low, the SPI interface is active and I3C^{SM}/I^{2}C are disabled. If CSB is high, I3C^{SM}/I^{2}C is selected.

4.1 I3C^{SM} / I^{2}C INTERFACE

The I3C^{SM}/I^{2}C interface can operate in I^{2}C legacy mode or I3C^{SM} SDR mode (SCL clock frequency up to 12.5 MHz).

After reset, the device requires a minimum of 10 clock cycles to initialize the I3C^{SM}/I^{2}C interface. Before doing this, no communication is possible through I3C^{SM}/I^{2}C. This initialization can be done through a dummy write transaction to address 0xEE.

4.1.1 I^{2}C Interface

The ICP-20100 I^{2}C slave interface can operate in following modes:

- Standard mode (SCL clock frequency up to 100 kHz)
- Fast mode (SCL clock frequency up to 400 kHz)
- Fast mode plus (SCL clock frequency up to 1 MHz)

4.1.2 I3C^{SM} Interface

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, dynamic addressing.

The I3C^{SM} interface complies with “MIPI I3C Specification -- public edition”, version 1.0, 23 December 2016.

By default, the I^{2}C protocol is used. Only when the device detects that it is connected to an I3C^{SM} bus, will it permanently switch to the I3C^{SM} protocol and the glitch filter will be disabled.

The I3C^{SM} interface supports:

- SDR data rate up to 12.5 MHz
- Dynamic Addressing
- Error detection (Parity)
- Common Command Codes described in Table 13.

4.1.3 I²C Data Protocol

A transfer is always started by addressing the device with an I²C write header followed by the targeted 8-bit register address.

For write accesses, the master continues sending the 8-bit data word.

For read accesses, the master must change the transfer direction from write to read by sending an I²C read header with the correct address. The device then transmits the data word (if available). An address increment feature enables reading multiple data bytes in a row.

All commands and memory locations are mapped to an 8-bit register space which can be accessed via the I²C interface. Data is always transferred as 8-bit words. Figure 5 illustrates the different transfer types.

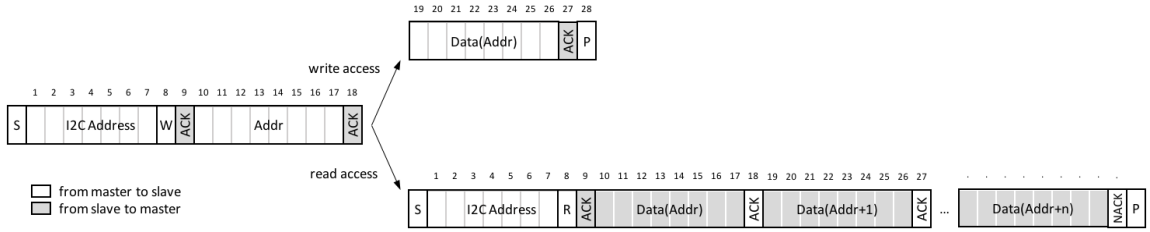


Figure 5. I²C Data Protocol

The I²C interface has access to all registers needed for functional operation.

Every byte transmitted from the I²C master to the slave device must be acknowledged.

In read direction, the master indicates with the acknowledge if an address increment read needs to be initiated. An ACK from the master indicates a request for an address increment read. A NACK from the master indicates the end of the read transfer and needs to be followed by a STOP condition.

Every last I2C bus transaction to ICP-20100 should end with read to address 0x00. At least once in every 255 I2C read or burst read transactions (Burst read accesses treated as one read transaction independent of burst size) on the bus to other I2C devices, the host should perform a read to ICP-20100 address 0x00.

One possible implementation of the requirement above would be to add a dummy read from ICP-20100 address 0x00 after any I2C transactions.

Another possible implementation is to perform a dummy read from ICP-20100 address 0x00 after each last I2C bus transaction to ICP-20100 and add a dummy read from ICP-20100 address 0x00 at a constant rate of 110Hz.

4.1.4 I3C^{SM} Data Protocol

The device is switched to I3C^{SM} mode by sending the reserved byte 7'h7E.

While in I3C^{SM} mode, the device is addressed with an I3C^{SM} write header containing the dynamic device address, followed by the targeted 8-bit register address.

For write accesses, the master continues sending the 8-bit data word.

For read accesses, the master must change the transfer direction from write to read by sending an I3C^{SM} read header containing the dynamic device address. The device then transmits the data word. An address increment feature allows to read out multiple data bytes in a row.

All commands and memory locations are mapped to an 8-bit register space which can be accessed via the I3C^{SM} interface. Data is always transferred as 8-bit words. Figure 6 illustrates the different transfer types.

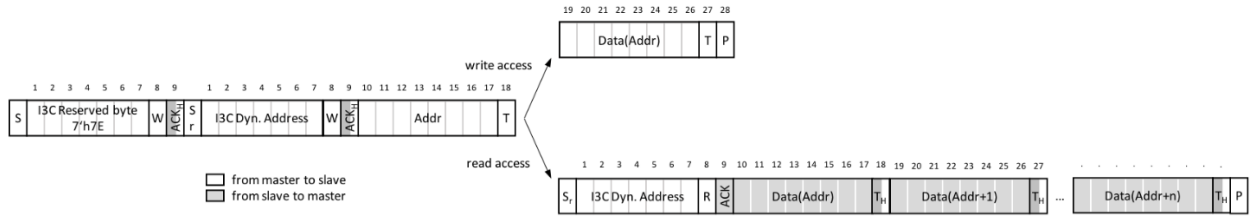


Figure 6. I3C^{SM} Data Protocol

The I3C^{SM} interface has access to all registers needed for functional operation.

Every last I3C bus transaction to ICP-20100 should end with read to address 0x00. At least once in every 255 I3C read or burst read transactions (Burst read accesses treated as one read transaction independent of burst size) on the bus to other I3C devices, the host should perform a read to ICP-20100 address 0x00.

One possible implementation of the requirement above would be to add a dummy read from ICP-20100 address 0x00 after any I3C transactions.

Another possible implementation is to perform a dummy read from ICP-20100 address 0x00 after each last I3C bus transaction to ICP-20100 and add a dummy read from ICP-20100 address 0x00 at a constant rate of 110Hz.

4.1.5 Supported I3C^{SM} Common Command Codes (CCC)

I3C^{SM} features CCCs that allow the master to manage the bus and its connected slaves, either directly or through a broadcast.

The I3C^{SM} master should not use any unsupported CCCs.

CODE	CCC TYPE	MNEMONIC	DESCRIPTION
0x06	broadcast	RSTDAA	Reset Dynamic Address Assignment
0x07	broadcast	ENTDAA	Enter Dynamic Address Assignment
0x86	direct	RSTDAA	Reset Dynamic Address Assignment (p2p)
0x87	direct	SETDASA	Set Dynamic Address from Static Address
0x88	direct	SETNEWDA	Set New Dynamic Address
0x8D	direct	GETPID	Get Provisional ID
0x8E	direct	GETBCR	Get Bus Characteristics Register
0x8F	direct	GETDCR	Get Device Characteristics Register
0x90	direct	GETSTATUS	Get Device Status

Table 13. Supported I3C^{SM} CCCs

4.1.6 I3C^{SM} Provisional Identifier

The Provision Identifier (PID) is hardwired as:

BIT	NAME	FIXED VALUE	NOTE
47:33	MIPI Manufacturer ID	15'h0235	TDK Manufacturer ID
32	PID Type Selector	0	0 = PID fixed value
31:16	Part ID	0	
15:12	Instance ID	0	
11:0	Vendor defined	0	

Table 14. I3C^{SM} Provisional Identifier

4.1.7 I3C^{SM} Bus Characteristics Register

The Bus Characteristics Register (BCR) is hardwired as:

BIT	NAME	FIXED VALUE	NOTE
7	Device Role [1]	0	fixed (slave role)
6	Device Role [0]	0	fixed (slave role)
5	Data Rate support	0	fixed (SDR only)
4	Bridge Identifier	0	fixed (no bridge)
3	Offline Capable	0	fixed (not offline capable)
2	IBI Payload	0	fixed (IBI not supported)
1	IBI Request Capable	0	fixed (IBI not supported)
0	Max Data Speed Limit	0	fixed (no speed limit, GETMXDS not supported)

Table 15. I3C^{SM} Bus Characteristics Register

4.1.8 I3C^{SM} Device Characteristics Register

The Device Characteristics Register (DCR) byte [7:0] is hardwired to the fixed value 0x62, which corresponds to the "Environment Pressure Sensor" as defined by MIPI. (see https://www.mipi.org/MIPI_I3C_device_characteristics_register)

4.1.9 Fixed I^{2}C slave address and address increment

The value assigned on AD0 allows to adapt the I^{2}C address as follows:

- AD0 = 0 : I^{2}C address = 0x63
- AD0 = 1 : I^{2}C address = 0x64

4.1.10 I3C^{SM} Slave Address

I3C^{SM} supports dynamic addressing feature which allows master and slaves to do dynamic address arbitration on the I3C^{SM} bus.

The concatenation of {PID[15:0],BCR[7:0],DCR[7:0]} is used to determine the priority for dynamic addressing by the Master.

Since there is already a static address present for I^{2}C, this can be used via the SETDASA command if known by the Master up front. When applicable, the address increment is applied as well.

4.2 SPI INTERFACE

The ICP-20100 SPI slave interface can operate in the following modes:

- 3-wire mode using pins CSB, SDIO and SCL
- 4-wire mode using pins CSB, SDI, SDO and SCL

The SPI interface has access to all registers needed for functional operation.

4.2.1 SPI Protocol

The SPI frame format is as follows:

1. SPI master pulls CSB low
2. SPI master sends 1 command byte
3. SPI master sends 1 address byte
4. For write frames, SPI master sends a master data byte
5. For read frames, IFPS replies with a number of slave data bytes
6. SPI master releases CSB

This is pictured in the Figure 7 and Figure 8 respectively for 4-wire SPI and 3-wire SPI.

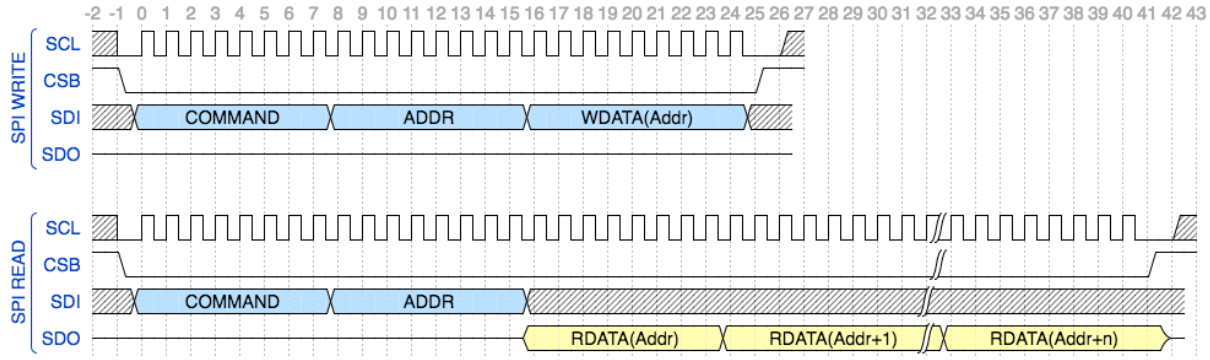


Figure 7. 4-Wire SPI Transaction Overview

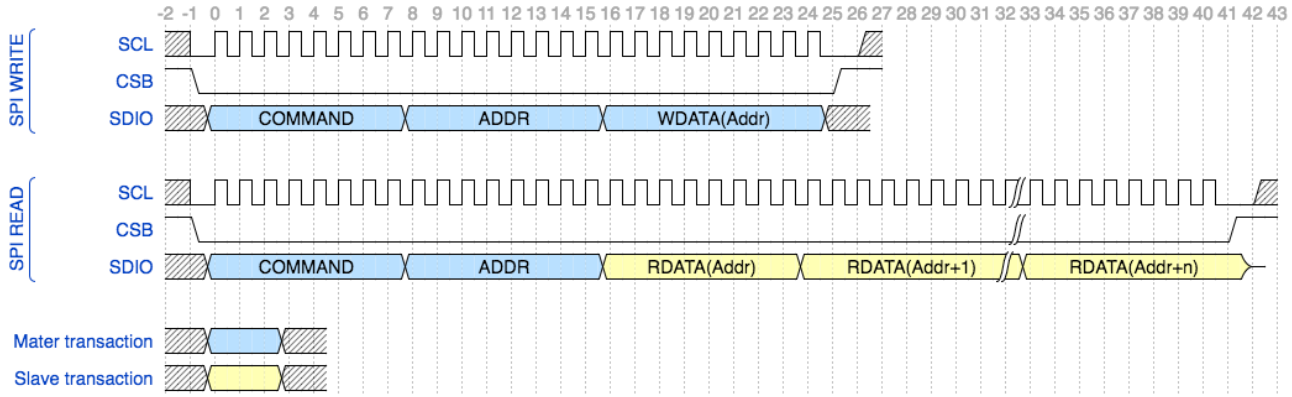


Figure 8. 3-Wire SPI Transaction Overview

A transmitter conceptually produces data bits at the falling edge of the SPI clock SCL, and a receiver samples the data bits at the rising edge of the SPI clock.

Bytes are transmitted in the order MSB to LSB.

The slave keeps SDO in high-Z unless a reply is expected from the command (read request).

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
spi_speed	Data rate of the SPI protocol	DC		12	Mbps	

Table 16. SPI Data Rate Specifications

4.2.2 SPI Modes

The ICP-20100 supports SPI MODE0 and MODE3.

When the SPI interface is idle, SCL is low. Data is propagated on the clock's falling edge and captured on the clock's rising edge.

4.2.3 SPI Frame Abort

The SPI master can abort an SPI frame by de-asserting CSB.

4.2.4 Supported Commands

Table 17 shows the supported commands via the SPI interface.

COMMAND CODE	COMMAND	DESCRIPTION
0x3C	CMD_READ_REG	Read from register
0x33	CMD_WRITE_REG	Write to register

Table 17. SPI Supported Commands

4.3 DRIVE STRENGTH CONFIGURATION

The device starts up with drive strength 2 mA in 1.8V IO supply mode. If the application requires high speed communication (>1 MHz) or uses VDDIO=1.2V, the drive strength settings need to be adapted. This is done by reconfiguring register IO_DRIVE_STRENGTH (section 13.5 in this datasheet).

This section provides MATLAB sample code on how to do this. The following terminology is used in this code for register map references:

regMap.Register_Name.Register_Field_Name.Write(Value)

where

- "Register_Name" is the register name;
- "Register_Field_Name" is the name of the register field in the register;
- "Write" is a write operation for the specified register field;
- "Value" is the value being written to the specified register field

Please refer to sections 12 and 13 for information about the registers/register fields shown in the sample code.

```
function PowerMode(self)
    %% PowerMode: function to move into power mode
    global regMap

    %% Move to power mode if not already inside
    if (regMap.MODE_SELECT.POWER_MODE.read==0)
        fprintf('Moving into power mode...\n')
        regMap.MODE_SELECT.POWER_MODE.write(1);
        pause(0.001);
    end
end

function Configure_drive_strength(self)
    %% Configure_drive_strength: sample code on how to configure the drive strength
    %  after a reset of the device

    global regMap

    self.PowerMode;

    %% Configure the drive strength mirror registers
    %  This example configures a drive strength of 12mA for 1.8V IO supply
    regMap.IO_DRIVE_STRENGTH.IO_DS.write('0x3');
end
```

5 APPLICATIONS INFORMATION

5.1 ICP-20100 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	DESCRIPTION
1	CSB	SPI Chip Select
2	SCL	I3C^{SM} / I^{2}C / SPI Serial Clock
3	VSS	Power Supply Ground
4	SDA / SDIO / SDI	SDA: I3C^{SM} / I^{2}C serial data; SDIO: SPI serial data I/O (3-wire mode); SDI: SPI serial data input (4-wire mode)
5	VDD	Power Supply Voltage
6	SDO / AD0	SDO: SPI serial data output (4-wire mode); AD0: I3C^{SM} / I^{2}C slave address LSB
7	INT	Interrupt Output
8	RESV	Connect to Ground
9	RESV	Connect to Ground
10	VDDIO	IO Power Supply

Table 18. ICP-20100 Signal Descriptions

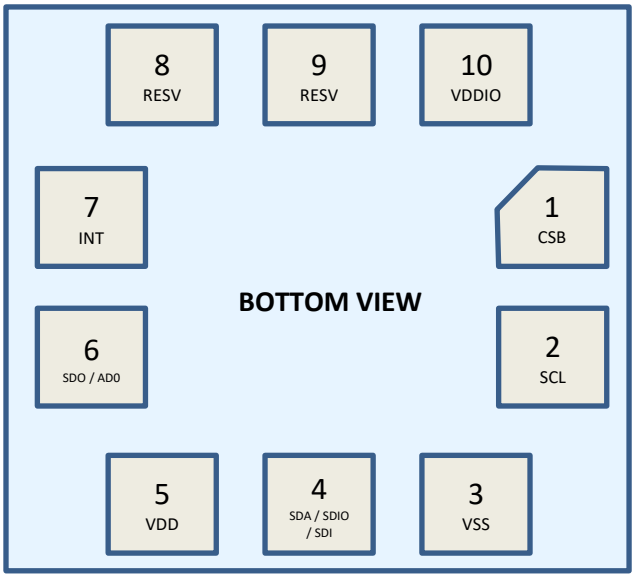


Figure 9. Pin Out Diagram for ICP-20100, 2mm x 2mm x 0.8mm LGA

5.2 TYPICAL OPERATING CIRCUITS

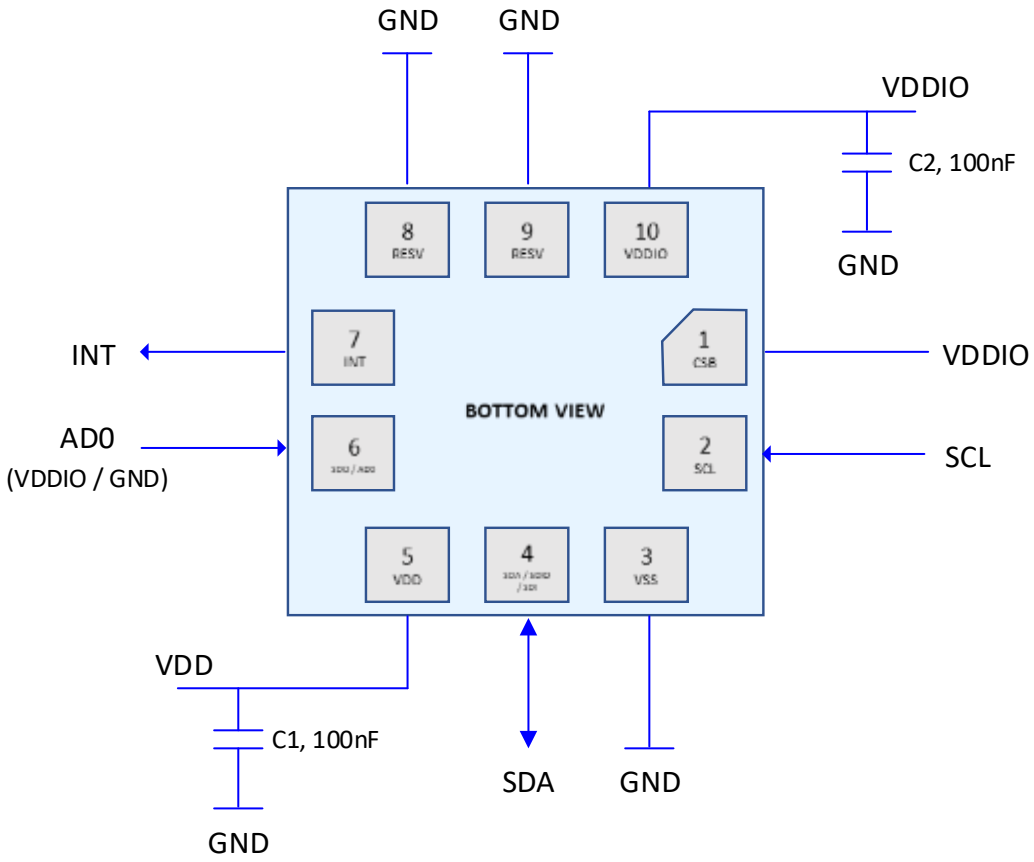


Figure 10. ICP-20100 Application Schematic (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 5kΩ) are required.

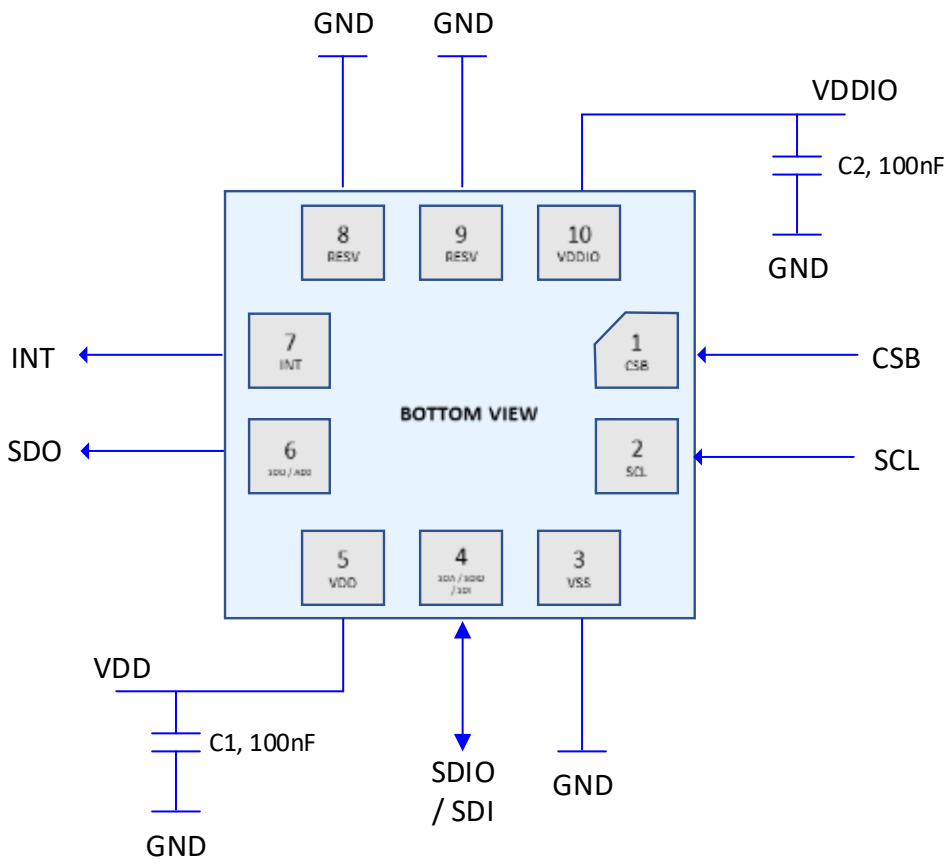


Figure 11. ICP-20100 Application Schematic (SPI Interface to Host)

5.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
VDD Bypass Capacitor	C1	X7R, 100nF ±10%	1
VDDIO Bypass Capacitor	C2	X7R, 100nF ±10%	1

5.4 ASIC IDENTIFICATION

For identifying this device, please use following procedure:

1) Power-on the ASIC
2) Initialize the I^2C interface by toggling the clock line a few times. The easiest way to do that is by inserting a dummy I^2C write transaction. You can, for example, execute the first transaction (write to lock register) twice.
3) Check that the value from register regMap.device_id equals 0x63
4) Check the value from register regMap.version:
   - 0x00 indicates a device version A
   - 0xB2 indicates a device version B

6 PRESSURE AND TEMPERATURE MEASUREMENT

The ICP-20100 uses a 2nd order ∑Δ ADC with time-multiplexed pressure and temperature measurements. Integration time for measurement, or over-sampling ratio (OSR) can be configured independently for pressure and temperature.

6.1 PRESSURE AND TEMPERATURE MEASUREMENT ACCURACY

Increasing the pressure OSR improves the noise on the pressure measurement but also results in more current consumption due to a delayed return to STANDBY mode.

Increasing the temperature OSR improves the noise on the temperature measurement and on the pressure measurement due to the non-linear pressure compensation as a function of the temperature but also results in more current consumption due to a delayed return to STANDBY.

The pressure and temperature OSR values are limited by the Output Data Rate (ODR) selection. For details of the relationship between these parameters, refer to section 6.2.

For given OSR and ODR settings, the noise can further be optimized by using an IIR filter. Refer to section 0 for details of the IIR filter.

6.2 PRESSURE AND TEMPERATURE MEASUREMENT SEQUENCING

Pressure and temperature measurements are time-multiplexed, with pressure measurement performed first and followed by temperature measurement.

A measurement can be started either automatically (duty cycled operation) or manually (triggered operation).

6.2.1 Duty Cycled Operation

In duty cycled operation Pressure/Temperature measurements are automatically started.

The time between 2 measurements is defined by the ODR (Output Data Rate) setting and is timed based on the low power clock.

In Figure 12 and Figure 13, T_{OSR_P} is the pressure sensor OSR and T_{OSR_T} is the temperature sensor OSR.

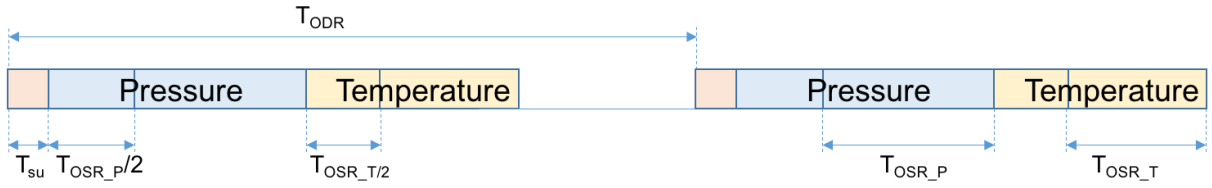


Figure 12. Duty Cycled Measurement

If the configured ODR period is smaller than the conversion time for pressure and temperature, the actual ODR is adapted to match the conversion time.

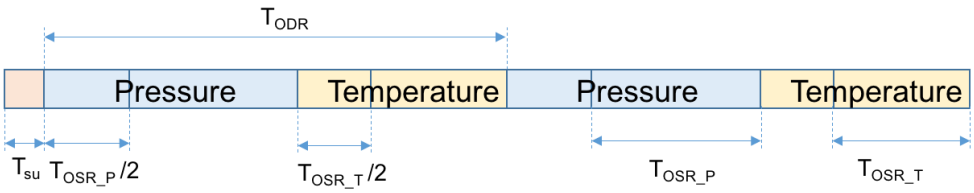


Figure 13. Duty Cycled Measurement Without Wait

By disabling the pressure or temperature measurement through setting its respective OSR configuration register (refer to the application note "*AN-000238: ICP-20100 and ICP-20132 User Configurable Operation Mode and IIR Filter*") to value 0, a temperature-only or pressure-only measurement can be configured.

If a pressure-only setting is combined with an ODR period setting that is smaller than the conversion time, a maximal conversion rate can be established in which no settling is needed for each individual sample and a higher ODR can be reached. The same principle applies for temperature-only setting.

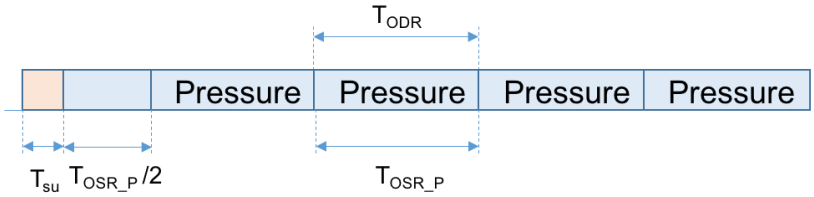


Figure 14. Pressure-Only Mode

The maximum ODR can be calculated based on the pressure and temperature OSR by the following formula:

$ODR_{MAX}(Hz) = 10^6/(168+2.1*1.5*(OSR_{PRESS}+OSR_{TEMP}))$

with OSR_{PRESS}, OSR_{TEMP} the pressure and temperature Over Sampling Ratio.

where $OSR_{PRESS} = \left(OSR\_PRESS_{register} + 1\right) * 2^5$ and $OSR_{TEMP} = \left(OSR\_TEMP_{register} + 1\right) * 2^5$

6.2.2 Triggered operation

Triggered operation (also called forced measurement mode) performs a single Pressure, Temperature, or Pressure/Temperature pair measurement. After the measurement, the device returns to standby mode.

Triggered operation is only supported for MODE4.

6.3 FIR FILTER

The ICP-20100 includes a FIR filter in the signal path.
The FIR filter is a low pass filter, filtering off the remaining noise above ODR/4.

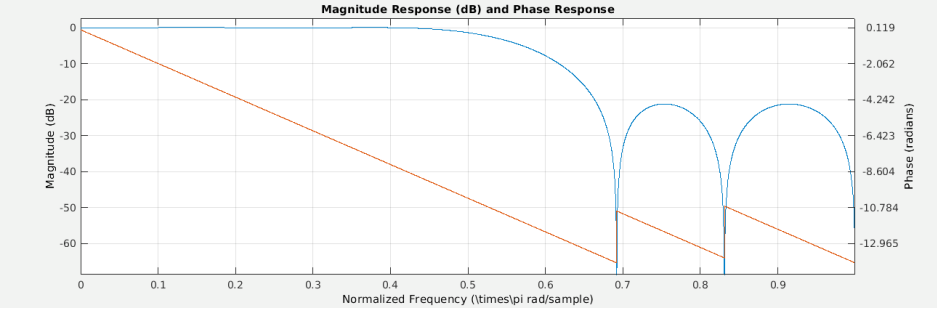


Figure 15. FIR Filter

In case the FIR filter is enabled first 14 samples should be ignored after mode change. This can be done by configuring ICP-20100 in required mode and poll for FIFO count to be 14 and flushing FIFO or by using FIFO watermark interrupt. The following sequence will explain ignoring first 14 samples using FIFO watermark interrupt:

1) Power-on the ASIC
2) Only for I^2C: initialize the I^2C interface by toggling the clock line a few times. The easiest way to do that is by inserting a dummy I^2C write transaction.
3) Configure the FIFO watermark high to 14 samples
   - regMap.FIFO_CONFIG = 0xE0
4) Unmask the watermark high interrupt
   - regMap.INTERRUPT_MASK = 0xFB
5) Start a measurement
   - regMap.MODE_SELECT.MEAS_CONFIG = M (M is the selected mode)
   - regMap.MODE_SELECT.MEAS_MODE = 1
   - regMap.MODE_SELECT.POWER_MODE = 0
6) Wait for the interrupt
7) Stop the measurement
   - regMap.MODE_SELECT = 0x00
   - wait 10us;
8) Flush the FIFO
   - regMap.FIFO_FILL = 0x80;
9) Reconfigure the interrupt settings if required for the application and detection of measurement data
10) Start a measurement
    - regMap.MODE_SELECT.MEAS_CONFIG = M (M is the selected mode)
    - regMap.MODE_SELECT.MEAS_MODE = 1
    - regMap.MODE_SELECT.POWER_MODE = 0

11) Wait for the interrupt or use another mechanism (polling, fixed wait) to detect if measurement data is available
12) Read the data from FIFO registers
    - Press[7:0] = regMap.PRESS_DATA_0
    - Press[15:8] = regMap.PRESS_DATA_1
    - Press[19:16] = regMap.PRESS_DATA_2
    - Temp[7:0] = regMap.TEMP_DATA_0
    - Temp[15:8] = regMap.TEMP_DATA_1
    - Temp[19:16] = regMap.TEMP_DATA_2
13) Repeat step 12 until the FIFO is empty

In case FIR filter is disabled (for operation mode 4) the first sample after mode change need to be ignored.

6.4 IIR FILTER

The ICP-20100 includes an IIR filter in the signal path, to filter out pressure glitches due to sudden pressure changes caused by events such as slamming door, or wind blowing on the sensor. The IIR filter is a 1st order filter with programmable cut-off frequency.

For details on how to program and use the IIR filter, refer to the application note "*AN-000238: ICP-20100 and ICP-20132 User Configurable Operation Mode and IIR Filter*."

6.5 BOOT SEQUENCE

Before starting any measurement, the device needs to be configured. This section lists the different steps to be taken before being able to conduct a measurement.

The following terminology is used in this code for register map references:

regMap.Register_Name.Register_Field_Name = Value

where

- "Register_Name" is the register name
- "Register_Field_Name" is the name of the register field in the register
- "Value" is the value being written to the specified register field

1) Power-on the ASIC
2) Initialize the I^2C interface by toggling the clock line a few times. The easiest way to do that is by inserting a dummy I^2C write transaction. You can for example execute the first transaction (write to lock register) twice.
3) Check the value from register regMap.version:
    - If 0x00 (version A), continue to step 4.
    - If 0xB2 (version B), no further initialization is required.
4) Check the value from register regMap. OTP_STATUS2. BOOT_UP_STATUS

- If 1, ICP-20100 didn't go through power cycle after previous boot up sequence. No further initialization is required.
- If 0, boot up config is not done after ICP-20100 power on. Continue to step 5

5) Bring the ASIC in power mode to activate the OTP power domain and get access to the main registers
   - regMap.MODE_SELECT.POWER_MODE = 1
   - Wait 4ms;
6) Unlock the main registers
   - regMap.MASTER_LOCK.LOCK = 0x1f
7) Enable the OTP and the write switch
   - regMap.OTP_CONFIG1.OTP_ENABLE = 1;
   - regMap.OTP_CONFIG1.OTP_WRITE_SWITCH = 1;
   - wait 10µs;
8) Toggle the OTP reset pin
   - regMap.OTP_DBG2.RESET = 1
   - wait 10us
   - regMap.OTP_DBG2.RESET = 0
   - wait 10us
9) Program redundant read
   - regMap.OTP_MRA_LSB = 0x04
   - regMap.OTP_MRA_MSB = 0x04
   - regMap.OTP_MRB_LSB = 0x21
   - regMap.OTP_MRB_MSB = 0x20
   - regMap.OTP_MR_LSB = 0x10
   - regMap.OTP_MR_MSB = 0x80
10) Write the address content and read command
   - regMap.OTP_ADDRESS.ADDRESS = 8'hF8 // for offset
   - regMap.OTP_COMMAND.ADDRESS = 4'h0
   - regMap.OTP_COMMAND.COMMAND = 1 // read action
11) Wait for the OTP read to finish
   - Monitor regMap.OTP_STATUS.BUSY to be 0
12) Read the data from register
   - Offset = regMap.OTP_RDATA.VALUE
13) Write the next address content and read command
   - regMap.OTP_ADDRESS.ADDRESS = 8'hF9 // for gain
   - regMap.OTP_COMMAND.ADDRESS = 4'h0

- regMap.OTP_COMMAND.COMMAND = 1 // read action

14) Wait for the OTP read to finish
    - Monitor regMap.OTP_STATUS.BUSY to be 0
15) Read the data from register
    - Gain = regMap.OTP_RDATA.VALUE
16) Write the next address content and read command
    - regMap.OTP_ADDRESS.ADDRESS = 8'hFA // for HFosc
    - regMap.OTP_COMMAND.ADDRESS = 4'h0
    - regMap.OTP_COMMAND.COMMAND = 1 // read action
17) Wait for the OTP read to finish
    - Monitor regMap.OTP_STATUS.BUSY to be 0
18) Read the data from register
    - HFosc = regMap.OTP_RDATA.VALUE
19) Disable OTP and write switch
    - regMap.OTP_CONFIG1.OTP_ENABLE = 0;
    - regMap.OTP_CONFIG1.OTP_WRITE_SWITCH = 0;
    - wait 10µs;
20) Write the Offset to the main registers
    - regMap.TRIM1_MSB.PEFE_OFFSET_TRIM = Offset[5:0]
21) Write the Gain to the main registers without touching the parameter BG_PTAT_TRIM
    - Rdata = regMap.TRIM2_MSB
    - Rdata[6:4] = Gain[2:0]
    - regMap.TRIM2_MSB = Rdata
22) Write the HFosc trim value to the main registers
    - regMap.TRIM2_LSB = HFosc
23) Lock the main registers
    - regMap.MASTER_LOCK.LOCK = 0x00
24) Move to standby
    - regMap.MODE_SELECT.POWER_MODE = 0
25) Write bootup config status to 1 to avoid re initialization with out power cycle.

    regMap. OTP_STATUS2. BOOT_UP_STATUS = 1

Note: The bootup sequence should be run only once for every powerup. Running the boot sequence multiple times could create issues.

6.6 MODE SWITCHING/SELECTION

Mode switching/selection is done by

- Making sure the previous mode is selected by reading the register field MODE_SYNC_STATUS of register DEVICE_STATUS until it is set to '1'.
- Starting the new mode by selecting it in the register field MEAS_CONFIG of register MODE_SELECT.

6.7 PRESSURE/TEMPERATURE READ-OUT

Pressure and temperature are read out by

- Waiting until the FIFO contains data (either by polling the FIFO_LEVEL register field in register FIFO_FILL or though configuration of the FIFO watermark high interrupt).
- Read out registers PRESS_DATA_0, PRESS_DATA_1, PRESS_DATA_2, TEMP_DATA_0 , TEMP_DATA_1, and TEMP_DATA_2 using the address increment burst feature of the SPI, I^2C or $I3C^{SM}$ interface. The FIFO read pointer will automatically increment on reading the last register TEMP_DATA_2. The read address will automatically wrap to address PRESS_DATA_0 (in case of Pressure first mode refer to section 7). This means that multiple FIFO locations can be read out by continuously using the interface address increment function until the FIFO is empty.

6.7.1 Pressure conversion formula

The 20-bit output pressure value represents a two's complement integer from -2^{19} till $2^{19}-1$

To convert this value into pressure, use the formula

$P = (P_{OUT}/2^{17})*40kPa + 70kPa$

- P: pressure in kPa
- P_{OUT}: two's complement representation of the pressure output code

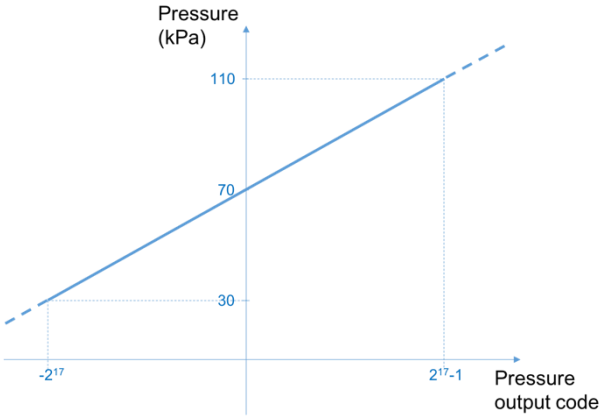


Figure 16. Pressure Output Code

6.7.2 Temperature conversion formula

The 20-bit output temperature value represents a two's complement integer from -2^{19} till $2^{19}-1$

To convert this value into temperature, use the formula

$T = (T_{OUT}/2^{18})*65C + 25C$

- T: temperature in degrees Celsius
- T_{OUT}: two's complement representation of the temperature output code

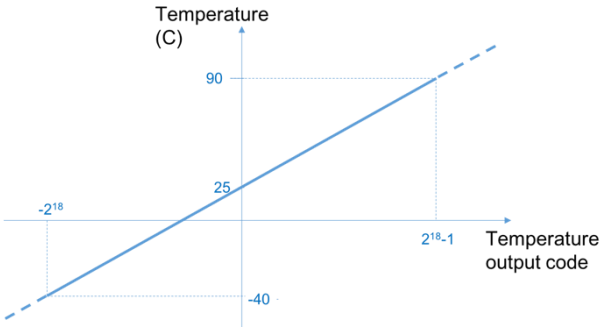


Figure 17. Temperature Output Code

7 FIFO

A 96-bytes FIFO allows to buffer up to 16 pressure and temperature measurement pairs before reading them out through I²C, I3C^SM or SPI.

Four modes are supported when reading out the FIFO with address increment:

- Pressure first: The address wraps to the start address of the Pressure value
- Temperature only: The address wraps to the start address of the Temperature value
- Temperature first: Temperature and pressure locations are switched, the address wraps to the start address of the Temperature value
- Pressure only: Temperature and pressure locations are switched, the address wraps to the start address of the Pressure value

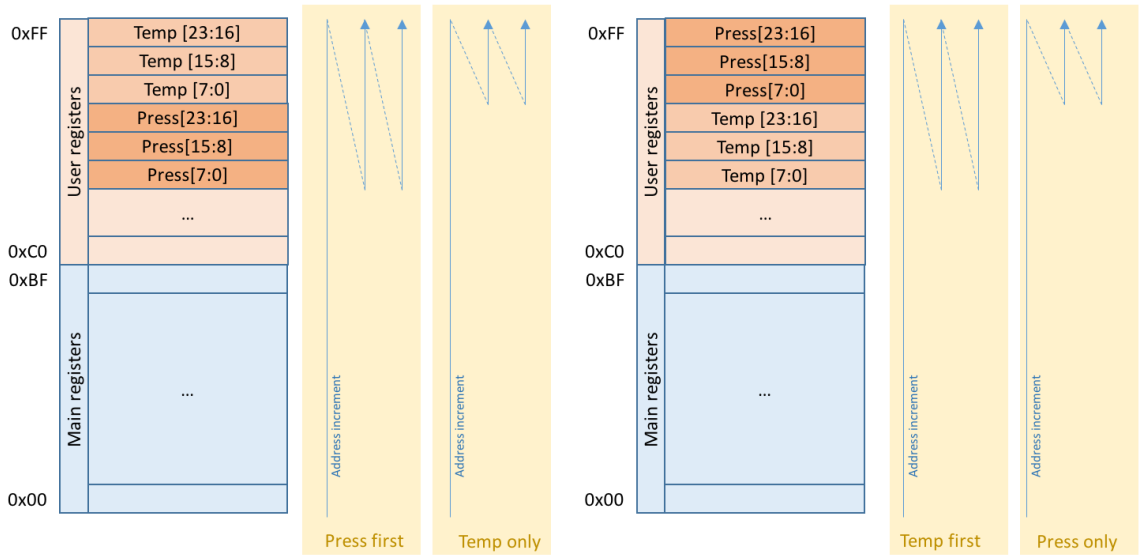


Figure 18. FIFO Read Out Modes

7.1 FIFO ACCESSIBILITY

The Measurement FIFO registers are accessible from the I²C/I3C^SM/SPI interface in all operating modes, including Standby mode.

The Measurement FIFO registers need to be read out in burst mode for I²C/I3C^SM. The data that is read out is not guaranteed to be consistent if every byte is addressed separately.

7.2 FIFO FULL/EMPTY

A FIFO full flag is raised when the FIFO level reaches the FIFO size.

Data is not written to the FIFO if it is full. The FIFO full flag is reset when the FIFO level drops below the FIFO size by fetching a FIFO word through from the $I^2C/I3C^{SM}$/SPI interface.

A FIFO empty flag is raised when the FIFO level reaches 0.

A read transaction from the FIFO returns 0x00 values if it is empty. The FIFO empty flag is reset when the FIFO level increases above 0.

7.3 FIFO OVERFLOW/UNDERFLOW

A FIFO overflow flag is raised when a new pressure/temperature pair is written to the FIFO while it is full. The written pressure/temperature pair is ignored. The FIFO overflow flag is latched and can be reset by setting it through the $I^2C/I3C^{SM}$/SPI interface.

A FIFO underflow flag is raised when a pressure/temperature pair is fetched from the FIFO while it is empty. The data read from the FIFO contains 0x00 values. The FIFO underflow flag is latched and can be reset by setting it through the $I^2C/I3C^{SM}$/SPI interface.

7.4 FIFO WATERMARK LOW/HIGH

Two FIFO watermark register fields, FIFO_WMK_LOW and FIFO_WMK_HIGH, can be used to manage the data flow from the sensor to the host.

The watermark high flag is set when the FIFO level reaches the high value watermark specified by FIFO_WMK_HIGH.

The watermark low flag is set when the FIFO level reaches the low value watermark specified by FIFO_WMK_LOW.

The FIFO watermark flags are latched and can be reset by setting them through the $I^2C/I3C^{SM}$/SPI interface.

7.5 FIFO FLUSH

A FIFO flush command allows the user to flush the FIFO. The register field FLUSH should be set to 1 to flush the FIFO.

7.6 ABSOLUTE PRESSURE VALUE OVERRUN/UNDERRUN

An absolute pressure value overrun flag is raised when the pressure value crosses a configurable 16-bit pressure overrun/underrun value. This value is configurable in the user register map using registers PRESS_ABS_LSB and PRESS_ABS_MSB.

7.7 DELTA PRESSURE VALUE OVERRUN

A delta pressure value overrun flag is raised when the absolute difference between 2 consecutive pressure values exceeds a configurable 16-bit delta pressure overrun value. This value is configurable in the user register map, using registers PRESS_DELTA_LSB and PRESS_DELTA_MSB.

8 INTERRUPTS

The interrupt pin is open-drain. It is pulled high by default by an internal pull-up resistor. On an interrupt event, it is driven low until the interrupt source has been cleared through the I^2C/$I3C^{SM}$/SPI interface.

The interrupt can be configured to be connected to any of the following interrupt sources:

- FIFO overflow
- FIFO underflow
- FIFO watermark low
- FIFO watermark high
- Absolute pressure threshold overrun
- Absolute pressure threshold underrun
- Delta pressure threshold overrun

Each interrupt source can be individually masked.

9 ASSEMBLY

This section provides general guidelines for assembling TDK Micro Electro-Mechanical Systems (MEMS) pressure sensors.

9.1 IMPLEMENTATION AND USAGE RECOMMENDATIONS

9.1.1 Soldering

When soldering, use the standard soldering profile IPC/JEDEC J-STD-020 with peak temperatures of 260°C. ICP-20100 may exhibit a pressure offset after soldering, some settling time may be required depending on soldering properties, PCB properties, and ambient conditions.

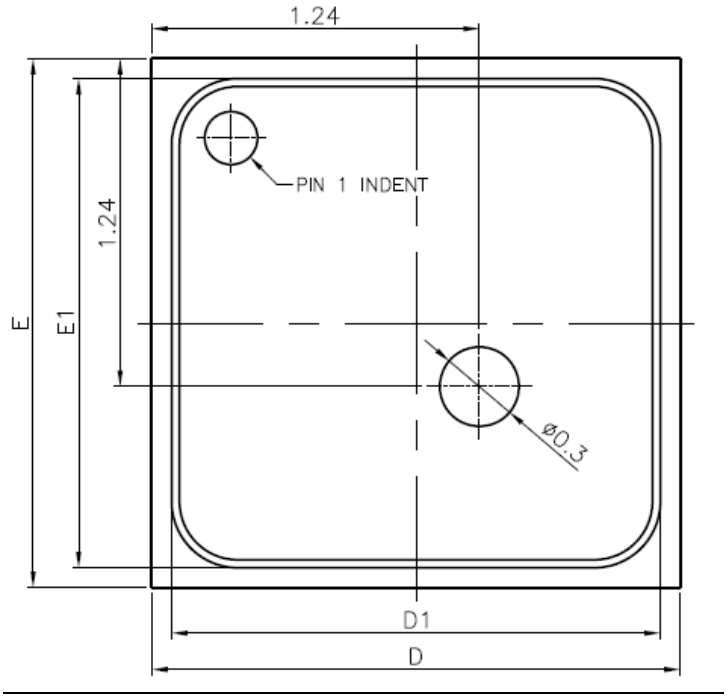
ICP-20100 devices have MSL rating 1, appropriate JEDEC J-STD-020 guidelines should be followed to avoid damaging the part.

9.1.2 Chemical Exposure and Sensor Protection

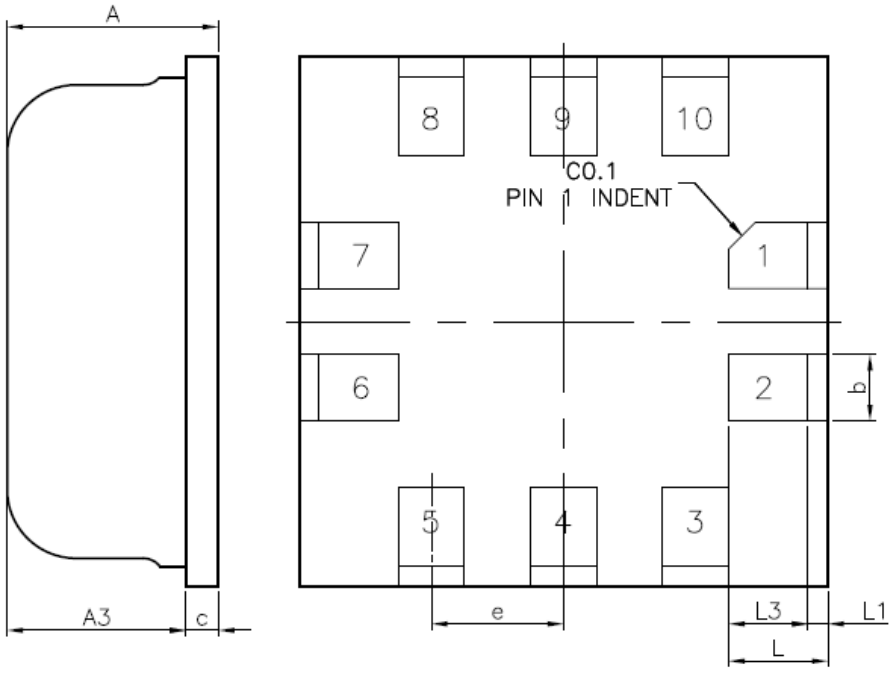
The ICP-20100 is an open cavity package and should not be exposed to particulates or liquids. If any type of protective coating must be applied to the circuit board, the sensor must be protected during the coating process.

10 PACKAGE DIMENSIONS

Package dimensions for the ICP-20100:



Top View: ICP-20100



Bottom View: ICP-20100

Figure 19. ICP-20100 Package Diagrams

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.750	0.800	0.850
A3	0.655	0.675	0.695
b	0.200	0.250	0.300
c	0.100	0.125	0.150
D	1.950	2.000	2.050
D1	1.820	1.850	1.880
E	1.950	2.000	2.050
E1	1.820	1.850	1.880
e	0.450	0.500	0.550
L	0.275	0.375	0.425
L1	0.025	0.075	0.100
L3	0.250	0.300	0.325

Table 19. ICP-20100 Package Dimensions

11 PART NUMBER PART MARKINGS

The part number part markings for ICP-20100 devices are summarized below:

PART NUMBER	PART MARKING
ICP-20100	S1

Table 20. Part Number Part Markings

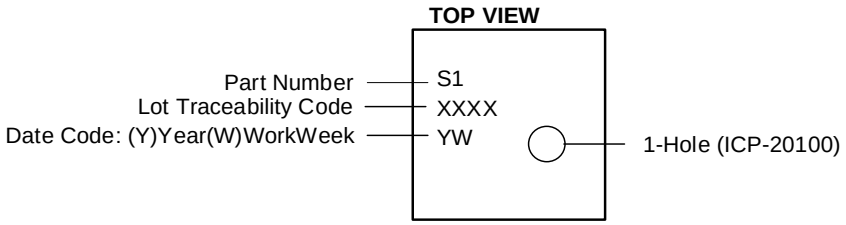


Figure 20. Part Number Part Markings for ICP-20100

12 REGISTER MAP

This section lists the register map for ICP-20100.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5	5	TRIM1_MSB	R/W	-		PEFE_OFFSET_TRIM					
6	6	TRIM2_LSB	R/W		HF_OSC_TRIM						
7	7	TRIM2_MSB	R/W	-	PEFE_GAIN_TRIM			BG_PTAT_TRIM			
C	12	DEVICE_ID	RO	VALUE							
D	13	IO_DRIVE_STRENGTH	R/W	-					IO_DS		
AC	172	OTP_CONFIG1	R/W	-						OTP_EN	OTP_WR
AD	173	OTP_MR_LSB	R/W	VALUE_LSB							
AE	174	OTP_MR_MSB	R/W	VALUE_MSB							
AF	175	OTP_MRA_LSB	R/W	VALUE_LSB							
B0	176	OTP_MRA_MSB	R/W	VALUE_MSB							
B1	177	OTP_MRB_LSB	R/W	VALUE_LSB							
B2	178	OTP_MRB_MSB	R/W	VALUE_MSB							
B5	181	OTP_ADDRESS_REG	R/W	OTP_ADDRESS_LSB							
B6	182	OTP_COMMAND_REG	R/W	-	COMMAND			OTP_ADDRESS_MSB			
B8	184	OTP_RDATA	R	VALUE							
B9	185	OTP_STATUS	R	-							BUSY
BC	188	OTP_DBG2	R/W	RESET	-						
BE	190	MASTER_LOCK	W	LOCK							
BF	191	OTP_STATUS2	R/W	-							BOOT_UP_STATUS
C0	192	MODE_SELECT	R/W	MEAS_CONFIG			FORCED_MEAS_TRIGGER	MEAS_MODE	POWER_MODE	FIFO_READOUT_MODE	
C1	193	INTERRUPT_STATUS	R/W	-	PRESS_DELTA_INT	PRESS_ABS_INT	-	FIFO_WM_LOW_INT	FIFO_WM_HIGH_INT	FIFO_UNDERFLOW_INT	FIFO_OVERFLOW_INT
C2	194	INTERRUPT_MASK	R/W	-	PRESS_DELTA_MASK	PRESS_ABS_MASK	-	FIFO_WM_LOW_MASK	FIFO_WM_HIGH_MASK	FIFO_UNDERFLOW_MASK	FIFO_OVERFLOW_MASK
C3	195	FIFO_CONFIG	R/W	FIFO_WM_HIGH				FIFO_WM_LOW			
C4	196	FIFO_FILL	R/W	FIFO_FLUSH	FIFO_EMPTY	FIFO_FULL	FIFO_LEVEL				
C5	197	SPI_MODE	R/W	-							SPI_MODE
C7	199	PRESS_ABS_LSB	R/W	PRESS_ABS_LSB							
C8	200	PRESS_ABS_MSB	R/W	PRESS_ABS_MSB							
C9	201	PRESS_DELTA_LSB	R/W	PRESS_DELTA_LSB							
CA	202	PRESS_DELTA_MSB	R/W	PRESS_DELTA_MSB							
CD	205	DEVICE_STATUS	R	-							MODE_SYNC_STATUS
CE	206	I3C_INFO	R	I3C_INFO							
D3	211	VERSION	R	MAJOR				MINOR			
FA	250	PRESS_DATA_0	R	PRESS_DATA_0							
FB	251	PRESS_DATA_1	R	PRESS_DATA_1							
FC	252	PRESS_DATA_2	R	-				PRESS_DATA_2			
FD	253	TEMP_DATA_0	R	TEMP_DATA_0							
FE	254	TEMP_DATA_1	R	TEMP_DATA_1							
FF	255	TEMP_DATA_2	R	-				TEMP_DATA_2			

Table 21. Register Map

13 REGISTER MAP DESCRIPTION

This section describes the function and contents of each register.

13.1 TRIM1_MSB

Name: TRIM1_MSB
Address: 5 (0x05)
Serial IF: R/W
Reset value: Device dependent

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	PEFE_OFFSET_TRIM	Trim value for the pressure front-end

13.2 TRIM2_LSB

Name: TRIM2_LSB
Address: 6 (0x06)
Serial IF: R/W
Reset value: Device dependent

BIT	NAME	FUNCTION
7	-	Reserved
6:0	HFOSC_TRIM	Trim value for the high frequency oscillator

13.3 TRIM2_MSB

Name: TRIM1_MSB
Address: 7 (0x07)
Serial IF: R/W
Reset value: Device dependent

BIT	NAME	FUNCTION
7	-	Reserved
6:4	PEFE_GAIN_TRIM	Trim value for the pressure front-end
3:0	BG_PTAT_TRIM	Trim value for PTAT current

13.4 DEVICE_ID

Name: DEVICE_ID
Address: 12 (0x0C)
Serial IF: RO
Reset value: 0x63

BIT	NAME	FUNCTION
7:0	VALUE	8-bit Device ID

13.5 IO_DRIVE_STRENGTH

Name: IO_DRIVE_STRENGTH
Address: 13 (0x0D)
Serial IF: R/W
Reset value: 0x03

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	IO_DS	IO drive strength value 000: 2 mA for 1.8V IO supply 001: 4 mA for 1.8V IO supply 010: 8 mA for 1.8V IO supply 011: 12 mA for 1.8V IO supply 100: 2 mA for 1.2V IO supply 101: 4 mA for 1.2V IO supply 110: 6 mA for 1.2V IO supply 111: 8 mA for 1.2V IO supply

13.6 OTP_CONFIG1

Name: OTP_CONFIG1
Address: 172 (0xAC)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:2	RESERVED	-
1	OTP_WRITE_SWITCH	Connect OTP VCC to VCORE. This is needed for OTP write. VCORE should be 3V3 in this case
0	OTP_ENABLE	Enable the OTP

13.7 OTP_MR_LSB

Name: OTP_MR_LSB
Address: 173 (0xAD)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_LSB	OTP MR register bits 7:0

13.8 OTP_MR_MSB

Name: OTP_MR_MSB
Address: 174 (0xAE)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_MSB	OTP MR register bits 15:8

13.9 OTP_MRA_LSB

Name: OTP_MRA_LSB
Address: 175 (0xAF)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_LSB	OTP MRA register bits 7:0

13.10 OTP_MRA_MSB

Name: OTP_MRA_MSB
Address: 176 (0xB0)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_MSB	OTP MRA register bits 15:8

13.11 OTP_MRB_LSB

Name: OTP_MRB_LSB
Address: 177 (0xB1)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_LSB	OTP MRB register bits 7:0

13.12 OTP_MRB_MSB

Name: OTP_MRB_MSB
Address: 178 (0xB2)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE_MSB	OTP MRB register bits 15:8

13.13 OTP_ADDRESS

Name: OTP_ADDRESS
Address: 181 (0xB5)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	ADDRESS	OTP address [7:0] to read from or to write to

13.14 OTP_COMMAND

Name: OTP_COMMAND
Address: 182 (0xB6)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	RESERVED	-
6:4	COMMAND	OTP access command
3:0	ADDRESS	OTP address [11:8] to read from or to write to

13.15 OTP_RDATA

Name: OTP_RDATA
Address: 184 (0xB8)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	VALUE	OTP read data word

13.16 OTP_STATUS

Name: OTP_STATUS
Address: 185 (0xB9)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:1	RESERVED	-
0	BUSY	OTP controller BUSY flag

13.17 OTP_DBG2

Name: OTP_DBG2
Address: 188 (0xBC)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	RESET	Value of the OTP port RESET
6:0	RESERVED	-

13.18 OTP_STATUS2

Name: OTP_STATUS2
Address: 191 (0xBF)
Serial IF: R/W
Reset value: 0xF0

BIT	NAME	FUNCTION
7:1	RESERVED	-

0	BOOT_UP_STATUS	Boot up config status. Host can set this bit to 1 when boot up config is done and read later to know if ICP-20100 is power cycled and needs boot up config.

13.19 MASTER_LOCK

Name: MASTER_LOCK
Address: 190 (0xBE)
Serial IF: W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	LOCK	Write 8'h1F to unlock write access to all main registers Write any other value to lock write access to all main registers The OTP mirror registers are not locked by this register

13.20 MODE_SELECT

Name: MODE_SELECT
Address: 192 (0xC0)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:5	MEAS_CONFIG	Measurement Configuration (the modes listed below are described in section 2.2) 000: Mode0 001: Mode1 010: Mode2 011: Mode3 100: Mode4 101 to 111: Reserved
4	FORCED_MEAS_TRIGGER	Initiate Triggered Operation (also called Forced Measurement Mode) 0: Stay in Standby mode 1: Trigger for forced measurement (only supported for Mode4)
3	MEAS_MODE	Measurement Mode Selection 0: Standby or trigger forced measurement based on the field FORCED_MEAS_TRIGGER 1: Continuous Measurements (duty cycled): Measurements are started based on the selected mode ODR_REG
2	POWER_MODE	Power Mode Selection 0: Normal Mode: Device is in standby and goes to active mode during the execution of a measurement 1: Active Mode: Power on DVDD and enable the high frequency clock
1:0	FIFO_READOUT_MODE	FIFO Readout Mode Selection (refer to the FIFO section for further information) 00: Pressure first. When you start reading from address 0xFA with address increment, you will read out press(n), temp(n), press(n+1), temp(n+1), … 01: Temperature only. When you start reading from address 0xFD with address increment, you will read out temp(n), temp(n+1), …

		10: Temperature first. When you start reading from address 0xFA with address increment, you will read out temp(n), press(n), temp(n+1), press(n+1), … 11: Pressure only. When you start reading from address 0xFD with address increment, you will read out press(n), press(n+1), …
Notes: - Make sure DEVICE_STATUS.MODE_SYNC_STATUS bit is set before writing this register.		

13.21 INTERRUPT_STATUS

Name: INTERRUPT_STATUS
Address: 193 (0xC1)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved
6	PRESS_DELTA_INT	Delta pressure overrun Read 0: The difference between 2 consecutive pressure measurements after filtering didn't exceed the programmed delta pressure overrun value. The interrupt has not triggered 1: The difference between 2 consecutive pressure measurements after filtering exceeded the programmed delta pressure overrun value. The interrupt has triggered Write policy is W1C 0: the press_delta_int interrupt status bit is unchanged 1: the press_delta_int interrupt status bit is cleared
5	PRESS_ABS_INT	Pressure underrun/overrun Read 0: The pressure value didn't cross the programmed pressure underrun/overrun value. The interrupt has not triggered 1: The pressure value crossed the programmed pressure underrun/overrun value. The interrupt has triggered Write policy is W1C 0: the press_abs interrupt status bit is unchanged 1: the press_abs interrupt status bit is cleared
4	-	Reserved
3	FIFO_WMK_LOW_INT	FIFO watermark low Read 0: The FIFO fill level didn't reach in downward direction the programmed watermark low value. The interrupt has not triggered 1: The FIFO fill level reached in downward direction the programmed watermark low value. The interrupt has triggered Write policy is W1C 0: the fifo_wmk_low interrupt status bit is unchanged 1: the fifo_wmk_low interrupt status bit is cleared
2	FIFO_WMK_HIGH_INT	FIFO watermark high Read 0: The FIFO fill level didn't reach in upward direction the programmed watermark high value. The interrupt has not triggered 1: The FIFO fill level reached in upward direction the programmed watermark high value. The interrupt has triggered

		Write policy is W1C 0: the fifo_wmk_high interrupt status bit is unchanged 1: the fifo_wmk_high interrupt status bit is cleared
1	FIFO_UNDERFLOW_INT	FIFO underflow Read 0: No new pressure/temperature pair was fetched from the FIFO while it was empty. The interrupt has not triggered 1: A new pressure/temperature pair was fetched from the FIFO while it was empty. The interrupt has triggered Write policy is W1C 0: the fifo_underflow interrupt status bit is unchanged 1: the fifo_underflow interrupt status bit is cleared
0	FIFO_OVERFLOW_INT	FIFO overflow Read 0: No new pressure/temperature pair was written to the FIFO while it was full. The interrupt has not triggered 1: A new pressure/temperature pair was written to the FIFO while it was full. The interrupt has triggered Write policy is W1C 0: the fifo_overflow interrupt status bit is unchanged 1: the fifo_overflow interrupt status bit is cleared

13.22 INTERRUPT_MASK

Name: INTERRUPT_MASK
Address: 194 (0xC2)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7	-	Reserved (program to 1)
6	PRESS_DELTA_MASK	0: PRESS_DELTA interrupt is not masked 1: PRESS_DELTA interrupt is masked
5	PRESS_ABS_MASK	0: PRESS_ABS interrupt is not masked 1: PRESS_ABS interrupt is masked
4	-	Reserved
3	FIFO_WMK_LOW_MASK	0: FIFO_WMK_LOW interrupt is not masked 1: FIFO_WMK_LOW interrupt is masked
2	FIFO_WMK_HIGH_MASK	0: FIFO_WMK_HIGH interrupt is not masked 1: FIFO_WMK_HIGH interrupt is masked
1	FIFO_UNDERFLOW_MASK	0: FIFO_UNDERFLOW interrupt is not masked 1: FIFO_UNDERFLOW interrupt is masked
0	FIFO_OVERFLOW_MASK	0: FIFO_OVERFLOW interrupt is not masked 1: FIFO_OVERFLOW interrupt is masked

13.23 FIFO_CONFIG

Name: FIFO_CONFIG
Address: 195 (0xC3)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	FIFO_WM_HIGH	FIFO high watermark value. Interrupt is triggered when the FIFO fill level reaches this value in the upward direction. A value of 0 disables the high watermark check.
3:0	FIFO_WM_LOW	FIFO low watermark value. Interrupt is triggered when the FIFO fill level reaches this value in the downward direction.

13.24 FIFO_FILL

Name: FIFO_FILL
Address: 196 (0xC4)
Serial IF: R/W
Reset value: 0x40

BIT	NAME	FUNCTION
7	FIFO_FLUSH	FIFO flush command. (This field should not be modified while doing a measurement) 0: No change 1: FIFO is flushed. Flushing the FIFO will empty it.
6	FIFO_EMPTY	FIFO empty indication. 0: The FIFO level is above 0 1: The FIFO level is at 0
5	FIFO_FULL	FIFO full indication. 0: The FIFO level is below the FIFO size 1: The FIFO level has reached the FIFO size
4:0	FIFO_LEVEL	FIFO fill level 00000: Empty 00001: 1/16 full 00010: 2/16 full 00011: 3/16 full 00100: 4/16 full 00101: 5/16 full 00110: 6/16 full 00111: 7/16 full 01000: 8/16 full 01001: 9/16 full 01010: 10/16 full 01011: 11/16 full 01100: 12/16 full 01101: 13/16 full 01110: 14/16 full 01111: 15/16 full 10000: Full 10001 to 11111: Reserved

13.25 SPI_MODE

Name: SPI_MODE
Address: 197 (0xC5)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:1	-	Reserved
0	SPI_MODE	0: SPI 4-wire mode enabled 1: SPI 3-wire mode enabled

13.26 PRESS_ABS_LSB

Name: PRESS_ABS_LSB
Address: 199 (0xC7)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_ABS_LSB	LSB part of the 16bit pressure overrun/underrun value. The 16bit value represents pressure values according to the formula P_{ABS} = (P(kPa)-70kPa)/40kPa*2^{13} For example, 80 kPa threshold results in value 0x0800, 50 kPa results in value 0xF000 This register should not be modified while doing a measurement.

13.27 PRESS_ABS_MSB

Name: PRESS_ABS_MSB
Address: 200 (0xC8)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_ABS_MSB	MSB part of the 16bit pressure overrun/underrun value. The 16bit value represents pressure values according to the formula P_{ABS} = (P(kPa)-70kPa)/40kPa*2^{13} For example, 80kPa threshold results in value 0x0800, 50 kPa results in value 0xF000 This register should not be modified while doing a measurement.

13.28 PRESS_DELTA_LSB

Name: PRESS_DELTA_LSB
Address: 201 (0xC9)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_DELTA_LSB	LSB part of the 16bit delta pressure overrun/underrun value. The 16bit value represents pressure values according to the formula P_{DELTA} = (P(kPa)/80)* 2^{14} For example, a delta pressure of 0.5 kPa is represented by the value 0x0066 This register should not be modified while doing a measurement.

13.29 PRESS_DELTA_MSB

Name: PRESS_DELTA_MSB
Address: 202 (0xCA)
Serial IF: R/W
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_DELTA_MSB	MSB part of the 16bit delta pressure overrun/underrun value. The 16bit value represents pressure values according to the formula P_{DELTA} = (P(kPa)/80)* 2^{14} For example, a delta pressure of 0.5 kPa is represented by the value 0x0066 This register should not be modified while doing a measurement.

13.30 DEVICE_STATUS

Name: DEVICE_STATUS
Address: 205 (0xCD)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:6	-	Reserved
0	MODE_SYNC_STATUS	0: Synchronization of the selected mode to the internal clock domain is ongoing. MODE_SELECT register is not accessible by the user. 1: Synchronization of the selected mode to the internal clock domain is finished. MODE_SELECT register is accessible by the user.

13.31 I3C_INFO

Name: I3C_INFO
Address: 206 (0xCE)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	I3C_INFO	This register contains the I3C^{SM} dynamic slave address

13.32 VERSION

Name: VERSION
Address: 211 (0xD3)
Serial IF: R
Reset value: 0x00 (version A); 0xB2 (version B)

BIT	NAME	FUNCTION
7:4	MAJOR	Major version number
3:0	MINOR	Minor version number

13.33 PRESS_DATA_0

Name: PRESS_DATA_0
Address: 250 (0xFA)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_DATA_0	Pressure data bits [7:0]

13.34 PRESS_DATA_1

Name: PRESS_DATA_1
Address: 251 (0xFB)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	PRESS_DATA_1	Pressure data bits [15:8]

13.35 PRESS_DATA_2

Name: PRESS_DATA_2
Address: 252 (0xFC)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	PRESS_DATA_2	Pressure data bits [19:16]

13.36 TEMP_DATA_0

Name: TEMP_DATA_0
Address: 253 (0xFD)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_DATA_0	Temperature data bits [7:0]

13.37 TEMP_DATA_1

Name: TEMP_DATA_1
Address: 254 (0xFE)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:0	TEMP_DATA_1	Temperature data bits [15:8]

13.38 TEMP_DATA_2

Name: TEMP_DATA_2
Address: 255 (0xFF)
Serial IF: R
Reset value: 0x00

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	TEMP_DATA_2	Temperature data bits [19:16]

14 TAPE & REEL SPECIFICATION

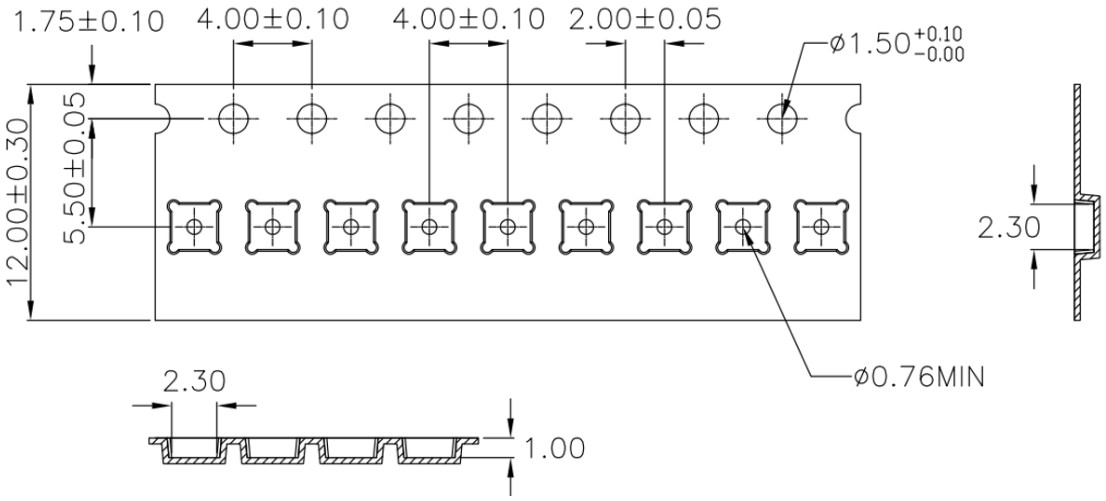


Figure 21. ICP-20100 Tape Dimensions

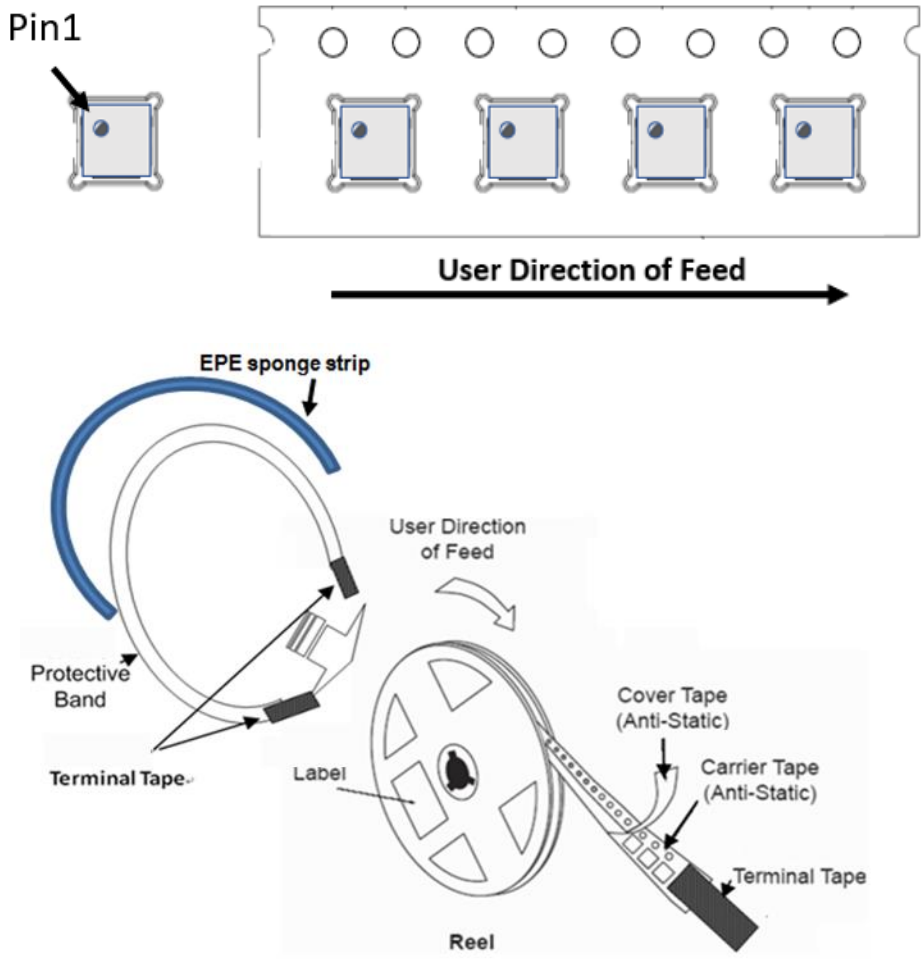


Figure 22. ICP-20100 Tape and Reel Drawing

15 ORDERING GUIDE

PART	TEMP RANGE	PACKAGE BODY	PACKAGE LID	QUANTITY	PACKAGING
ICP-20100†	−40°C to +85°C	2x2x0.8mm LGA-10L	1-Hole	10,000	13” Tape and Reel

†Denotes RoHS and Green-Compliant Package

16 REFERENCES

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” and “Pressure Sensor PCB Design Guidelines (AN-000140)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

17 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
10/12/2020	0.1	Initial Release
03/12/2021	0.2	Updated ASIC Identification Procedure (Section 5.4); Updated Duty Cycled Operation Description (Section 6.2.1); Updated FIFO FULL/EMPTY Description (Section 7.2); Moved sections on FIFO OVERFLOW/UNDERFLOW, FIFO WATERMARK LOW/HIGH, ABSOLUTE PRESSURE VALUE OVERRUN/UNDERRUN, DELTA PRESSURE VALUE OVERRUN from Section 7 to Section 8.
04/01/2021	0.3	Updated Pressure Sensor Specifications (Table 3); Updated ASIC Identification Procedure (Section 5.4); Updated Duty Cycled Operation Description (Section 6.2.1); Updated Interrupts (Section 8).
05/03/2021	0.4	Added MSL information (Cover Page); Added Tape & Reel Specification (Section 14).
07/09/2021	1.0	Updated Pressure Sensor Specifications (Table 3); Updated References (Section 16)
09/15/2021	1.1	Updated Table 3 Notes and Conditions; Added OSR_{PRESS} and OSR_{TEMP} Calculation (Section 6.2.1); Updated FIFO_FLUSH Register Field Description (Section 13.23)
12/08/2021	1.2	Updated Drive Strength for VDDIO = 1.2V and for VDDIO = 1.8V/3.3V (Section 3.1); Updated HBM from 2kV to 1.5kV (Section 3.2); Added new dummy reads for I2C and I3C (Section 4.1.3 and Section 4.1.4); Updated Drive Strength Configuration (Section 4.3); Updated FIR Filter section (Section 6.3); Updated drive strength (Section 13.5, 3.1); Updated boot section (Section 6.5); Updated ASIC identification section (Section 5.4, 13.31); Added register OTP_STATUS2 (Section 12, 13.18); Updated IO_DS description (Section 13.5); Added Notes (Section 13.20)
12/17/2021	1.3	Updated Boot Sequence (Section 6.5)

TDK InvenSense