



EVL3424A-G-00A

CC/CV, Configurable-Current, Synchronous Boost Converter with Output Disconnect and Low Inrush Current Evaluation Board

DESCRIPTION

The EVL3424A-G-00A is an evaluation board designed to demonstrate the capabilities of the MP3424A, a high-efficiency, current-mode, synchronous, step-up converter with output disconnect.

The MP3424A provides inrush current limiting, output short-circuit protection (SCP), and a configurable load current limit. The integrated P-channel rectifier improves efficiency and eliminates the need for an external Schottky diode. During shutdown, the P-channel MOSFET disconnects the output from the input.

The 580kHz switching frequency (f_{sw}) allows for small external components, while the internal compensation and soft start (SS) minimize the number of external components.

The MP3424A is available in a QFN-14 (2mmx2mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	2.8 to 4.2	V
Output Voltage	V_{OUT}	5	V
Output Current	I_{OUT}	3.1	A

FEATURES

- 2V to 5.5V Operating Input Range
- 3V to 5.5V Output Voltage Range
- Supports 5V/3.1A Output from a 2.8V Input
- 270mA Linear Charge Inrush Current
- Configurable Average Load Current Limit
- 580kHz Fixed Switching Frequency (f_{sw})
- Up to 97% Efficiency
- Output Load Disconnect from Input
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), Over-Temperature Protection (OTP)
- Available in a QFN-14 (2mmx2mm) Package



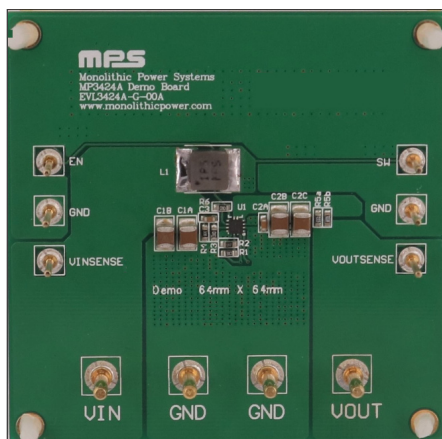
Optimized Performance with
MPS Inductor MPL-AL5030 Series

APPLICATIONS

- Battery-Powered Products
- Power Banks, Juice Packs, and Backup Batteries
- Optical Modules
- USB Power Supplies
- Consumer Electronic Accessories

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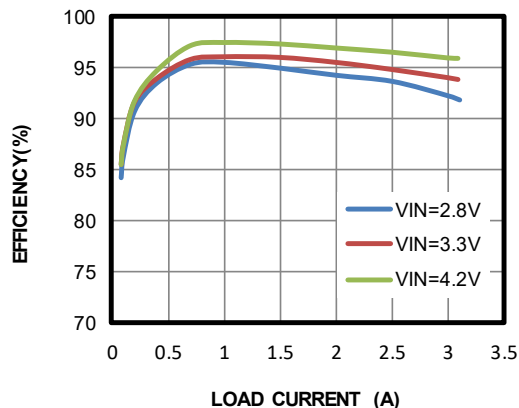
EVL3424A-G-00A EVALUATION BOARD



LxWxH (6.35cmx6.35cmx0.6cm)

Board Number	MPS IC Number	MPS Inductor
EVL3424A-G-00A	MP3424AGG	MPL-AL5030-1R5

Efficiency vs. Load Current



QUICK START GUIDE

The EVL3424A-G-00A's output voltage (V_{OUT}) is set to 5V. The board layout accommodates most commonly used components.

1. Preset the power supply between 2.8V and 4.2V.
2. Turn off the power supply.
3. Connect the power supply terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
4. Connect the load terminals to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
5. After making the connections, turn on the power supply. The board should start up automatically.
6. The board's V_{OUT} is set at 5V. V_{OUT} can be adjusted by changing the resistor (R2). Then V_{OUT} can be calculated with Equation (1):

$$V_{out} = V_{FB} \times \frac{R1+R2}{R2} \quad (1)$$

Where $V_{FB} = 0.805V$, and $R1 = 1M\Omega$.

7. To use the enable (EN) function, apply a digital input to the EN pin. Drive EN above 1.2V to turn the converter on; drive EN below 0.4V to turn it off.

EVALUATION BOARD SCHEMATIC

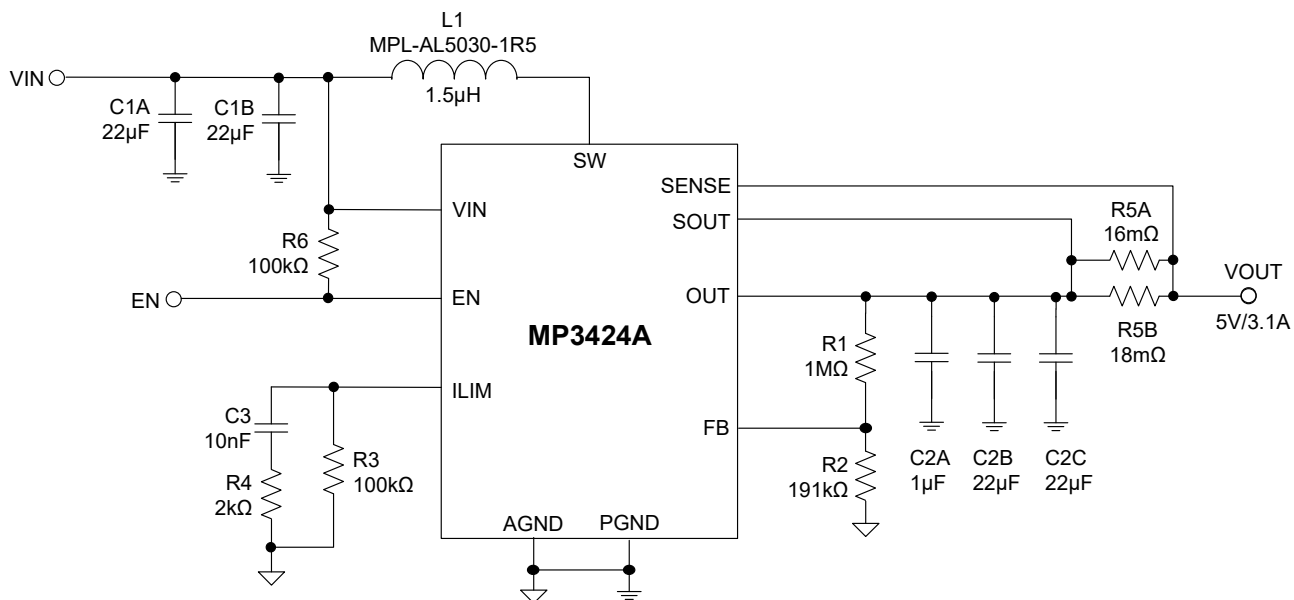


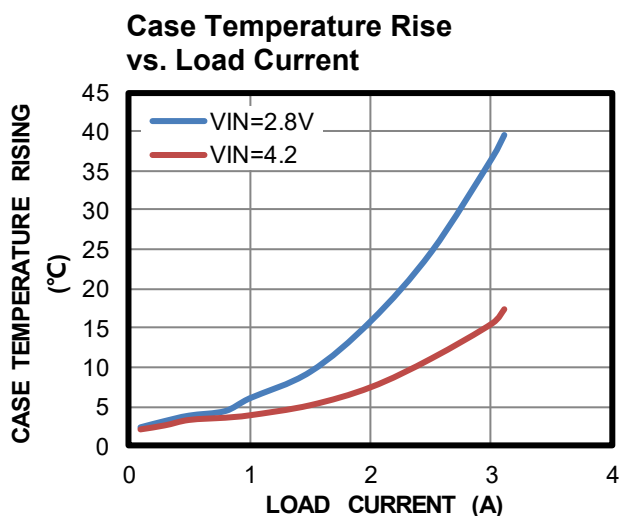
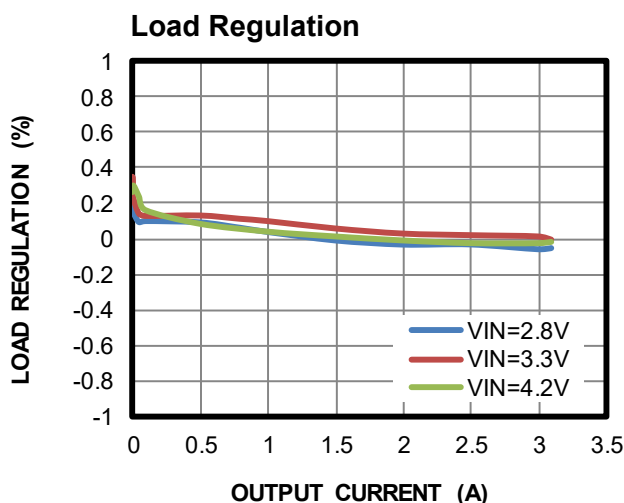
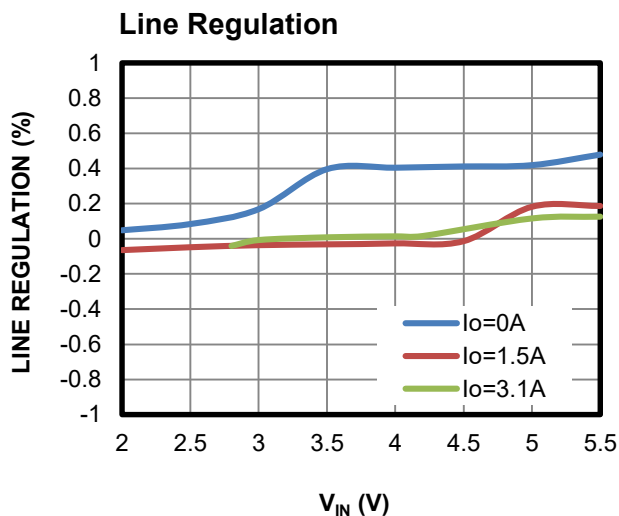
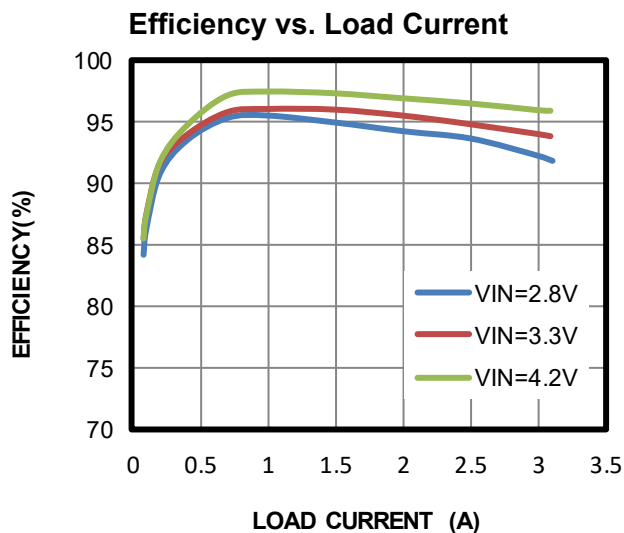
Figure 1: Evaluation Board Schematic

EVL3424A-G-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	C1A, C1B, C2B, C2C	22 μ F	Ceramic capacitor, 16V, X7R	1210	Murata	GRM32ER71C226KEA8L
1	C2A	1 μ F	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KE15D
1	C3	10nF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C103KA01D
1	L1	1.5 μ H	Inductor, RDC = 9.7m Ω , I _{SAT} = 12.5A	SMD	MPS	MPL-AL5030-1R5
1	R1	1M Ω	Film resolution, 1%	0603	Yageo	RC0603FR-071ML
1	R2	191k Ω	Film resolution, 1%	0603	Yageo	RC0603FR-07191KL
2	R3, R6	100k Ω	Film resolution, 1%	0603	Yageo	RL0603FR-07100KL
1	R4	2k Ω	Film resolution, 1%	0603	Yageo	RC0603FR-072KL
1	R5A	16m Ω	Film resolution, 1%	0603	Yageo	RL0603FR-070R016L
1	R5B	18m Ω	Film resolution, 1%	0603	Yageo	RL0603FR-070R018L
1	U1	MP3424A	Synchronous, step-up converter with output disconnect	QFN (2mmx 2mm)	MPS	MP3424AGG

EVB TEST RESULTS

$V_{IN} = 3.3V$, $V_{OUT} = 5V$, $L = 1.5\mu H$, $T_A = 25^\circ C$, unless otherwise noted.



EVB TEST RESULTS *(continued)*

$V_{IN} = 3.3V$, $V_{OUT} = 5V$, $L = 1.5\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

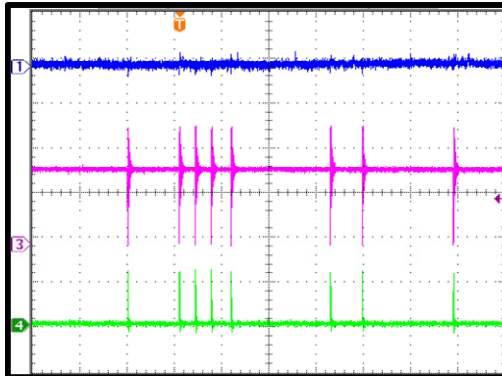
Output Voltage Ripple

Load = 0A

CH1:
 V_{OUT}/AC
10mV/div.

CH3: V_{SW}
2V/div.

CH4: I_L
200mA/div.



20µs/div.

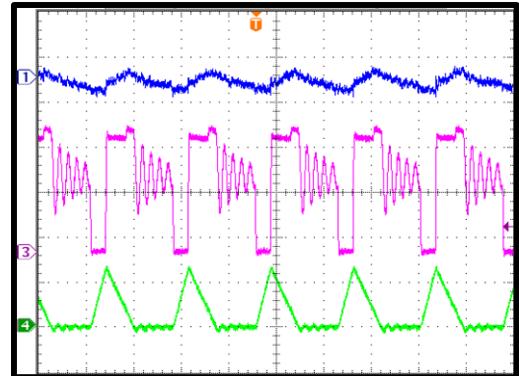
Output Voltage Ripple

Load = 0.1A

CH1:
 V_{OUT}/AC
10mV/div.

CH3: V_{SW}
2V/div.

CH4: I_L
500mA/div.



1µs/div.

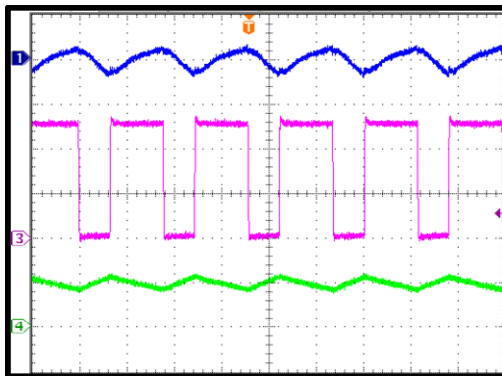
Output Voltage Ripple

Load = 3.1A

CH1:
 V_{OUT}/AC
100mV/div.

CH3: V_{SW}
2V/div.

CH4: I_L
5A/div.



1µs/div.

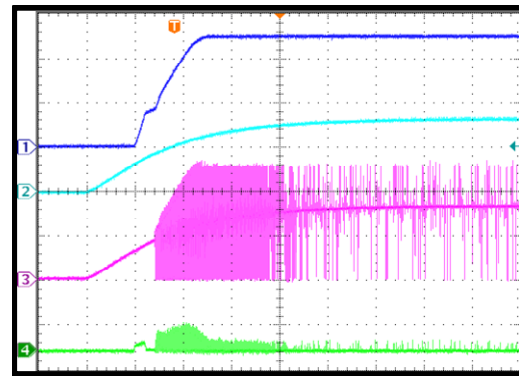
Start-Up through VIN

Load = 0A

CH1: V_{OUT}
2V/div.
CH2: V_{IN}
2V/div.

CH3: V_{SW}
2V/div.

CH4: I_L
1A/div.



2ms/div.

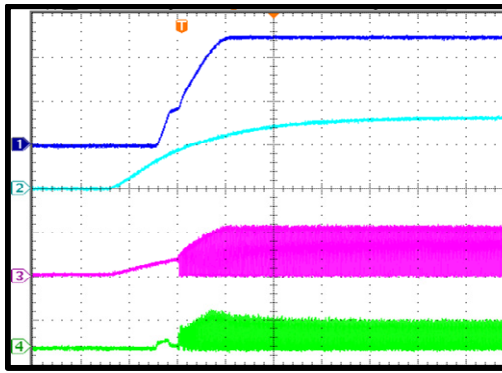
Start-Up through VIN

Load = 0.1A

CH1: V_{OUT}
2V/div.
CH2: V_{IN}
2V/div.

CH3: V_{SW}
5V/div.

CH4: I_L
5A/div.



2ms/div.

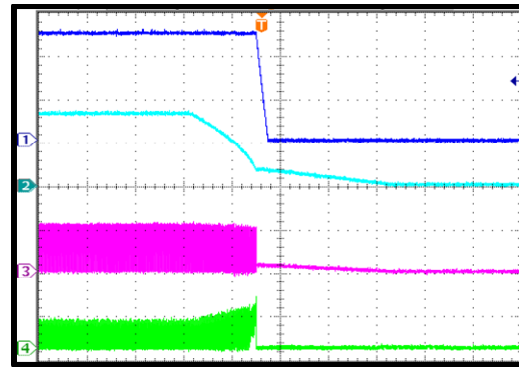
Shutdown through VIN

Load = 0.1A

CH1: V_{OUT}
2V/div.
CH2: V_{IN}
2V/div.

CH3: V_{SW}
5V/div.

CH4: I_L
1A/div.



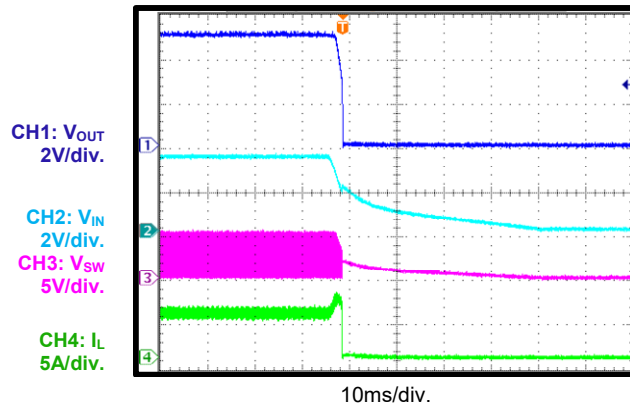
10ms/div.

EVB TEST RESULTS *(continued)*

$V_{IN} = 3.3V$, $V_{OUT} = 5V$, $L = 1.5\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

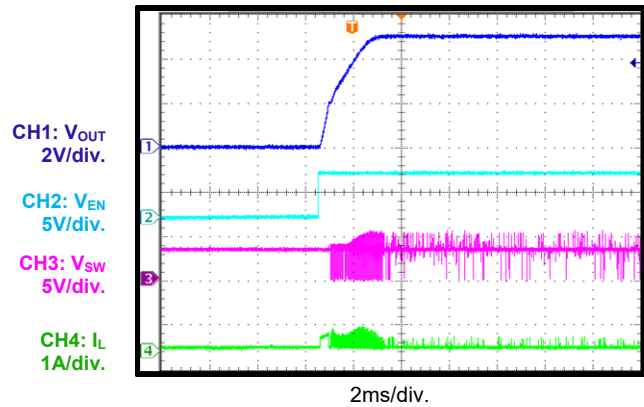
Shutdown through VIN

Load = 3.1A



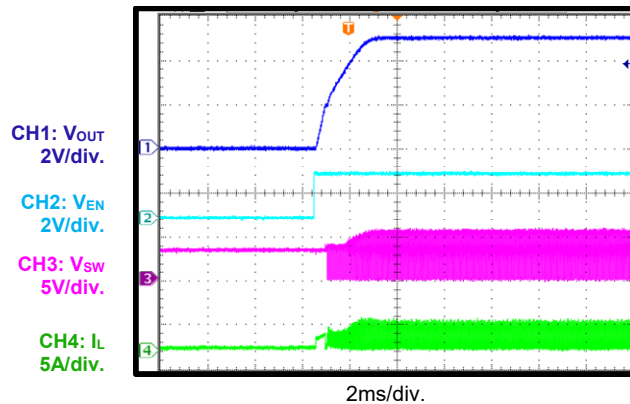
Start-Up through EN

Load = 0A



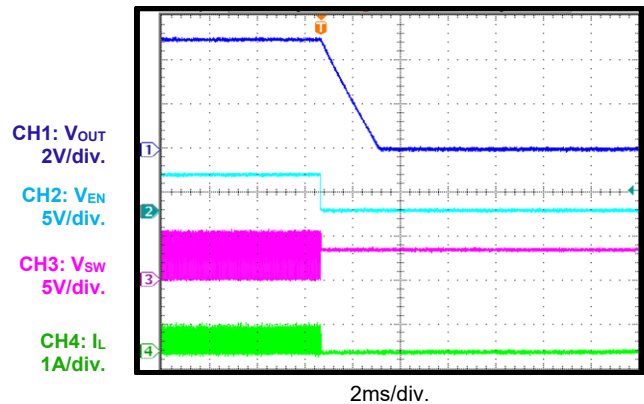
Start-Up through EN

Load = 0.1A



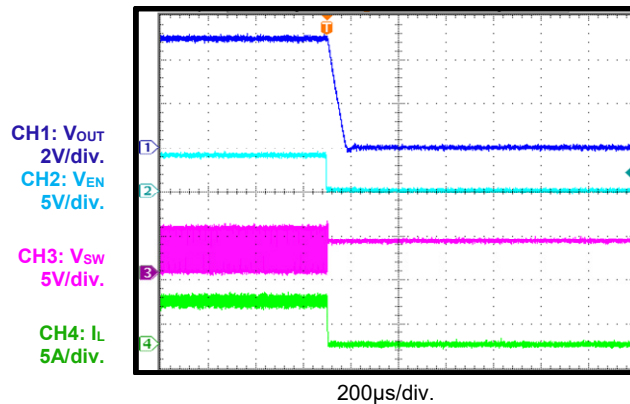
Shutdown through EN

Load = 0.1A



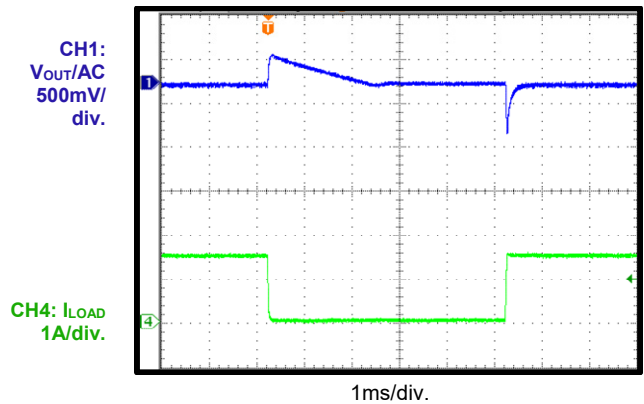
Shutdown through EN

Load = 3.1A



Load Transient

$I_{LOAD} = 0A$ to $1.5A$ at $150mA/\mu s$

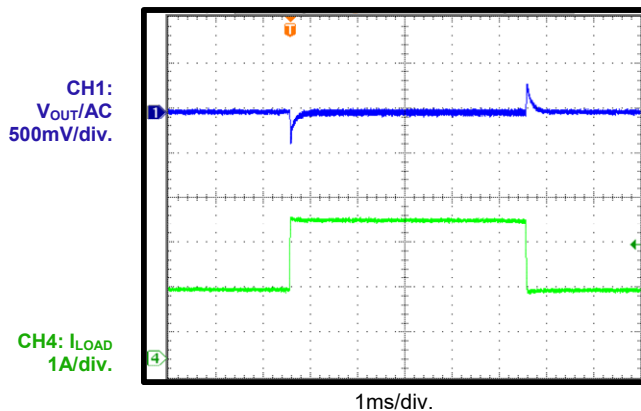


EVB TEST RESULTS (continued)

$V_{IN} = 3.3V$, $V_{OUT} = 5V$, $L = 1.5\mu H$, $T_A = 25^{\circ}C$, unless otherwise noted.

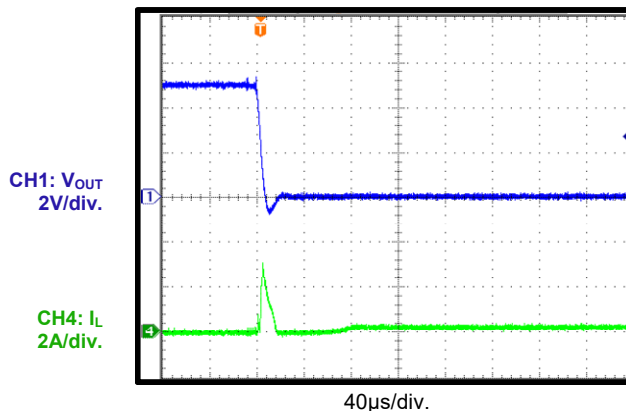
Load Transient

$I_{LOAD} = 1.5A$ to $3.1A$ at $150mA/\mu s$



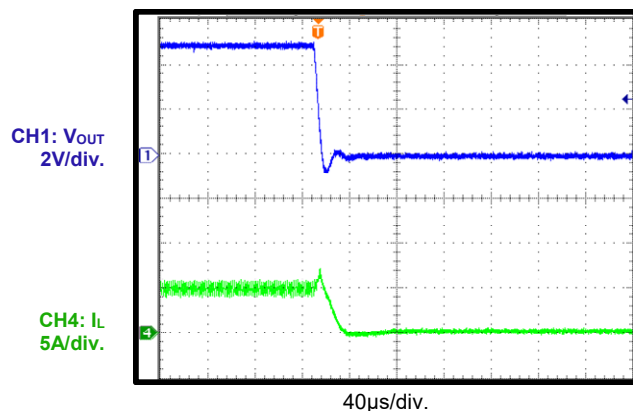
SCP Entry

0A load to short



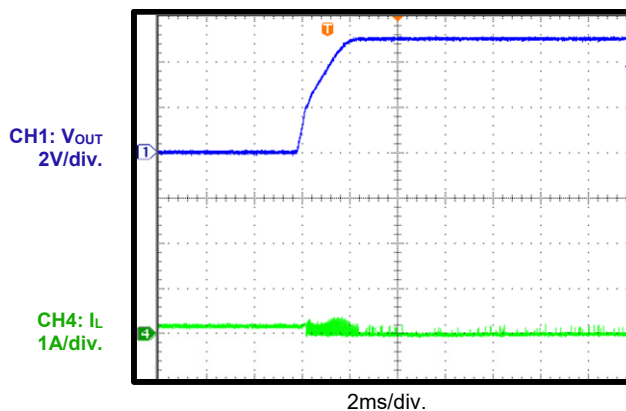
SCP Entry

3.1A load to short



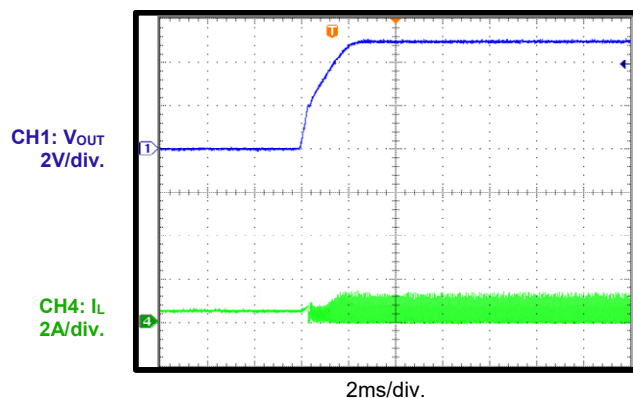
SCP Recovery

Recover to 0A load



SCP Recovery

Recover to 0.1A load



PCB LAYOUT

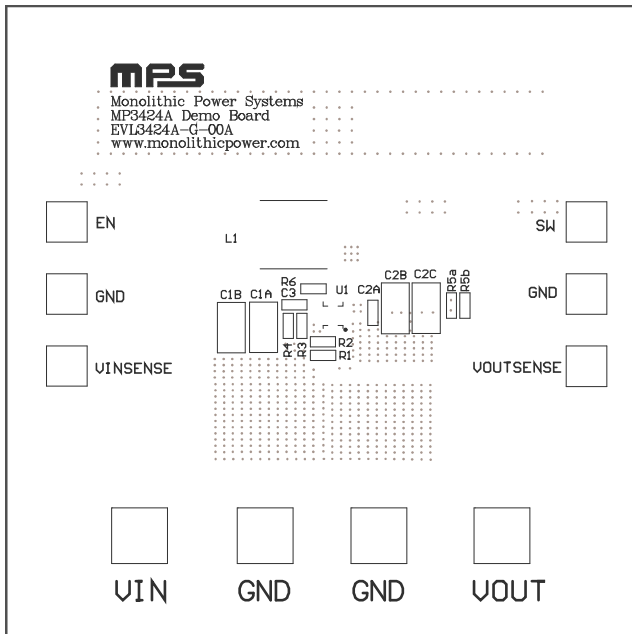


Figure 2: Top Silk

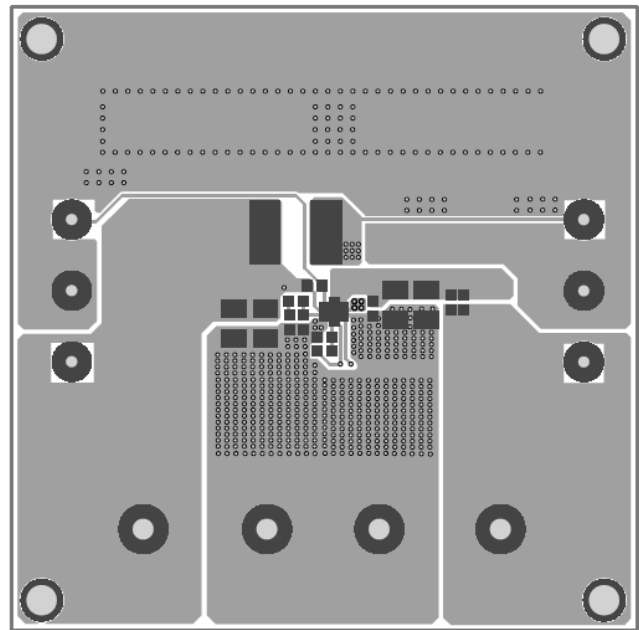


Figure 3: Top Layer

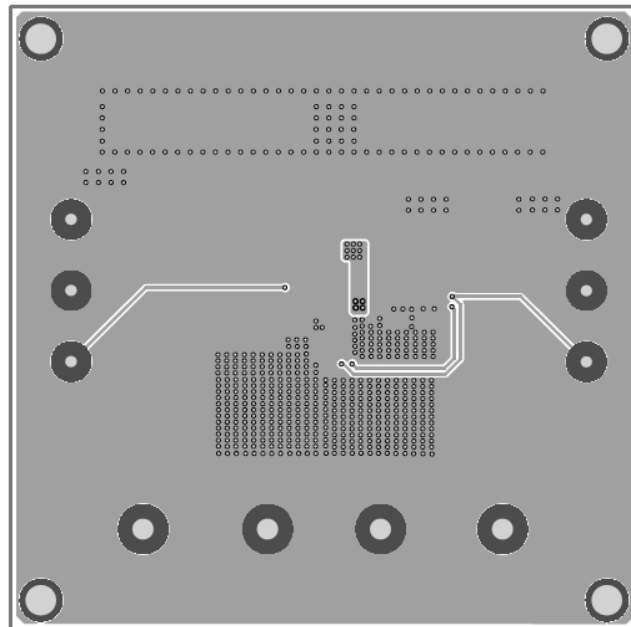


Figure 4: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/01/2021	Initial Release	-

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