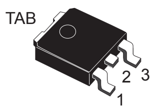
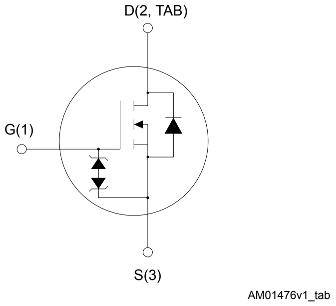
STD80N240K6

Datasheet

N-channel 800 V, 197 mΩ typ., 16 A MDmesh K6 Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD80N240K6	800 V	220 mΩ	16 A

- Worldwide best $R_{DS(on)}$ x area
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Flyback converter
- Adapters for tablets, notebook and AIO
- LED Lighting

Description

This very high voltage N-channel Power MOSFET is designed using the ultimate MDmesh K6 technology based on 20 years STMicroelectronics experience on super junction technology. The result is the best-in-class on-resistance per area and gate charge for applications requiring superior power density and high efficiency.

Product status link
STD80N240K6

Product summary	
Order code	STD80N240K6
Marking	80N240K6
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	16	A
I_D	Drain current (continuous) at T_C = 100 °C	10	A
I_{DM} (1)	Drain current (pulsed)	35	A
P_{TOT}	Total power dissipation at T_C = 25 °C	105	W
dv/dt (2)	Peak diode recovery voltage slope	5	V/ns
dv/dt (2)	Peak diode recovery current slope	100	A/µs
dv/dt (3)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 4 A; V_{DS} (peak) = 400 V*
3. *V_{DS} ≤ 640 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.19	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	50	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	3.3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C[(1)]			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±1	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.5	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		197	220	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	1350	-	pF
C_{oss}	Output capacitance		-	20	-	pF
$C_{o(er)}$ [(1)]	Equivalent capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	139	-	pF
$C_{o(tr)}$ [(2)]	Equivalent capacitance energy related		-	25	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D= 0 A	-	1.8	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 7 A, V_{GS}= 0 to 10 V (see Figure 19. Test circuit for gate charge behavior)	-	25.9	-	nC
Q_{gs}	Gate-source charge		-	6.9	-	nC
Q_{gd}	Gate-drain charge		-	8.4	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D =7 A, R_G = 4.7 Ω V_{GS} = 10 V see (Figure 17. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	47.8	-	ns
t_f	Fall time		-	12	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM} (1)	Source-drain current (pulsed)		-		35	A
V_{SD} (2)	Forward on voltage	I_{SD} = 14 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	335		ns
Q_{rr}	Reverse recovery charge		-	5.4		µC
I_{RRM}	Reverse recovery current		-	27.5		A
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	430		ns
Q_{rr}	Reverse recovery charge		-	7.4		µC
I_{RRM}	Reverse recovery current		-	28		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

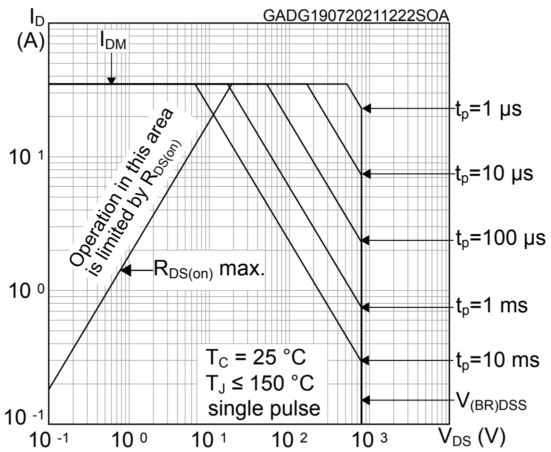


Figure 2. Maximum transient thermal impedance

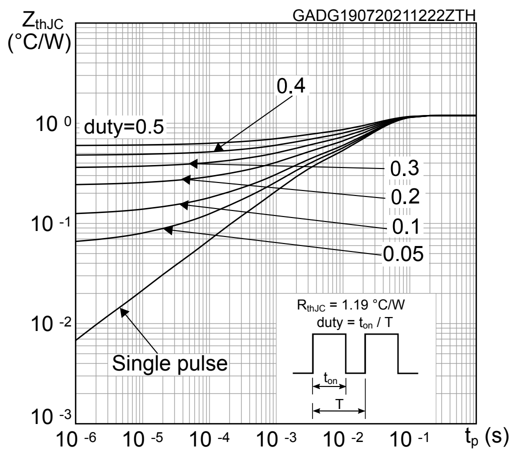


Figure 3. Typical output characteristics

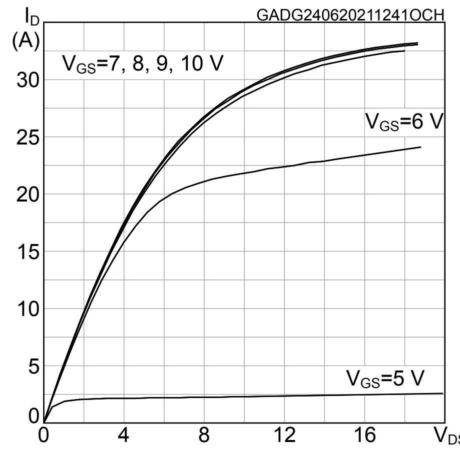


Figure 4. Typical transfer characteristics

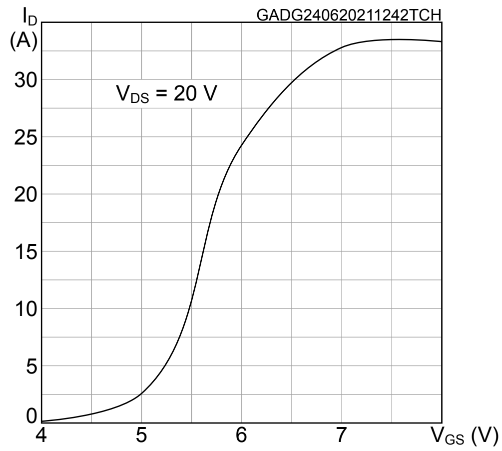


Figure 5. Typical gate charge characteristics

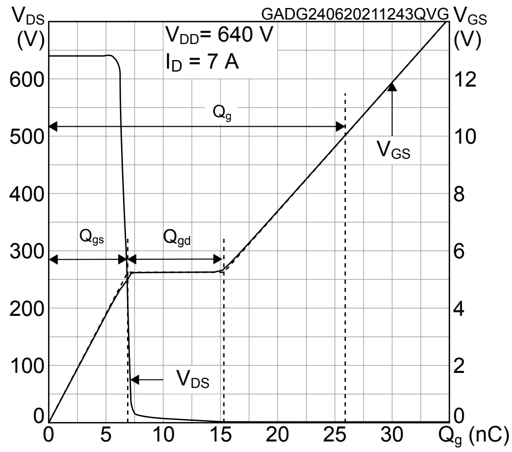


Figure 6. Typical drain-source on-resistance

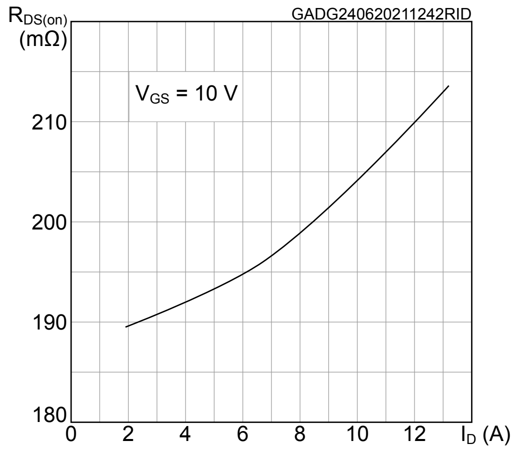


Figure 7. Typical capacitance characteristics

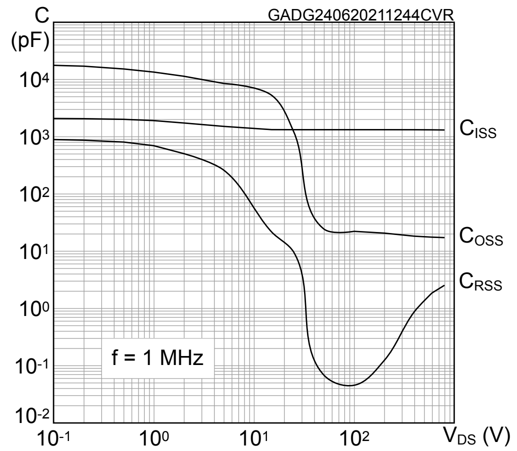


Figure 8. Typical output capacitance stored energy

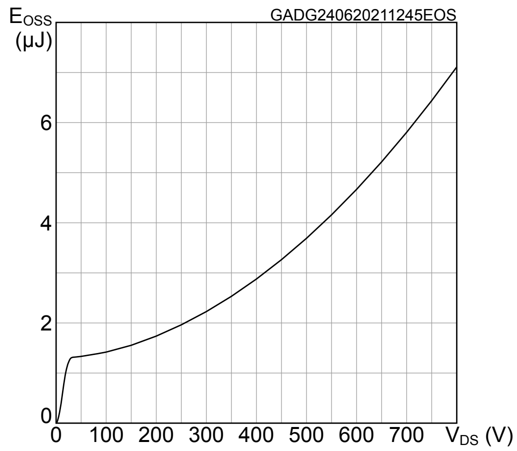


Figure 9. Normalized gate threshold vs temperature

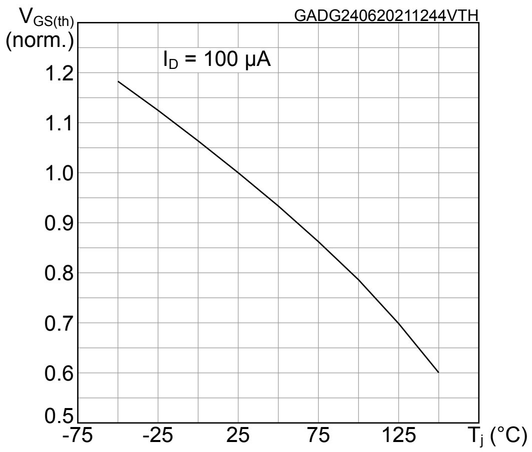


Figure 10. Normalized on-resistance vs temperature

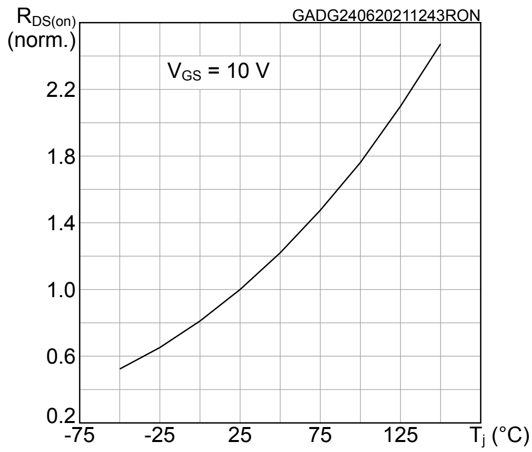


Figure 11. Normalized breakdown voltage vs temperature

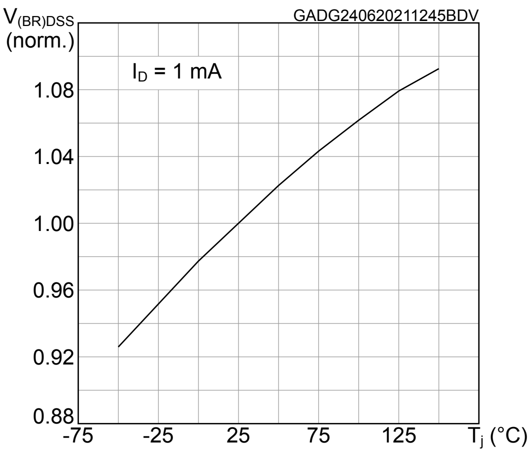


Figure 12. Typical reverse diode forward characteristics

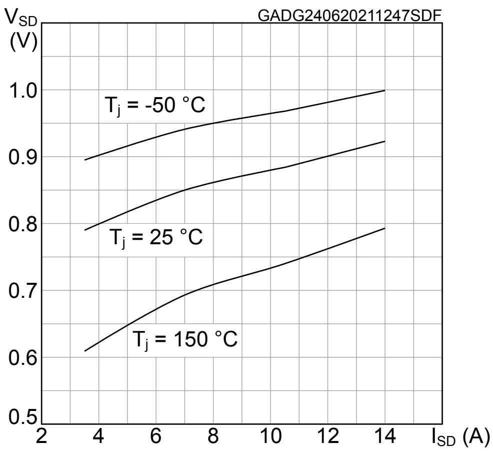


Figure 13. Maximum avalanche energy vs temperature

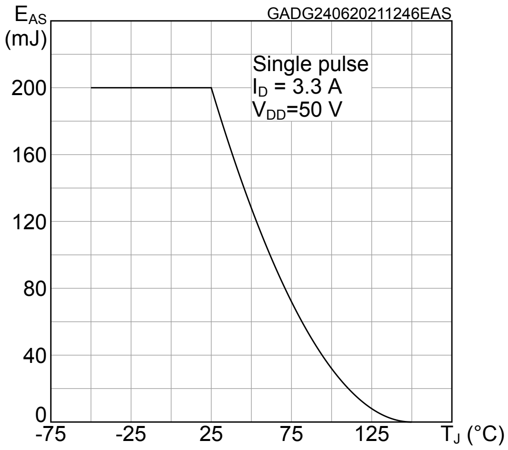


Figure 14. Typical output capacitance stored energy

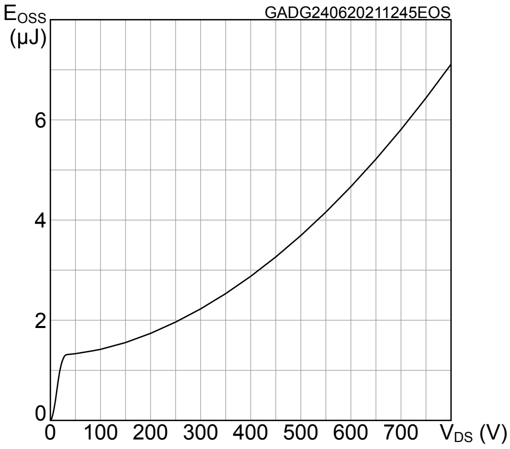


Figure 15. Typical inductive load switching energy vs I_D

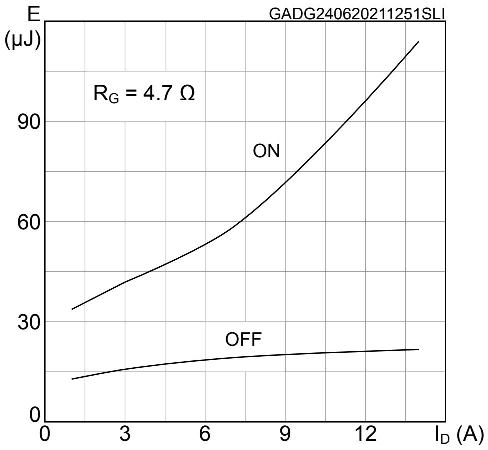
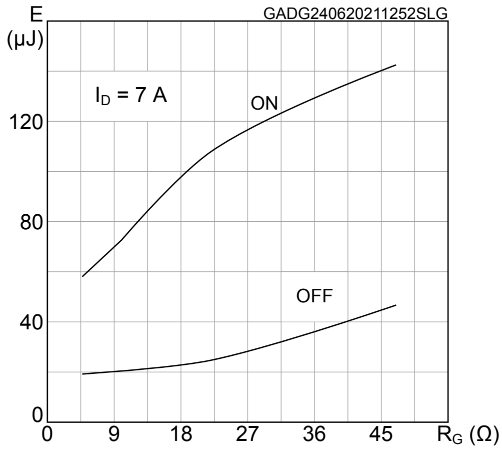


Figure 16. Typical inductive load switching energy vs Rg



3 Test circuits

Figure 17. Test circuit for resistive load switching times

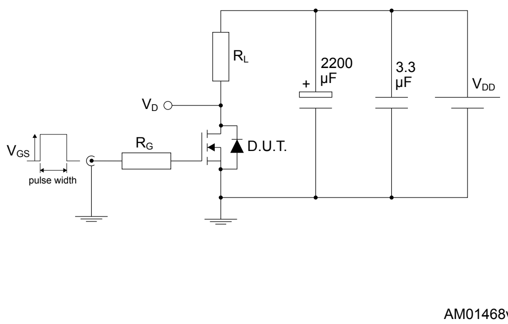


Figure 18. Switching time waveform

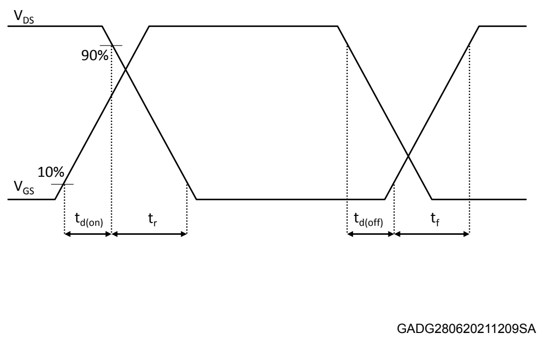


Figure 19. Test circuit for gate charge behavior

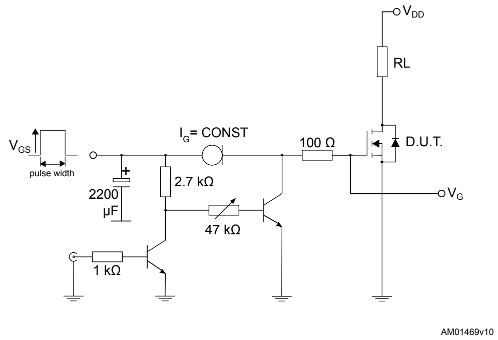


Figure 20. Test circuit for inductive load switching and diode recovery times

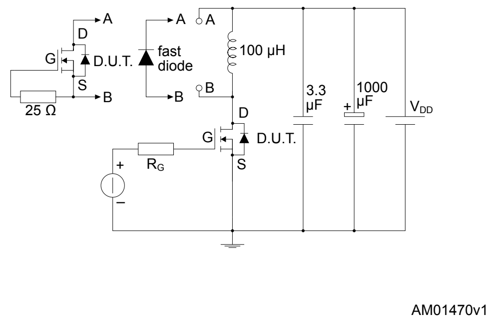


Figure 21. Unclamped inductive load test circuit

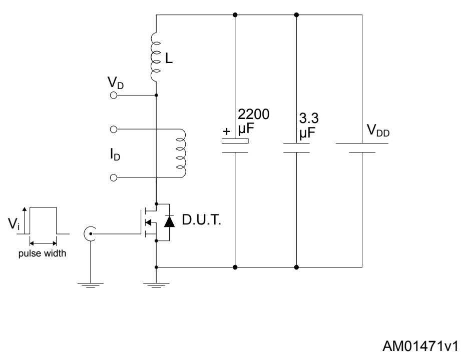
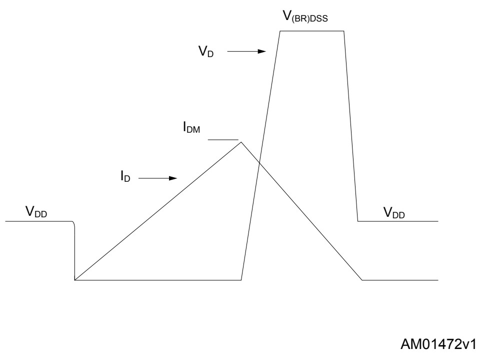


Figure 22. Unclamped inductive waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 23. DPAK (TO-252) type A2 package outline

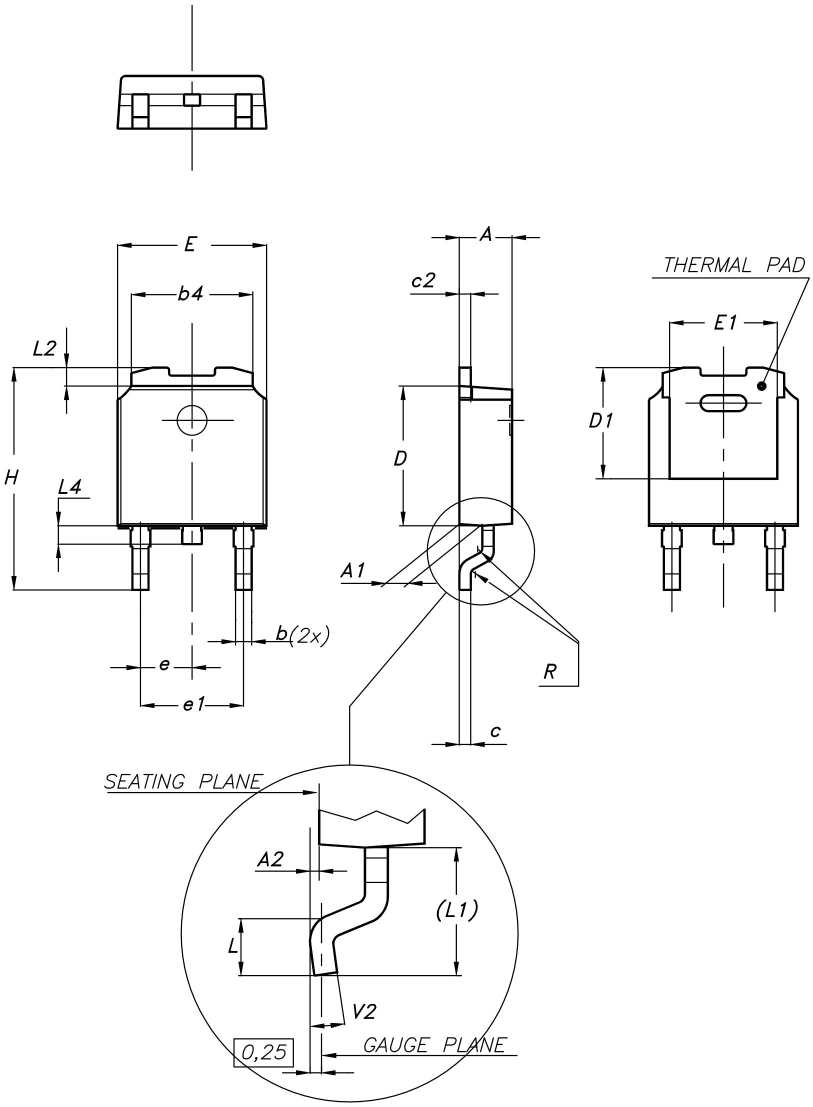


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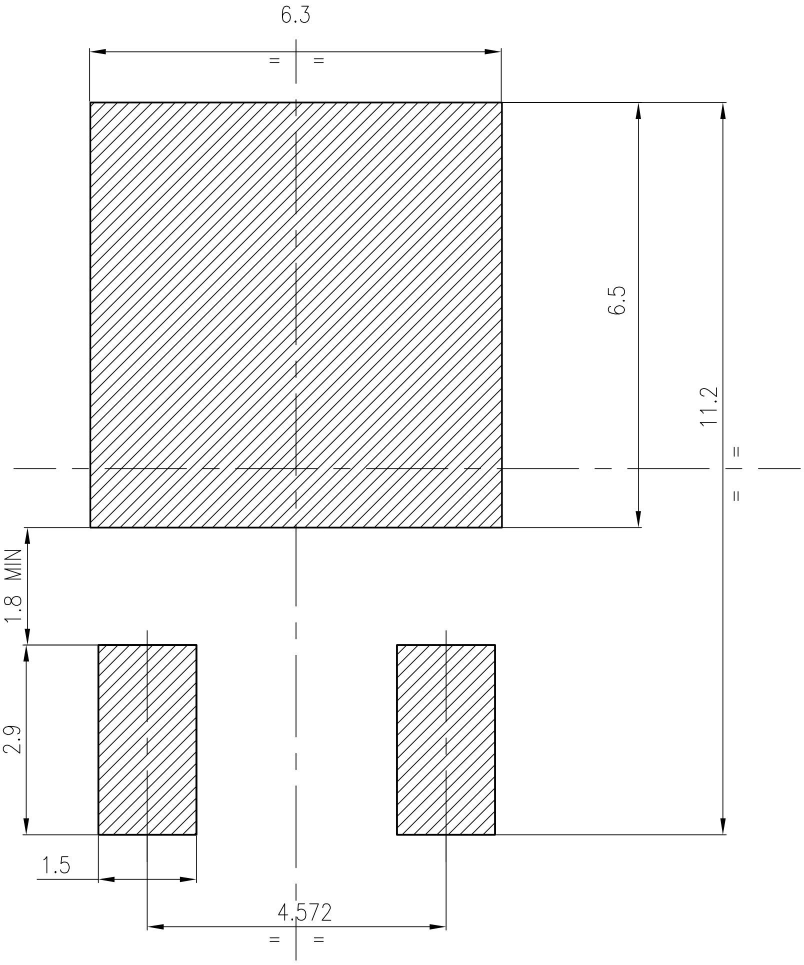
Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



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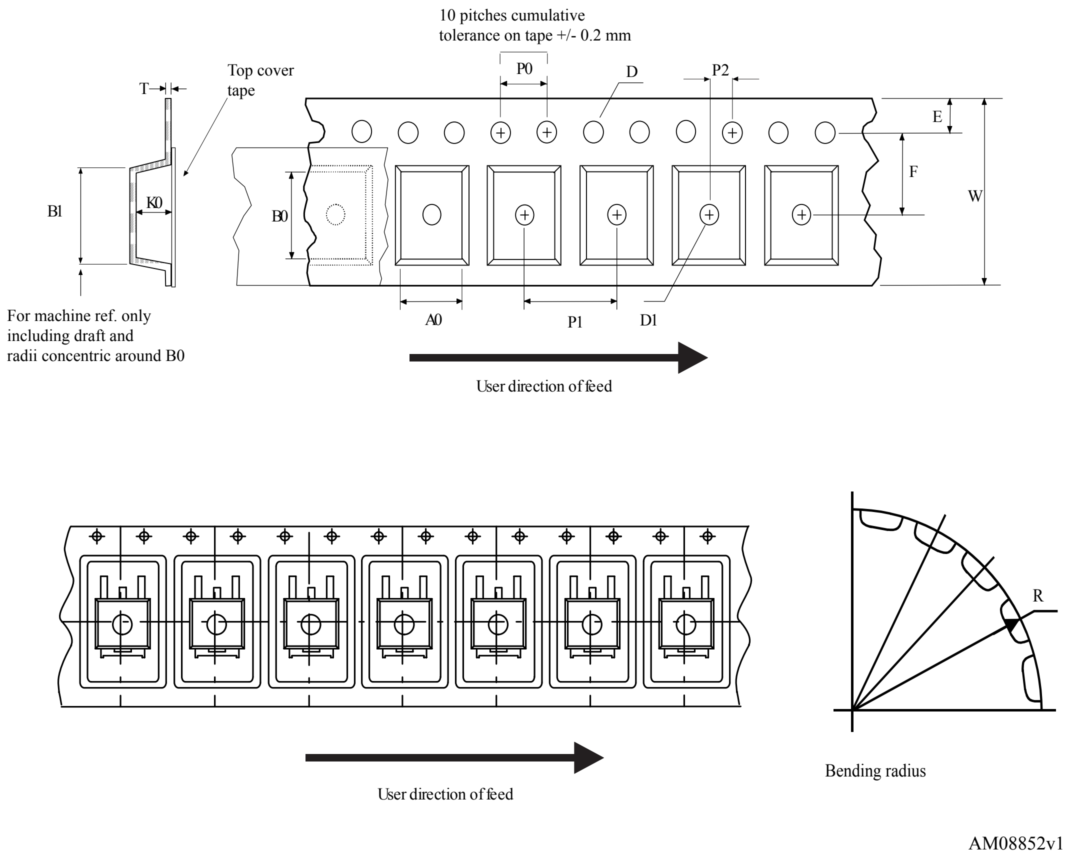
4.2 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline



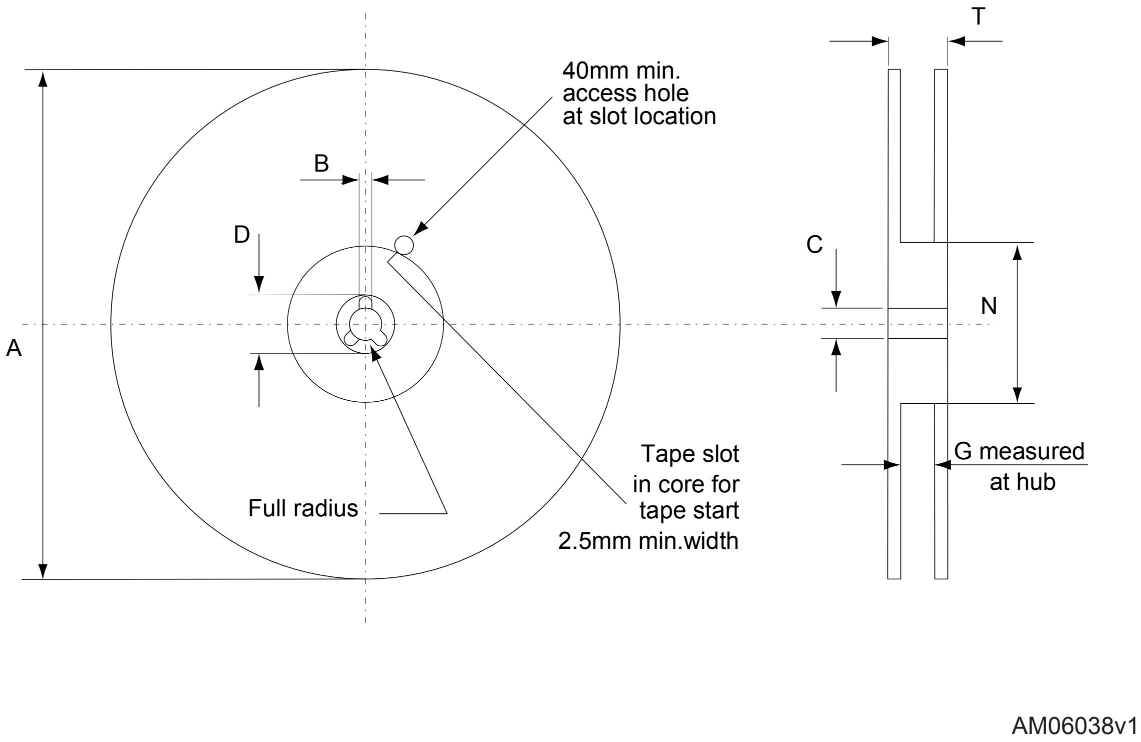


Figure 26. DPAK (TO-252) reel outline

Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Jul-2021	1	First release.
17-Feb-2022	2	Updated Section Applications on cover page. Updated Table 5. Dynamic. Updated Figure 15. Typical inductive load switching energy vs I_D. Updated Figure 16. Typical inductive load switching energy vs Rg. Minor text changes.

Contents