Product Change Notification / SYST-06AUDA206

Date:

10-May-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATtiny3216/3217 Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

SYST-06AUDA206_Affected_CPN_05102022.pdf
SYST-06AUDA206_Affected_CPN_05102022.csv

Notification Text:

SYST-06AUDA206

Microchip has released a new Product Documents for the ATtiny3216/3217 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny3216/3217 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
Updated errata:
1) Device: 2.2.1. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values
Added errata:
1) CCL: 2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT
2) NVMCTRL: 2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register
3) TCA: 2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode
4) TCB: 2.8.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode
5) TCD:
- 2.9.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used
- 2.9.2. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used
6) USART
- 2.10.4. Full Range Duty Cycle Not Supported When Validating LIN Sync Field
- 2.10.5. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode
- 2.10.6. Receiver Non-Functional after Detection of Inconsistent Synchronization Field

Added data sheet clarifications:
1) Memories: 3.1.1. Fuses - Factory Default Values
2) SLPCTRL: 3.2.1. Sleep Mode Activity Overview
3) USART: 3.3.1. TXDATA Buffer

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 10 May 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny3216/3217 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY3216-SF
ATTINY3216-SFR
ATTINY3216-SN
ATTINY3216-SNR
ATTINY3217-MF
ATTINY3217-MFR
ATTINY3217-MN
ATTINY3217-MNR

ATtiny3216/3217

Silicon Errata and Data Sheet Clarifications

The ATtiny3216/3217 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002205), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny3216/3217 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002205) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A	Rev. C
Device	2.2.1. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X
ADC	2.3.2. ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X
	2.3.3. ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X	X
	2.3.4. One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X
CCL	2.4.1. Connecting LUTs in Linked Mode Requires OUTEN Set to ‘1’	X	-
	2.4.2. D-latch is Not Functional	X	-
	2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
NVMCTRL	2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X	X
RTC	2.6.2. Disabling the RTC Stops the PIT	X	-
TCA	2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.8.1. Minimum Event Duration Must Exceed the Selected Clock Period	X	X
	2.8.2. The TCA Restart Command Does Not Force a Restart of TCB	X	X
	2.8.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.9.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X	X
	2.9.2. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is ‘0’ or Dual Slope Mode is Used	X	X
USART	2.10.1. TXD Pin Override Not Released When Disabling the Transmitter	X	X
	2.10.2. Frame Error on a Previous Message May Cause False Start Bit Detection	X	-
	2.10.3. Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X
	2.10.4. Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	-
	2.10.5. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	-	X
	2.10.6. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	-	X

The following silicon revision was never released to production: **Rev. B**

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when using the OSC20M oscillator as the Main Clock source.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.3 ADC - Analog-to-Digital Converter

2.3.1 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.3.2 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. A	Rev. C

X	X

2.3.3 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and V_{DD} < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for V_{DD} < 2.7V.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.3.4 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around
Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around
None

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the reset value of NVMCTRL.CTRLA will not be '0x00'. Even reserved bits can be read as '1' after Reset.

Work Around
Ignore the initial value.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.6 RTC - Real-Time Counter

2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.6.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around
Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.7 TCA - Timer/Counter A

2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.8 TCB - Timer/Counter B

2.8.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement*.

Work Around
Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.8.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.8.3 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.9 TCD - Timer/Counter D

2.9.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When configuring the TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0' events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.9.2 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around
Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from '0' and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around
There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.10.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around
Wait for the RXD pin to go high before reading RXDATA by, for instance, polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.10.3 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A	Rev. C
X	X

2.10.4 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART validates each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around
None.

Affected Silicon Revisions

Rev. A	Rev. C
X	-

2.10.5 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A	Rev. C
-	X

2.10.6 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set.

The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud mode (GENAUTO) or LIN Constrained Auto-Baud mode (LINAUTO), and the received synchronization frame does not conform to the conditions as described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A	Rev. C
-	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002205).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Memories

3.1.1 Fuses - Factory Default Values

A clarification has been made for the *Fuse Description* section concerning the fuse default values. The data sheet refers to these values as reset values when they should have been given as factory-programmed values. Also, they are given in both hexadecimal and binary values, which contradicts each other.

The following sentence has been added to each sub-section of the *Fuse Description* section.

The default value given in this fuse description is the factory-programmed value and should not be mistaken for the Reset value.

The table below lists the reset values given by the data sheet and the actual factory-programmed default values.

Fuse	Stated Reset Value in Data Sheet		Actual Factory Default on Device	
	Hexadecimal	Binary	Hexadecimal	Binary
WDTCFG	-	`b00000000	**0x00**	**`b00000000**
BODCFG	-	`b00000000	**0x00**	**`b00000000**
OSCCFG	-	`b0XXXXX10	**0x02**	**`b00000010**
TCD0CFG	-	`b00000000	**0x00**	**`b00000000**
SYSCFG0	0xC4	`b11X101X0	**0xF6**	**`b11110110**
SYSCFG1	-	`bXXXXX111	**0x07**	**`b00000111**
APPEND	-	`b00000000	**0x00**	**`b00000000**
BOOTEND	-	`b00000000	**0x00**	**`b00000000**
LOCKBIT	-	`b00000000	**0xC5**	**`b11000101**

3.2 SLPCTRL - Sleep Controller

3.2.1 Sleep Mode Activity Overview

A clarification has been made to Table 11-1 *Sleep Mode Activity Overview*, where the single table has been split into three separate tables for clarity. Functional changes are shown in **bold**.

Table 3-1. Sleep Mode Activity Overview for Peripherals

Peripheral	Active in Sleep Mode		
	Idle	Standby	Power-Down
CPU	-	-	-
RTC	X	X(1)	X(2)
WDT	X	X	X
BOD	X	X	X

.....continued			
Peripheral	**Active in Sleep Mode**		
	Idle	**Standby**	**Power-Down**
EVSYS	**X**	**X**	**X**
CCL	X	X(1)	-
ACn			
ADCn/PTC			
TCBn			
All other peripherals	X	-	-

Notes:
1. Set the RUNSTBY bit of the corresponding peripheral to enter the active state.
2. PIT only.

Table 3-2. Sleep Mode Activity Overview for Clock Sources

Clock Source	**Active in Sleep Mode**		
	Idle	**Standby**	**Power-Down**
Main clock source	X	X(1)	-
RTC clock source	X	X(1)	X(2)
WDT oscillator	X	X	X
BOD oscillator(3)	**X**	**X**	**X**
CCL clock source	**X**	**X(1)**	-

Notes:
1. Set the RUNSTBY bit of the corresponding peripheral to enter the active state.
2. PIT only.
3. **The BOD oscillator runs only in Sampled mode.**

Table 3-3. Sleep Mode Wake-Up Sources

Wake-Up Sources	**Active in Sleep Mode**		
	Idle	**Standby**	**Power-Down**
PORT Pin Interrupt	X	X	X(1)
BOD VLM interrupt	**X**	**X**	**X**
RTC interrupts	X	X(2)	X(3)
TWIn Address Match interrupt	X	X	X
USARTn Start-of-Frame interrupt	-	X	-
TCBn interrupts	**X**	**X(2)**	**-**
ADCn/PTC interrupts	X	X(2)	-
ACn interrupts	**X**	**X(4)**	-
All other interrupts	X	-	-

Notes:

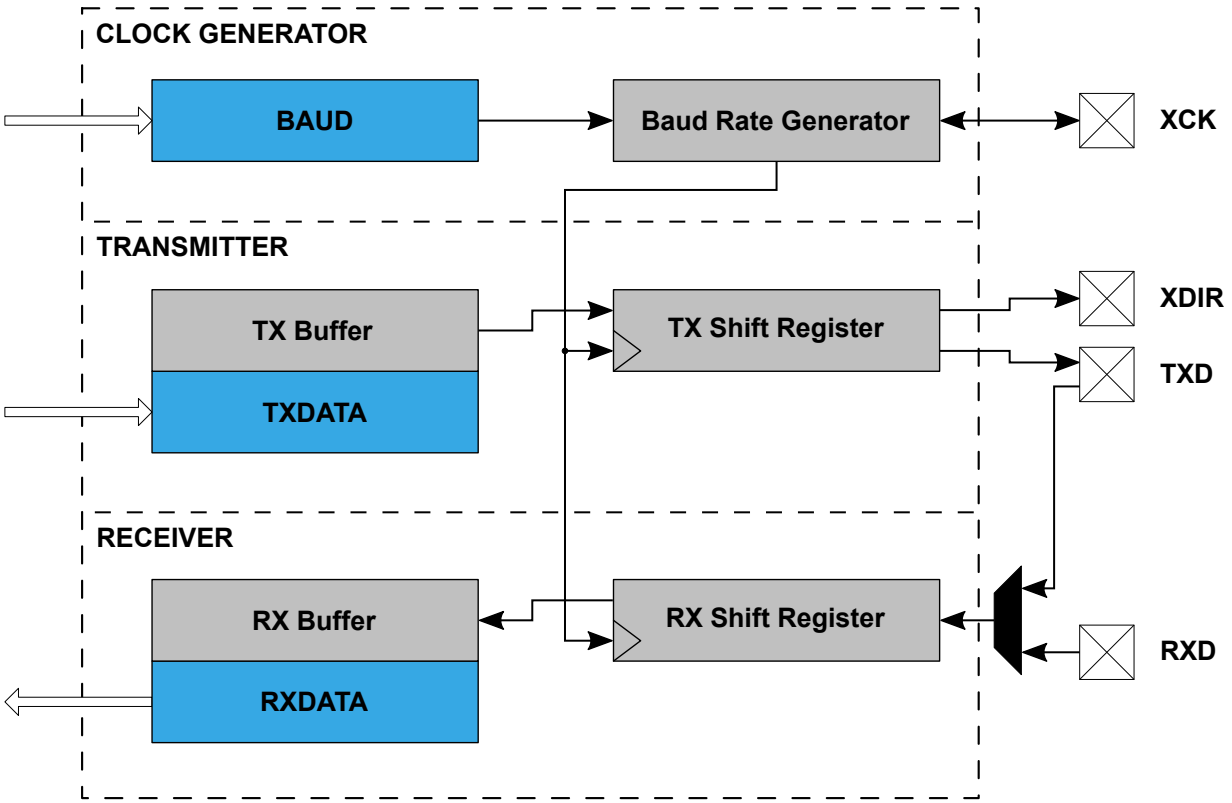
1. **Configure the I/O pin according to *Asynchronous Sensing Pin Properties* in the PORT section.**
2. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
3. PIT only.
4. **When the RUNSTDBY bit is set, the AC will operate without updating its Status register or triggering interrupts. If another peripheral has requested CLK_PER, the AC will use the clock to update the Status register and trigger interrupts.**

3.3 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

3.3.1 TXDATA Buffer

The block diagram is missing that USART TX is double-buffered from Figure 25-1 in the data sheet. The figure below shows the added **TX Buffer**.

Figure 3-1. Block Diagram



The following text is changed in the *Overview* section:

The transmitter consists of a **two-level** write buffer.

The following text is changed in the *Data Transmission* section:

The data transmission is initiated by loading the **Transmit Data (USARTn.TXDATAL and USARTn.TXDATAH)** registers with the data to be sent. The data in the **Transmit Data registers are moved to the TX Buffer** once emptied and then to the Shift register once it is empty and ready to send a new frame.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
B	05/2022	Updated errata: • Device: 2.2.1. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values Added errata: • CCL: 2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT • NVMCTRL: 2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register • TCA: 2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode • TCB: 2.8.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode • TCD: – 2.9.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used – 2.9.2. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used • USART – 2.10.4. Full Range Duty Cycle Not Supported When Validating LIN Sync Field – 2.10.5. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode – 2.10.6. Receiver Non-Functional after Detection of Inconsistent Synchronization Field Added data sheet clarifications: • Memories: 3.1.1. Fuses - Factory Default Values • SLPCTRL: 3.2.1. Sleep Mode Activity Overview • USART: 3.3.1. TXDATA Buffer

.....continued

Doc Rev.	Date	Comments
A	05/2020	• Initial document release The content of the document has been restructured from: • ATtiny1614 Silicon Errata and Data Sheet Clarification • ATtiny1616/3216 Silicon Errata and Data Sheet Clarification • ATtiny1617/3217 Silicon Errata and Data Sheet Clarification to: • ATtiny1614/1616/1617 Silicon Errata and Data Sheet Clarification • **ATtiny3216/3217 Silicon Errata and Data Sheet Clarification (this document)** Refer to 4.2. Appendix - Obsolete Revision History for further details. The following items are referring to changes between the latest revisions of the obsolete documents and this document: • Added erratas: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – USART: *Open-Drain Mode Does Not Work When TXD is Configured as Output* • Removed erratas not applicable for ATtiny3216/3217 – AC • *AC Interrupt Flag Not Set Unless Interrupt is Enabled* • *False Triggers May Occur Under Certain Conditions* • *False Triggering When Sweeping Negative Input of the AC When the Low-Power Mode is Disabled* – ADC • *SAMPDLY and ASDV Does Not Work Together With SAMPLEN* • *ADC Interrupt Flags Cleared When Reading RESH* • *Changing ADC Control Bits During Free-Running Mode not Working* • *Changing ADC Control Bits During Free-Running Mode not Working* • *ADC Wake-Up with WCOMP* – TCB • *The TCB Interrupt Flag is Cleared When Reading CCMPH* • *TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock* – TCD • *TCD Event Output Lines May Give False Events* • *TCD Auto-Update Not Working* – TWI • *TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible* • *TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit* • *TWI Smart Mode Gives Extra Clock Pulse* • *The TWI Master Enable Quick Command is Not Accessible* – USART • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • Removed data sheet clarifications, as the corresponding data sheet has been updated with correct information

4.2 Appendix - Obsolete Revision History

Notes: Due to document structure change from pin organized documents, the following obsolete document revision history is provided as reference.

- ATtiny1616/3216 Silicon Errata and Data Sheet Clarification (DS40002120B)
- ATtiny1617/3217 Silicon Errata and Data Sheet Clarification (DS40002121B)

4.2.1 Obsolete Document DS40002120

Doc Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarifications to ADC, AC and PTC electrical characteristics
A	06/2019	• Initial document release

4.2.2 Obsolete Document DS40002121

Doc Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten • Added clarifications to ADC, AC and PTC electrical characteristics
A	06/2019	• Initial document release

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