DAQ S Series

S Series User Manual

NI 6110/6111/6115/6120/6122/6123/6132/6133/6143 Simultaneous Multifunction Input/Output Devices

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About This Manual

The *S Series User Manual* contains information about using the National Instruments S Series data acquisition (DAQ) devices with NI-DAQmx 8.8 and later.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 This icon denotes a note, which alerts you to important information.

 This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Read Me First: Safety and Electromagnetic Compatibility* document for information about precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

Platform — Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

Related Documentation

Each application software package and driver includes information about writing applications for taking measurements and controlling measurement devices. The following references to documents assume you have NI-DAQmx 8.8 or later, and where applicable, version 7.1 or later of the NI application software.

NI-DAQmx for Windows

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx for Windows software, how to install your NI-DAQmx-supported DAQ device, and how to confirm that your device is operating properly. Select **Start»All Programs»National Instruments»NI-DAQ»DAQ Getting Started Guide**.

The *NI-DAQ Readme* lists which devices are supported by this version of NI-DAQ. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQ Readme**.

The *NI-DAQmx Help* contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs» National Instruments»NI-DAQ»NI-DAQmx Help**.

NI-DAQmx for Linux

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx-supported DAQ device and confirm that your device is operating properly.

The *NI-DAQ Readme for Linux* lists supported devices and includes software installation instructions, frequently asked questions, and known issues.

The *C Function Reference Help* describes functions and attributes.

The *NI-DAQmx for Linux Configuration Guide* provides configuration instructions, templates, and instructions for using test panels.

Note All NI-DAQmx documentation for Linux is installed at `/usr/local/natinst/nidaqmx/docs`.

NI-DAQmx Base (Linux/Mac OS X)

(NI 611*x*/6120/6143 Only) The *NI-DAQmx Base Getting Started Guide* describes how to install your NI-DAQmx Base software, your NI-DAQmx Base-supported DAQ device, and how to confirm that your device is operating properly. In Windows, select **Start»All Programs»National Instruments»NI-DAQmx Base»Documentation»Getting Started Guide**.

Getting Started with NI-DAQmx Base for Linux and Mac Users describes how to install your NI-DAQmx Base software, your NI-DAQmx Base-supported DAQ device, and how to confirm that your device is operating properly on your Mac/Linux machine.

The *NI-DAQmx Base Readme* lists which devices are supported by this version of NI-DAQmx Base. In Windows, select **Start»All Programs» National Instruments»NI-DAQmx Base»DAQmx Base Readme**.

The *NI-DAQmx Base VI Reference Help* contains VI reference and general information about measurement concepts. In LabVIEW, select **Help» NI-DAQmx Base VI Reference Help**.

The *NI-DAQmx Base C Reference Help* contains C reference and general information about measurement concepts. In Windows, select **Start»All Programs»National Instruments»NI-DAQmx Base»Documentation» C Function Reference Help**.

Note All NI-DAQmx Base documentation for Linux is installed at `/usr/local/natinst/nidaqmxbase/documentation`.

Note All NI-DAQmx Base documentation for Mac OS X is installed at `/Applications/National Instruments/NI-DAQmx Base/documentation`.

LabVIEW

If you are a new user, use the *Getting Started with LabVIEW* manual to familiarize yourself with the LabVIEW graphical programming environment and the basic LabVIEW features you use to build data acquisition and instrument control applications. Open the *Getting Started with LabVIEW* manual by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals** or by navigating to the `labview\manuals` directory and opening `LV_Getting_Started.pdf`.

Use the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help** in LabVIEW, to access information about LabVIEW

programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools. Refer to the following locations on the **Contents** tab of the *LabVIEW Help* for information about NI-DAQmx:

- **Getting Started with LabVIEW»Getting Started with DAQ**—Includes overview information and a tutorial to learn how to take an NI-DAQmx measurement in LabVIEW using the DAQ Assistant.
- **VI and Function Reference»Measurement I/O VIs and Functions**—Describes the LabVIEW NI-DAQmx VIs and properties.
- **Taking Measurements**—Contains the conceptual and how-to information you need to acquire and analyze measurement data in LabVIEW, including common measurements, measurement fundamentals, NI-DAQmx key concepts, and device considerations.

LabWindows/CVI

The **Data Acquisition** book of the *LabWindows/CVI Help* contains measurement concepts for NI-DAQmx. This book also contains *Taking an NI-DAQmx Measurement in LabWindows/CVI*, which includes step-by-step instructions about creating a measurement task using the DAQ Assistant. In LabWindows™/CVI™, select **Help»Contents**, then select **Using LabWindows/CVI»Data Acquisition**.

The **NI-DAQmx Library** book of the *LabWindows/CVI Help* contains API overviews and function reference for NI-DAQmx. Select **Library Reference»NI-DAQmx Library** in the *LabWindows/CVI Help*.

Measurement Studio

If you program your NI-DAQmx-supported device in Measurement Studio using Visual C++, Visual C#, or Visual Basic .NET, you can interactively create channels and tasks by launching the DAQ Assistant from MAX or from within Visual Studio .NET. You can generate the configuration code based on your task or channel in Measurement Studio. Refer to the *DAQ Assistant Help* for additional information about generating code. You also can create channels and tasks, and write your own applications in your ADE using the NI-DAQmx API.

For help with NI-DAQmx methods and properties, refer to the NI-DAQmx .NET Class Library or the NI-DAQmx Visual C++ Class Library included in the *NI Measurement Studio Help*. For general help with programming in Measurement Studio, refer to the *NI Measurement Studio Help*, which is fully integrated with the Microsoft Visual Studio .NET help. To view

this help file in Visual Studio. NET, select **Measurement Studio» NI Measurement Studio Help**.

To create an application in Visual C++, Visual C#, or Visual Basic .NET, follow these general steps:

1. In Visual Studio .NET, select **File»New»Project** to launch the New Project dialog box.
2. Find the Measurement Studio folder for the language you want to create a program in.
3. Choose a project type. You add DAQ tasks as a part of this step.

ANSI C without NI Application Software

The *NI-DAQmx Help* contains API overviews and general information about measurement concepts. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

The *NI-DAQmx C Reference Help* describes the NI-DAQmx Library functions, which you can use with National Instruments data acquisition devices to develop instrumentation, acquisition, and control applications. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQmx C Reference Help**.

.NET Languages without NI Application Software

With the Microsoft .NET Framework version 1.1 or later, you can use NI-DAQmx to create applications using Visual C# and Visual Basic .NET without Measurement Studio. You need Microsoft Visual Studio .NET 2003 or Microsoft Visual Studio 2005 for the API documentation to be installed.

The installed documentation contains the NI-DAQmx API overview, measurement tasks and concepts, and function reference. This help is fully integrated into the Visual Studio .NET documentation. To view the NI-DAQmx .NET documentation, go to **Start»Programs»National Instruments»NI-DAQ»NI-DAQmx .NET Reference Help**. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Reference** to view the function reference. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Using the Measurement Studio .NET Class Libraries** to view conceptual topics for using NI-DAQmx with Visual C# and Visual Basic .NET.

To get to the same help topics from within Visual Studio, go to **Help» Contents**. Select **Measurement Studio** from the **Filtered By** drop-down list and follow the previous instructions.

Device Documentation and Specifications

The following specifications documents contain contains all specifications for the following S Series devices:

- *NI PCI-6110/6111 Specifications*
- *NI 6115/6120 Specifications*
- *NI 6122/6123 Specifications*
- *NI 6132/6133 Specifications*
- *NI 6143 Specifications*

Documentation for supported devices and accessories, including PDF and help files describing device terminals, specifications, features, and operation are on the NI-DAQmx media that includes Device Documentation. Insert the media, open the Device Documentation directory, and double-click the Device Documents shortcut for your language to find, view, and print device documents.

Training Courses

If you need more help getting started developing an application with NI products, NI offers training courses. To enroll in a course or obtain a detailed course outline, refer to `ni.com/training`.

Technical Support on the Web

For additional support, refer to `ni.com/support` or `zone.ni.com`.

DAQ specifications and some DAQ manuals are available as PDFs. You must have Adobe Acrobat Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the Adobe Systems Incorporated Web site at `www.adobe.com` to download Acrobat Reader. Refer to the National Instruments Product Manuals Library at `ni.com/manuals` for updated documentation resources.

1 Getting Started

S Series devices discussed in the *S Series User Manual* are simultaneous sampling multifunction I/O devices that use the DAQ-STC ASIC.

Before installing your DAQ device, you must install the software you plan to use with the device.

Installing NI-DAQmx

The *DAQ Getting Started Guide*, which you can download at `ni.com/manuals`, offers NI-DAQmx users step-by-step instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application.

Installing Other Software

If you are using other software, refer to the installation instructions that accompany your software.

Installing the Hardware

The *DAQ Getting Started Guide* contains non-software-specific information about how to install PCI and PXI devices, as well as accessories and cables.

Device Self-Calibration

NI recommends that you self-calibrate your S Series device after installation and whenever the ambient temperature changes. Self-calibration should be performed after the device has warmed up for the recommended time period. Refer to the device specifications to find your device warm-up time. This function measures the onboard reference voltage of the device and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment. Disconnect all external signals when you self-calibrate a device.

You can initiate self-calibration using Measurement & Automation Explorer (MAX), by completing the following steps.

1. Launch MAX.
2. Select **My System»Devices and Interfaces»NI-DAQmx Devices»*your device***.
3. Initiate self-calibration using one of the following methods:
   - Click **Self-Calibrate** in the upper right corner of MAX.
   - Right-click the name of the device in the MAX configuration tree and select **Self-Calibrate** from the drop-down menu.

Note You can also programmatically self-calibrate your device with NI-DAQmx, as described in *Device Calibration* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Device Pinouts

Refer to Appendix A, *Device-Specific Information*, for S Series device pinouts.

Device Specifications

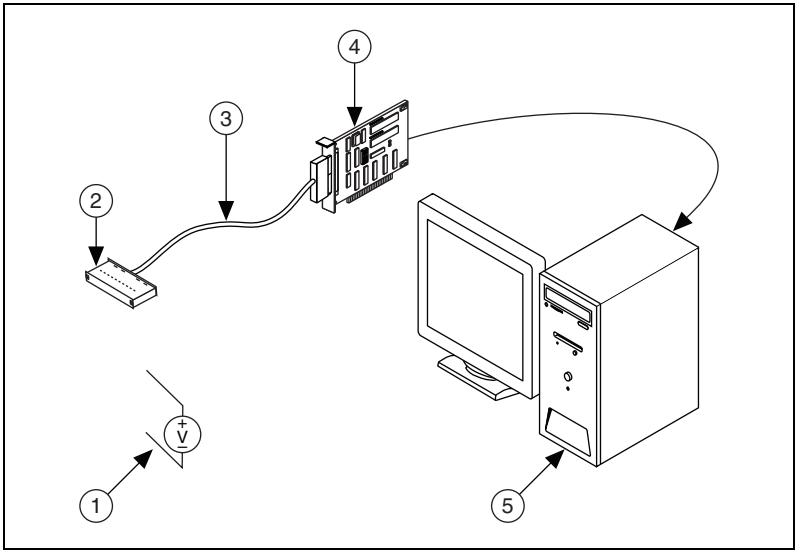
Refer to the specifications for your device, available on the NI-DAQ Device Document Browser or `ni.com/manuals`, for more detailed information about S Series devices:

- *NI PCI-6110/6111 Specifications*
- *NI 6115/6120 Specifications*
- *NI 6122/6123 Specifications*
- *NI 6132/6133 Specifications*
- *NI 6143 Specifications*

2

DAQ System Overview

Figure 2-1 shows a typical DAQ system setup, which includes transducers, signal conditioning, cables that connect the various devices to the accessories, the S Series device, and the programming software. Refer to Appendix A, *Device-Specific Information*, for a list of S Series devices and their compatible accessories.



1	Sensors and Transducers	4	DAQ Hardware
2	Signal Conditioning	5	PC or PXI Chassis and DAQ Software
3	Cable Assembly		

Figure 2-1. Typical DAQ System

DAQ Hardware

DAQ hardware digitizes signals, performs D/A conversions to generate analog output signals, and measures and controls digital I/O signals. The following sections contain more information about specific components of the DAQ hardware.

Figure 2-2 shows the components common to most S Series devices.

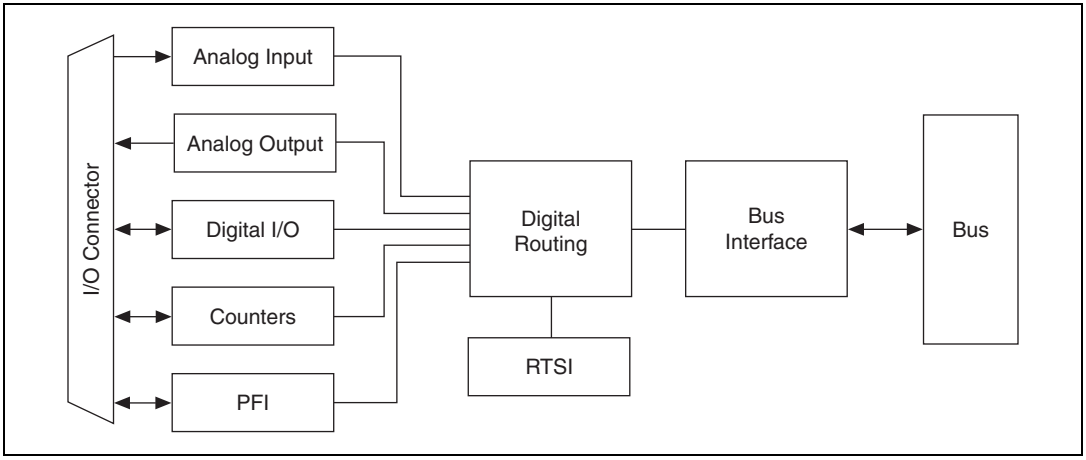


Figure 2-2. S Series Block Diagram

DAQ-STC

S Series devices use the National Instruments DAQ system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of the following three timing groups:

- **AI**—Two 24-bit, two 16-bit counters
- **AO**—Three 24-bit, one 16-bit counter
- **General-purpose counter/timer functions**—Two 24-bit counters

You can independently configure the groups for timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is flexible and completely software-configurable.

The DAQ-STC offers PFI lines to import external timing and trigger signals or to export internally generated clocks and triggers. The DAQ-STC also supports buffered operations, such as buffered waveform acquisition, buffered waveform generation, and buffered period measurement. It also supports numerous non-buffered operations, such as single pulse or pulse train generation, digital input, and digital output.

Calibration Circuitry

Calibration is the process of making adjustments to a measurement device to reduce errors associated with measurements. Without calibration, the measurement results of your device will drift over time and temperature. Calibration adjusts for these changes to improve measurement accuracy and ensure that your product meets its required specifications.

DAQ devices have high precision analog circuits that must be adjusted to obtain optimum accuracy in your measurements. Calibration determines what adjustments these analog circuits should make to the device measurements. During calibration, the value of a known, high precision measurement source is compared to the value your device acquires or generates. The adjustment values needed to minimize the difference between the known and measured values are stored in the EEPROM of the device as calibration constants. Before performing a measurement, these constants are read out of the EEPROM and are used to adjust the calibration hardware on the device. NI-DAQmx determines when this is necessary and does it automatically. If you are not using NI-DAQmx, you must load these values yourself.

You can calibrate S Series devices in two ways—through internal (or self-calibration) or through external calibration.

Internal or Self-Calibration

Self-calibration is a process to adjust the device relative to a highly accurate and stable internal reference on the device. Self-calibration is similar to the autocalibration or autozero found on some instruments. You should perform a self-calibration on a regular basis whenever environmental conditions, such as ambient temperature, change significantly. To perform self-calibration, use the self-calibrate function or VI that is included with your driver software. Self-calibration requires no external connections.

External Calibration

External calibration is a process to adjust the device relative to a traceable, high precision calibration standard. The accuracy specifications of your device change depending on how long it has been since your last external calibration. National Instruments recommends that you calibrate your device at least as often as the intervals listed in the accuracy specifications.

For a detailed calibration procedure for S Series devices, refer to the *B/E/M/S Series Calibration Procedure for NI-DAQmx*, which you can find at `ni.com/calibration` and selecting **Manual Calibration Procedures**.

Signal Conditioning

Many sensors and transducers require signal conditioning before a computer-based measurement system can effectively and accurately acquire the signal. The front-end signal conditioning system can include functions such as signal amplification, attenuation, filtering, electrical isolation, simultaneous sampling, and multiplexing. In addition, many transducers require excitation currents or voltages, bridge completion, linearization, or high amplification for proper and accurate operation. Therefore, most computer-based measurement systems include some form of signal conditioning in addition to plug-in data acquisition DAQ devices.

Sensors and Transducers

Sensors can generate electrical signals to measure physical phenomena, such as temperature, force, sound, or light. Some commonly used sensors are strain gauges, thermocouples, thermistors, angular encoders, linear encoders, and resistance temperature detectors (RTDs).

To measure signals from these various transducers, you must convert them into a form that a DAQ device can accept. For example, the output voltage of most thermocouples is very small and susceptible to noise. Therefore, you may need to amplify or filter the thermocouple output before digitizing it. The manipulation of signals to prepare them for digitizing is called signal conditioning.

For more information about sensors, refer to the following documents:

- For general information about sensors, visit `ni.com/sensors`.
- If you are using LabVIEW, refer to the *LabVIEW Help* by selecting **Help»Search the LabVIEW Help** in LabVIEW and then navigate to the **Taking Measurements** book on the **Contents** tab.
- If you are using other application software, refer to *Common Sensors* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Programming Devices in Software

National Instruments measurement devices are packaged with NI-DAQmx driver software, an extensive library of functions and VIs you can call from your application software, such as LabVIEW or LabWindows/CVI, to program all the features of your NI measurement devices. Driver software has an application programming interface (API), which is a library of VIs, functions, classes, attributes, and properties for creating applications for your device.

NI-DAQmx includes a collection of programming examples to help you get started developing an application. You can modify example code and save it in an application. You can use examples to develop a new application or add example code to an existing application.

To locate LabVIEW, LabWindows/CVI. Measurement Studio, Visual Basic, and ANSI C examples, refer to the KnowledgeBase document, *Where Can I Find NI-DAQmx Examples?*, by going to `ni.com/info` and entering the info code `daqmxexp`.

For additional examples, refer to `zone.ni.com`.

3

I/O Connector

This chapter contains information about the S Series I/O connectors.

Refer to Appendix A, *Device-Specific Information*, for the I/O connector pinout for your device.

I/O Connector Signal Descriptions

Table 3-1 describes the signals found on the I/O connectors for S Series devices. For more information about these signals, refer to the specifications for your device.

Table 3-1. S Series Device Signal Descriptions

I/O Connector Pin	Reference	Direction	Signal Description
AI <0..7> GND	—	—	**Analog Input Channels 0 through 7 Ground**—These pins are the bias current return point for differential measurements.
AI <0..7> +	AI <0..7> GND	Input	**Analog Input Channels 0 through 7 (+)**—These pins are routed to the (+) terminal of the respective channel amplifier.
AI <0..7> –	AI <0..7> GND	Input	**Analog Input Channels 0 through 7 (–)**—These pins are routed to the (–) terminal of the respective channel amplifier.
AO <0..1>	AO GND	Output	**Analog Output Channels 0 through 1**—These pins supply the voltage output of analog output channels 0 and 1.
AO GND	—	—	**Analog Output Ground**—The AO voltages and the external reference voltage are referenced to these pins.
D GND	—	—	**Digital Ground**—These pins supply the reference for the digital signals at the I/O connector and the +5 VDC supply.
P0.<0..7>	D GND	Input or Output	**Digital I/O Channels 0 through 7**—You can individually configure each signal as an input or output. P0.6 and P0.7 can also control the up/down signal of Counters 0 and 1, respectively.
+5 V	D GND	Output	**+5 Power Source**—These pins provide +5 V power. For more information, refer to the *+5 V Power Source* section.

Table 3-1. S Series Device Signal Descriptions (Continued)

I/O Connector Pin	Reference	Direction	Signal Description
EXT STROBE*	D GND	Output	**External Strobe Signal**—This output can be toggled under software control to latch signals or trigger events on external devices. This signal is not available for use with NI-DAQmx. For more information, refer to the *External Strobe Signal* section of Chapter 4, *Analog Input*.
PFI 0/AI START TRIG	D GND	Input	**PFI 0**—As an input for digital signals, this pin is a general-purpose input terminal. As an input for analog signals, this pin is the source for the hardware analog trigger. This is the default input for the AI Start Trigger signal. For more information about PFI signals, refer to Chapter 8, *Programmable Function Interfaces (PFI)*.
		Output	**AI Start Trigger Signal**—As an output, this pin emits the AI Start Trigger signal. A low-to-high transition of this signal indicates the start of an acquisition. For more information, refer to the *AI Start Trigger Signal* section of Chapter 4, *Analog Input*.
PFI 1/AI REF TRIG	D GND	Input	**PFI 1**—As an input, this is a general-purpose input terminal. This is the default input for the AI Reference Trigger signal.
		Output	**AI Reference Trigger Signal**—As an output, this pin emits the AI Reference Trigger signal. This is a low-to-high transition signal. For more information, refer to the *AI Reference Trigger Signal* section of Chapter 4, *Analog Input*.
PFI 2/AI CONV CLK	D GND	Input	**PFI 2**—As an input, this pin is a general-purpose input terminal.
		Output	**AI Convert Clock Signal**—This pin reflects the internal signal connected to AI Sample Clock. This signal is only available internally
PFI 3/CTR 1 SOURCE	D GND	Input	**PFI 3**—As an input, this pin is a general-purpose input terminal. This is the default input for the Ctr1Source signal.
		Output	**Counter 1 Source Signal**—As an output, this pin emits the selected Ctr1Source signal. This signal reflects the actual source signal connected to Counter 1. For more information, refer to the *Counter 1 Source Signal* section of Chapter 7, *Counters*.

Table 3-1. S Series Device Signal Descriptions (Continued)

I/O Connector Pin	Reference	Direction	Signal Description
PFI 4/CTR 1 GATE	D GND	Input	**PFI 4**—As an input, this pin is a general-purpose input terminal. This is the default input for the Ctr1Gate signal.
		Output	**Counter 1 Gate Signal**—As an output, this pin emits the selected Ctr1Gate signal. This signal reflects the actual gate signal connected to Counter 1. For more information, refer to the *Counter 1 Gate Signal* section of Chapter 7, *Counters*.
CTR 1 OUT	D GND	Output	**Counter 1 Output Signal**—This pin emits the Ctr1InternalOutput signal. For more information, refer to the *Counter 1 Internal Output Signal* section of Chapter 7, *Counters*.
PFI 5/AO SAMP CLK*	D GND	Input	**PFI 5**—As an input, this pin is a general-purpose input terminal.
		Output	**AO Sample Clock Signal**—As an output, this pin emits the AO Sample Clock signal. A high-to-low transition of this signal indicates a new sample is being generated. For more information, refer to the *AO Sample Clock Signal* section of Chapter 5, *Analog Output*.
PFI 6/AO START TRIG	D GND	Input	**PFI 6**—As an input, this pin is a general-purpose input terminal. This is the default input for the AO Start Trigger signal.
		Output	**AO Start Trigger Signal**—As an output, this pin emits the AO Start Trigger signal. A low-to-high transition of this signal indicates the start of a generation. For more information, refer to the *AO Start Trigger Signal* section of Chapter 5, *Analog Output*.
PFI 7/AI SAMP CLK	D GND	Input	**PFI 7**—As an input, this pin is a general-purpose input terminal.
		Output	**AI Sample Clock Signal**—As an output, this pin emits the AI Sample Clock signal. A low-to-high transition of this signal indicates the start of the sample. For more information, refer to the *AI Sample Clock Signal* section of Chapter 4, *Analog Input*.
PFI 8/CTR 0 SOURCE	D GND	Input	**PFI 8**—As an input, this pin is a general-purpose input terminal and can also be used to route signals directly to the RTSI bus. This is the default input for the Ctr0Source signal.
		Output	**Counter 0 Source Signal**—As an output, this pin emits the Ctr0Source signal. This signal reflects the actual source signal connected to Counter 0. For more information, refer to the *Counter 0 Source Signal* section of Chapter 7, *Counters*.

Table 3-1. S Series Device Signal Descriptions (Continued)

I/O Connector Pin	Reference	Direction	Signal Description
PFI 9/CTR 0 GATE	D GND	Input	**PFI 9**—As an input, this pin is a general-purpose input terminal and can also be used to route signals directly to the RTSI bus. This is the default input for the Ctr0Gate signal.
		Output	**Counter 0 Gate Signal**—As an output, this pin emits the Ctr0Gate signal. This signal reflects the actual gate signal connected to Counter 0. For more information, refer to the *Counter 0 Gate Signal* section of Chapter 7, *Counters*.
CTR 0 OUT	D GND	Input	**Counter 0 Output Signal**—As an input, this pin can be used to route signals directly to the RTSI bus. For more information, refer to the *Counter 0 Internal Output Signal* section of Chapter 7, *Counters*.
		Output	As an output, this pin emits the Ctr0InternalOutput signal.
FREQ OUT	D GND	Output	**Frequency Output Signal**—This output is from the frequency generator. For more information, refer to the *Frequency Output Signal* section of Chapter 7, *Counters*.

Terminal Name Equivalents

With NI-DAQmx, National Instruments has revised its terminal names so they are easier to understand and more consistent among National Instruments hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. Table 3-2 lists the Traditional NI-DAQ (Legacy) terminal names and their NI-DAQmx equivalents.

Table 3-2. Terminal Name Equivalents

Traditional NI-DAQ (Legacy)	NI-DAQmx
ACH#	AI #
ACH# +	AI # +
ACH# –	AI # –
ACHGND	AI GND
ACK#	PFI #
AIGND	AI GND
AISENSE	AI SENSE
AISENSE2	AI SENSE 2
AOGND	AO GND

Table 3-2. Terminal Name Equivalents (Continued)

Traditional NI-DAQ (Legacy)	NI-DAQmx
CONVERT*	AI CONV CLK or AI CONV
DAC0OUT	AO 0
DAC1OUT	AO 1
DGND	D GND
DIO_#	P0.#
DIO#	P0.#
DIOA#, DIOB#, DIOC#...	P0.#, P1.#, P2.#...
EXTREF	AO EXT REF or EXT REF
EXT_STROBE	EXT STROBE
EXT_TRIG	EXT TRIG
EXT_CONV	EXT CONV
FREQ_OUT	FREQ OUT or F OUT
GPCTR0_GATE	CTR 0 GATE
GPCTR0_OUT	CTR 0 OUT
GPCTR0_SOURCE	CTR 0 SOURCE or CTR 0 SRC
GPCTR1_GATE	CTR 1 GATE
GPCTR1_OUT	CTR 1 OUT
GPCTR1_SOURCE	CTR 1 SOURCE or CTR 1 SRC
PA#, PB#, PC#...	P0.#, P1.#, P2.#...
PFI#	PFI #
PFI_#	PFI #
PCLK#	PFI #
REQ#	PFI #
SCANCLK	AI HOLD COMP or AI HOLD
SISOURCE	AI Sample Clock Timebase
STARTSCAN	AI SAMP CLK or AI SAMP
STOPTRIG#	PFI #
TRIG1	AI START TRIG or AI START
TRIG2	AI REF TRIG or REF TRIG

Table 3-2. Terminal Name Equivalents (Continued)

Traditional NI-DAQ (Legacy)	NI-DAQmx
UISOURCE	AO Sample Clock Timebase
UPDATE	AO SAMP CLK or AO SAMP
WFTRIG	AO START TRIG or AO START

+5 V Power Source

The +5 V pins on the I/O connector supply +5 V power. You can use these pins, referenced to D GND, to power external circuitry.

Newer revision S Series devices have a traditional fuse to protect the supply from overcurrent conditions. This fuse is not customer-replaceable; if the fuse permanently opens, return the device to NI for repair.

Older revision S Series devices have a self-resetting fuse to protect the supply from overcurrent conditions. This fuse resets automatically within a few seconds after the overcurrent condition is removed. For more information about the self-resetting fuse and precautions to take to avoid improper connection of +5 V and ground terminals, refer to the KnowledgeBase document, *Self-Resetting Fuse Additional Information*, by going to `ni.com/info` and entering the info code `pptc`.

Power rating (most devices): +4.65 to +5.25 VDC at 1 A

To find your device's power rating, refer to the specifications document for your device.

Caution Never connect these +5 V power pins to analog or digital ground or to any other voltage source on the S Series device or any other device. Doing so can damage the device and the computer. NI is *not* liable for damage resulting from such a connection.

4

Analog Input

Figure 4-1 shows the analog input circuitry of each channel of an S Series device.

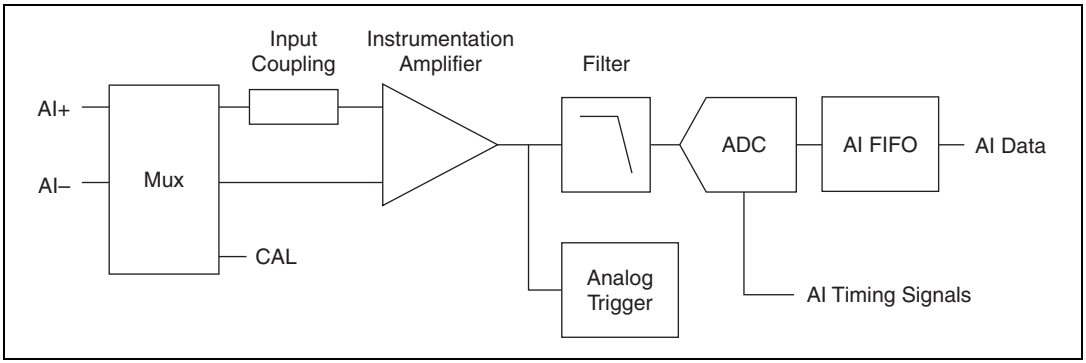


Figure 4-1. S Series Analog Input Block Diagram

Note Figure 4-1 offers a general overview of the analog input circuitry for most S Series devices. Refer to Appendix A, *Device-Specific Information*, for a diagram of the specific elements that comprise the analog input circuitry of your device.

On S Series devices, each channel uses its own instrumentation amplifier, FIFO, multiplexer (mux), and A/D converter to achieve simultaneous data acquisition. The main blocks featured in the S Series analog input circuitry are as follows:

- **Mux**—By default, the mux is set to route AI signals to the analog front end. When you calibrate your device, the state of the mux switches. You can manually switch the state of the mux to measure AI GND.
- **Input Coupling—(NI 611*x*/6120 Only)** You can configure these S Series devices for either AC or DC input coupling on a per-channel basis. Use AC coupling when the AC signal contains a large DC component. If you enable AC coupling, you remove the large DC offset for the input amplifier and amplify only the AC component. This configuration makes effective use of the ADC dynamic range.

- **Instrumentation Amplifier**—The instrumentation amplifier can amplify or attenuate an AI signal to ensure that you get the maximum resolution of the ADC. NI 611*x*/6120/6123/6133 devices provide programmable instrumentation amplifiers that allow you to select the input range.
- **Filter**—The filter on the S Series device minimizes high frequency noise without attenuating signals of interest within the Nyquist bandwidth.
- **A/D Converter**—The analog-to-digital converter (ADC) digitizes the AI signal by converting the analog voltage into a digital number.
- **AI FIFO**—A large first-in-first-out (FIFO) buffer holds data during A/D conversions to ensure that no data is lost. S Series devices can handle multiple A/D conversion operations with DMA, interrupts, or programmed I/O.
- **Analog Trigger**—For information about the trigger circuitry of S Series devices, refer to the *Analog Input Triggering* section.
- **AI Timing Signals**—For information about the analog input timing signals available on S Series devices, refer to the *Analog Input Timing Signals* section.

Analog Input Terminal Configuration

S Series devices support only differential (DIFF) input mode. The channels on S Series devices are true differential inputs, meaning both positive and negative inputs can carry signals of interest. For more information about differential input, refer to the *Connecting Analog Input Signals* section, which contains diagrams showing the signal paths for differential input mode.

(NI 611*x*/6120 Only) The channels on these S Series devices are pseudodifferential inputs. The input signal of each channel, AI <0..*x*> +, is connected to the positive input of the instrumentation amplifier, and each reference signal AI <0..*x*> –, is connected to the negative input of the instrumentation amplifier. The inputs are differential only in the sense that ground loops are broken. The reference signal, AI <0..*x*> –, is not intended to carry signals of interest but only to provide a DC reference point for AI <0..*x*> + that may be different from ground.

Pseudodifferential signal connections reduce noise pickup and increase common-mode noise rejection. This connection type also allows input signals to float within the common-mode limits of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings can be found in the specifications document for each S Series device.

Input Polarity and Range

Input range refers to the set of input voltages that an analog input channel can digitize with the specified accuracy. On some S Series devices, you can individually program the input range of each AI channel.

The input range affects the resolution of the S Series device for an AI channel. Resolution refers to the voltage of one ADC code. For example, a 16-bit ADC converts analog inputs into one of 65,536 (= 2^{16}) codes, meaning one of 65,536 possible digital values. These values are spread fairly evenly across the input range. So, for an input range of –5 V to 5 V, the voltage of each code of a 16-bit ADC is:

$$\frac{5\text{ V} - (-5\text{ V})}{2^{16}} = 153\ \mu\text{V}$$

S Series devices support bipolar input ranges. A bipolar input range means that the input voltage range is between $-V_{ref}$ and V_{ref}.

The instrumentation amplifier applies a different gain setting to the AI signal depending on the input range. Gain refers to the factor by which the instrumentation amplifier multiplies (amplifies) the input signal before sending it to the ADC.

On S Series devices with programmable input ranges, choose an input range that matches the expected input range of your signal. A large input range can accommodate a large signal variation, but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but may result in the input signal going out of range. For more information about programming these settings, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Working Voltage Range

On most S Series devices, the PGIA operates normally by amplifying signals of interest while rejecting common-mode signals under the following three conditions:

- The common-mode voltage (V_{cm}), which is equivalent to subtracting AI <0..*x*> GND from AI <0..*x*> –, must be less than ±10 V. This V_{cm} is a constant for all range selections.
- The signal voltage (V_s), which is equivalent to subtracting AI <0..*x*> + from AI <0..*x*> –, must be less than or equal to the range selection of the given channel. If V_s is greater than the range selected, the signal clips and information are lost.
- The total working voltage of the positive input, which is equivalent to (V_{cm} + V_s), or subtracting AI <0..*x*> GND from AI <0..*x*> +, must be less than ±11 V.

If any of these conditions are exceeded, the input voltage is clamped until the fault condition is removed.

Note All inputs are protected at up to ±42 V.

(NI 6143 Only) The instrumentation amplifier operates normally by amplifying signals of interest while rejecting common-mode signals under one condition. The total voltage, (V_{cm} + V_s), present at the positive and negative input terminals must be less than the working voltage, which is ±7 V.

AI Data Acquisition Methods

When performing analog input measurements, there are several different data acquisition methods available. You can either perform software-timed or hardware-timed acquisitions:

- **Software-Timed Acquisitions**—With a software-timed acquisition, software controls the rate of the acquisition. Software sends a separate command to the hardware to initiate each ADC conversion. In NI-DAQmx, software-timed acquisitions are referred to as having on demand timing. Software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single point of data.
- **Hardware-Timed Acquisitions**—With hardware-timed acquisitions, a digital hardware signal controls the rate of the acquisition. This

signal can be generated internally on your device or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions:

– The time between samples can be much shorter.

– The timing between samples can be deterministic.

– Hardware-timed acquisitions can use hardware triggering. For more information, refer to Chapter 12, *Triggering*.

Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in the computer memory where acquired samples are stored.

– Buffered—In a buffered acquisition, data is moved from the DAQ device's onboard FIFO memory to a PC buffer using DMA or interrupts before it is transferred to ADE memory. Buffered acquisitions typically allow for much faster transfer rates than non-buffered acquisitions because data is moved in large blocks, rather than one point at a time. For more information about DMA and interrupts, refer to the *Data Transfer Methods* section of Chapter 11, *Bus Interface*.

  One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

  • Finite sample mode acquisition refers to the acquisitions of a specific, predetermined number of data samples. After the specified number of samples has been collected into the buffer, the acquisition stops. If you use a reference trigger, you must use finite sample mode. Refer to the *AI Reference Trigger Signal* section for more information.

  • Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous acquisition continues until you stop the operation. A continuous acquisition is also referred to as double-buffered or circular-buffered acquisition.

    If data cannot be transferred across the bus fast enough, the data in the FIFO will be overwritten and an error will be generated. With continuous operations, if the user program does not read data out of the PC buffer fast enough to keep up with the data transfer, the buffer could reach an overflow condition, causing an error to be generated.

– Non-Buffered—In non-buffered acquisitions, data is read directly from the FIFO on the device. Typically, hardware-timed non-buffered operations are used to read single samples with known time increments between them and small latency.

Analog Input Triggering

Analog input supports three different triggering actions: start, reference, and pause. An analog or digital hardware trigger can initiate these actions. All S Series devices support digital triggering, and some also support analog triggering. To find your device's triggering options, refer to the specifications document for your device.

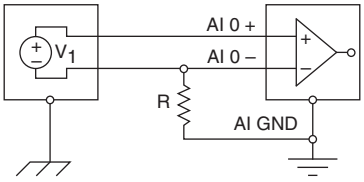
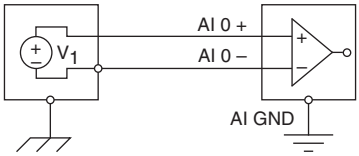
The *AI Start Trigger Signal*, *AI Reference Trigger Signal*, and *AI Pause Trigger Signal* sections contain information about the analog input trigger signals.

Refer to Chapter 12, *Triggering*, for more information about triggers.

Connecting Analog Input Signals

Table 4-1 summarizes the recommended input configuration for different types of signal sources for S Series devices.

Table 4-1. S Series Analog Input Signal Configuration

Input	Floating Signal Sources (Not Connected to Earth Ground)	Ground-Referenced Signal Sources
	Examples: • Ungrounded thermocouples • Signal conditioning with isolated outputs • Battery devices	Example: • Plug-in instruments with non-isolated outputs
Differential (DIFF)		

Refer to the *Analog Input Terminal Configuration* section for descriptions of the input modes.

Types of Signal Sources

When configuring the input channels and making signal connections, first determine whether the signal sources are ground-referenced or floating:

- **Ground-Referenced Signal Sources**—A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system as the source. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

  The difference in ground potential between two instruments connected to the same building power system is typically between 1 mV and 100 mV, but the difference can be much higher if power distribution circuits are improperly connected. If a grounded signal source is incorrectly measured, this difference can appear as measurement error. Follow the connection instructions for grounded signal sources to eliminate this ground potential difference from the measured signal.
- **Floating Signal Sources**—A floating signal source is not connected in any way to the building ground system, and instead has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must connect the ground reference of a floating signal to the AI ground of the device to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats outside the common-mode input range.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-2 shows how to connect a ground-referenced signal source to a channel on an S Series device.

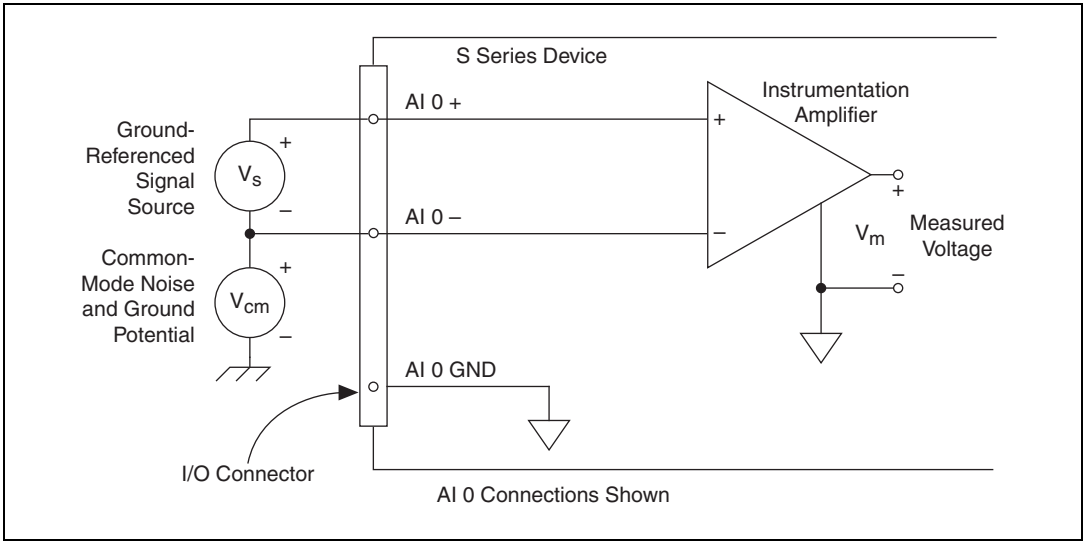


Figure 4-2. Differential Connection for Ground-Referenced Signals

With these types of connections, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in the figure.

Common-Mode Signal Rejection Considerations

The instrumentation amplifier can reject any voltage caused by ground potential differences between the signal source and the device. In addition, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within the working voltage range of the device.

Differential Connections for Floating Signal Sources

Figure 4-3 shows how to connect a floating, or non-referenced, signal source to a channel on an S Series device.

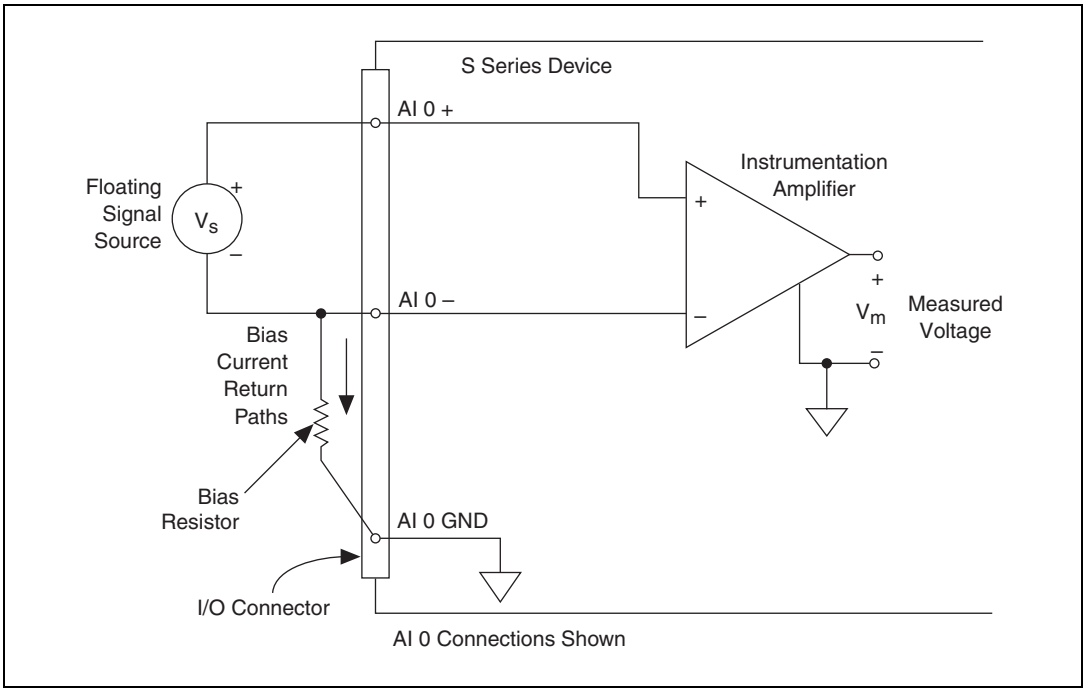


Figure 4-3. Differential Connection for Floating Signals

Figure 4-3 shows a bias resistor connected between AI 0 – and the floating signal source ground. This resistor provides a return path for the bias current. A value of 10 kΩ to 100 kΩ is usually sufficient. If you do not use the resistor and the source is truly floating, the source is not likely to remain within the common-mode signal range of the instrumentation amplifier, so the instrumentation amplifier saturates, causing erroneous readings. You must reference the source to the respective channel ground.

DC-Coupled

You can connect low source impedance and high source impedance DC-coupled sources:

- **Low Source Impedance**—You must reference the source to AI GND. The easiest way to make this reference is to connect the positive side of the signal to the positive input of the instrumentation amplifier and

connect the negative side of the signal to AI GND as well as to the negative input of the instrumentation amplifier, without using resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

- **High Source Impedance**—For larger source impedances, this connection leaves the differential signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the instrumentation amplifier does not reject it. In this case, instead of directly connecting the negative line to AI GND, connect the negative line to AI GND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. This configuration does not load down the source (other than the very high input impedance of the instrumentation amplifier).

  You can fully balance the signal path by connecting another resistor of the same value between the positive input and AI GND. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

AC-Coupled

Both inputs of the instrumentation amplifier require a DC path to ground in order for the instrumentation amplifier to work. If the source is AC-coupled (capacitively coupled), the instrumentation amplifier needs a resistor between the positive input and AI GND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, connect the negative input directly to AI GND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source.

Pseudodifferential Connections for Ground-Referenced Signal Sources

(NI 6115/6120 Only) Figure 4-4 shows how to connect a ground-referenced signal source to a channel on the NI 6115.

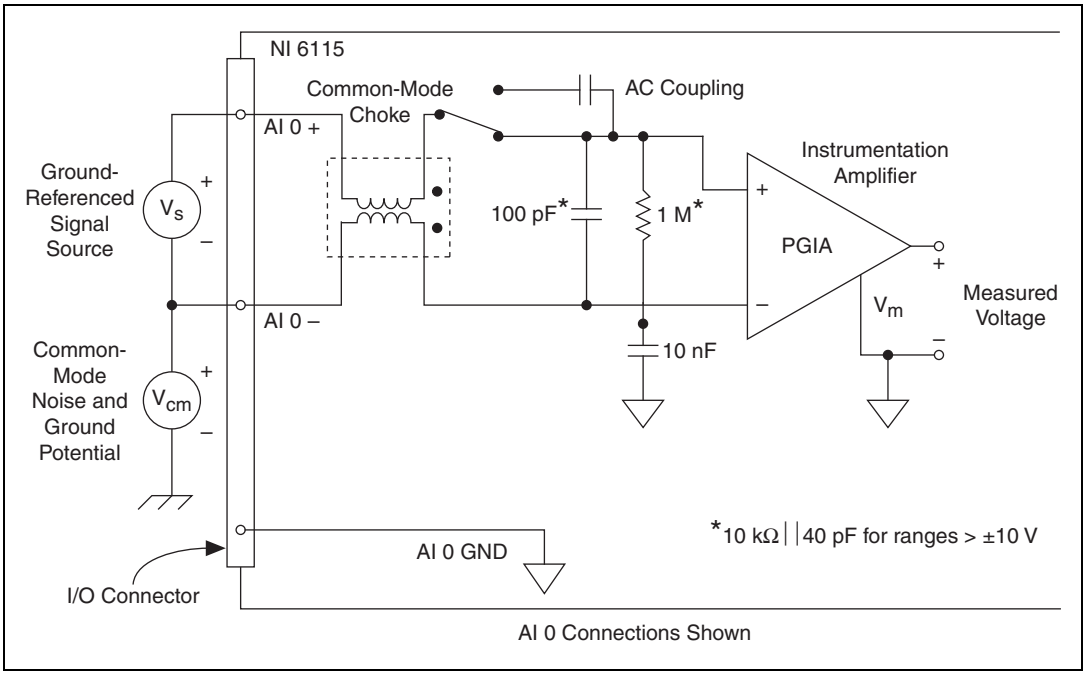


Figure 4-4. Pseudodifferential Connection for Ground-Referenced Signals on NI 6115 Devices

Figure 4-5 shows how to connect a ground-referenced signal source to a channel on the NI 6120.

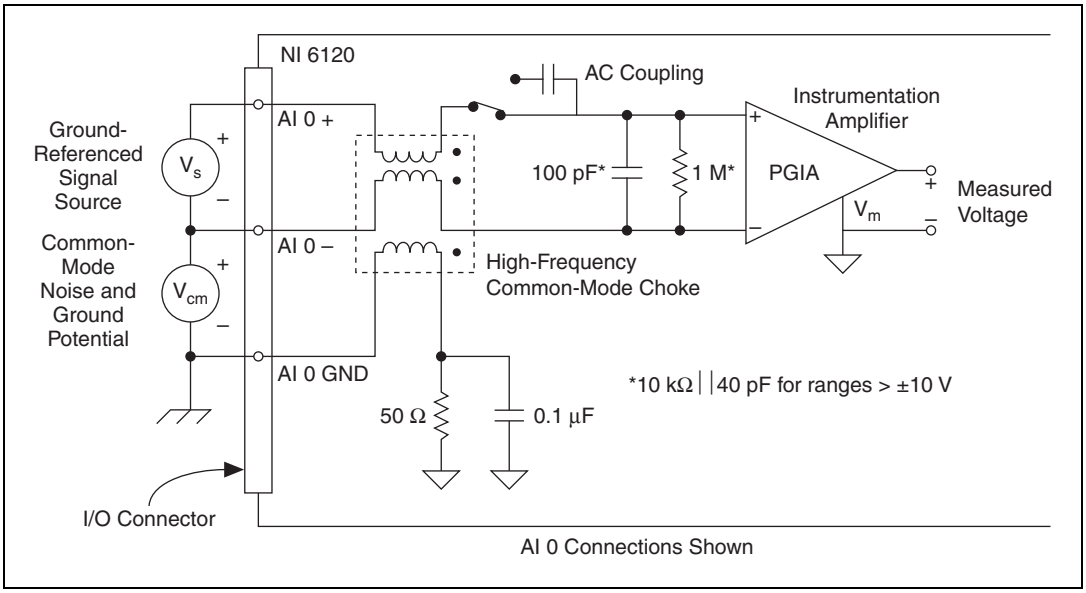


Figure 4-5. Pseudodifferential Connection for Ground-Referenced Signals on NI 6120 Devices

With this type of connection, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in these figures.

Common-Mode Signal Rejection Considerations

The instrumentation amplifier can reject any voltage caused by ground potential differences between the signal source and the device. In addition, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within the working voltage range of the device.

Like any amplifier, the common-mode rejection ratio (CMRR) of the PGIA is limited at high frequency. A common-mode choke on each channel of the NI 6115/6120 compensates for this limitation.

(NI 6115 Only) The purpose of the 10 nF capacitance on the AI <0..3> – connection of the NI 6115 is to provide an impedance for this choke to work against at high frequency, which improves the high-frequency CMRR. Depending on your application and the type of common noise at your source, it is possible to gain further common-noise rejection by placing a 0.1 µF ceramic bypass capacitor between AI – and AI 0 GND.

Pseudodifferential Connections for Floating Signal Sources

(NI 6115/6120 Only) Figure 4-6 shows how to connect a floating, or non-referenced, signal source to a channel on the NI 6115.

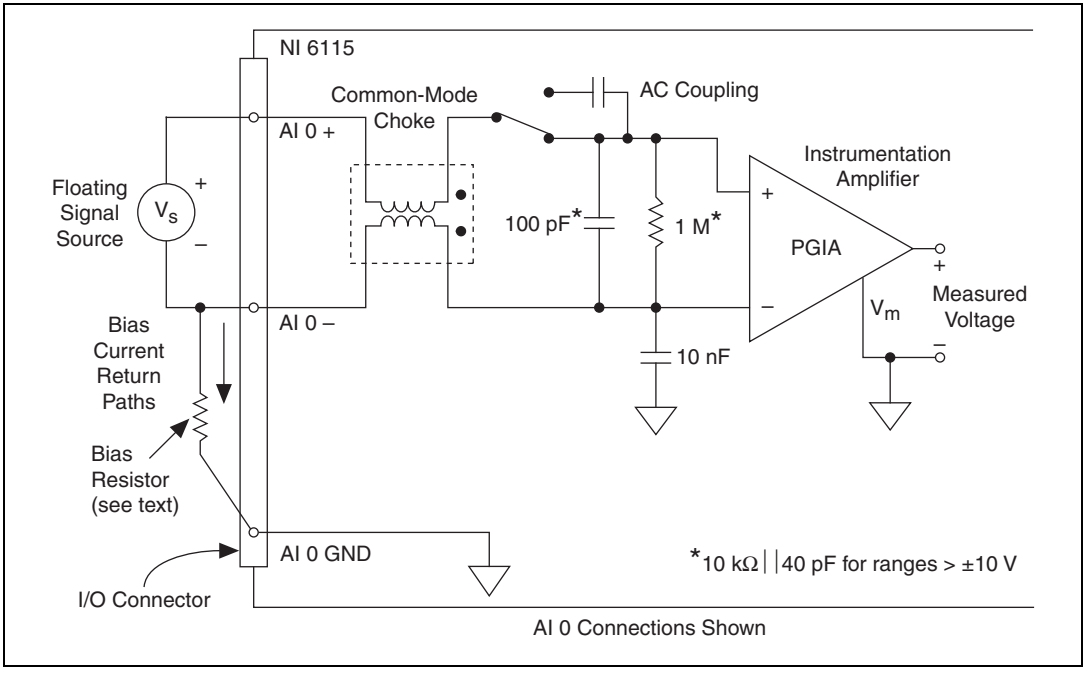


Figure 4-6. Pseudodifferential Connection for Floating Signals on NI 6115 Devices

Figure 4-7 shows how to connect a floating signal source to a channel on the NI 6120.

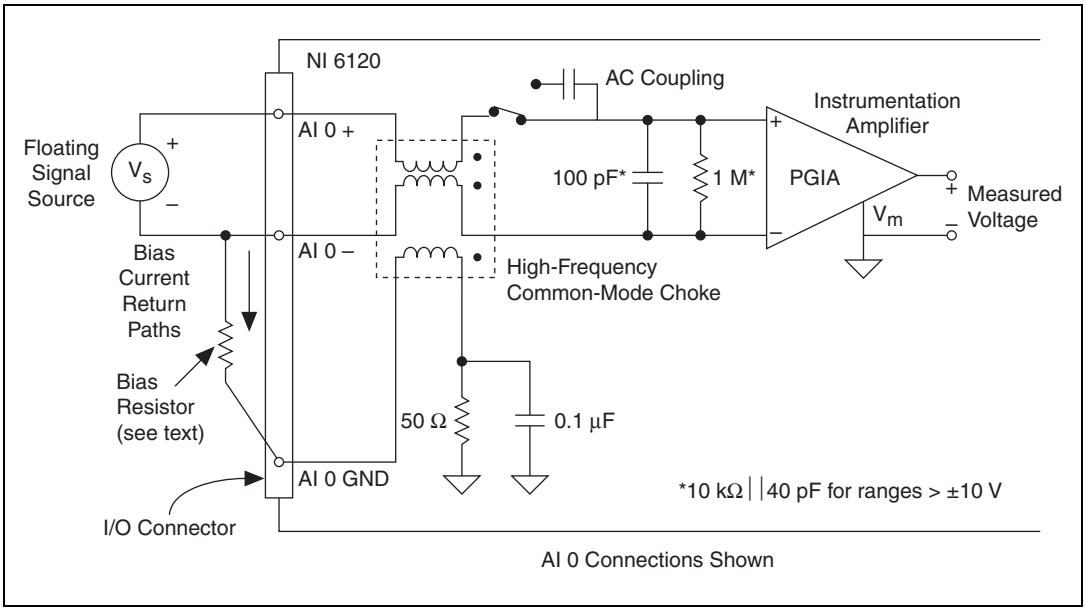


Figure 4-7. Pseudodifferential Connection for Floating Signals on NI 6120 Devices

The figures show a bias resistor connected between AI 0 – and the floating signal source ground. This resistor provides a return path for the bias current. A value of 10 kΩ to 100 kΩ is usually sufficient. If you do not use the resistor and the source is truly floating, the source is not likely to remain within the common-mode signal range of the instrumentation amplifier, so the instrumentation amplifier saturates, causing erroneous readings. You must reference the source to the respective channel ground.

Common-mode rejection might be improved by using another bias resistor from the AI 0 + input to AI 0 GND. This connection gives a slight measurement error due to the voltage divider formed with the output impedance of the floating source, but it also gives a more balanced input for better common-mode rejection.

If a signal source is truly floating, you can use a bias resistor with a smaller value to reduce noise. You can further reduce noise by putting a capacitor in parallel with the bias resistor.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the S Series device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions.

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the AI + and AI – inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI DAQ system is the video monitor. Separate the monitor from the analog signals as far as possible.
- Separate the signal lines of the S Series device from high-current or high-voltage lines. These lines can induce currents in or voltages on the signal lines of the S Series device if they run in close parallel paths. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone document, *Field Wiring and Noise Considerations for Analog Signals*, for more information. To access this document, go to `ni.com/info` and enter the info code `rdfwn3`.

Minimizing Drift in Differential Mode

If the readings from the DAQ device are random and drift rapidly, you should check the ground-reference connections. The signal can be referenced to a level that is considered floating with reference to the device ground reference. Even though you are in differential mode, you must still

reference the signal to the same ground level as the device reference. There are various methods of achieving this reference while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in the *Connecting Analog Input Signals* section.

AI GND is an AI common signal that routes directly to the ground connection point on the devices. You can use this signal if you need a general analog ground connection point to the device.

Analog Input Timing Signals

An acquisition with posttrigger data allows you to view data that is acquired after a trigger event is received. A typical posttrigger DAQ sequence is shown in Figure 4-8. The sample counter is loaded with the specified number of posttrigger samples, in this example, five. The value decrements with each pulse on AI Sample Clock (ai/SampleClock), until the value reaches zero and all desired samples have been acquired.

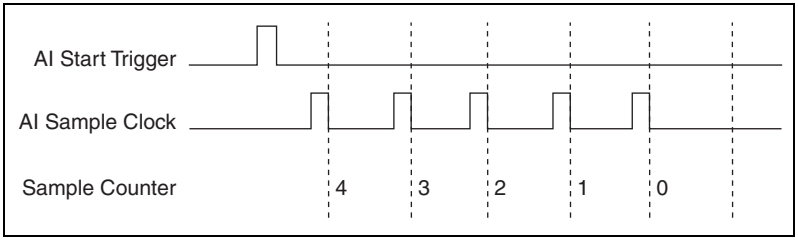


Figure 4-8. Typical Posttriggered DAQ Sequence

An acquisition with pretrigger data allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. Figure 4-9 shows a typical pretrigger DAQ sequence. The AI Start Trigger (ai/StartTrigger) signal can be either a hardware or software signal. If AI Start Trigger is set up to be a software start trigger, an output pulse appears on the AI START TRIG line when the acquisition begins. When the AI Start Trigger pulse occurs, the sample counter is loaded with the number of pretrigger samples, in this example, four. The value decrements with each pulse on AI Sample Clock, until the value reaches zero. The sample counter is then loaded with the number of posttrigger samples, in this example, three.

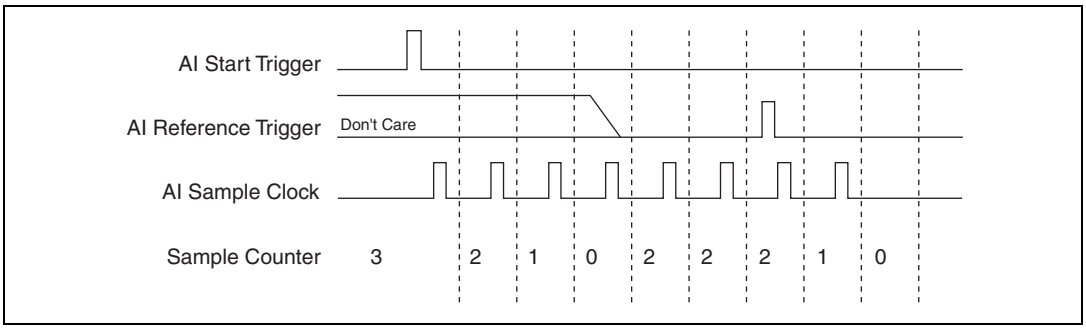


Figure 4-9. Typical Pretriggered DAQ Sequence

If an AI Reference Trigger (ai/ReferenceTrigger) pulse occurs before the specified number of pretrigger samples are acquired, the trigger pulse is ignored. Otherwise, when the AI Reference Trigger pulse occurs, the sample counter value decrements until the specified number of posttrigger samples have been acquired. For more information about start and reference triggers, refer to the *Analog Input Triggering* section.

In order to provide all of the timing functionality described throughout this section, the DAQ-STC provides an extremely powerful and flexible timing engine. For more information about all of the clock routing and timing options that the analog input timing engine provides, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

S Series devices feature the following analog input timing signals:

- *AI Sample Clock Signal*
- *AI Sample Clock Timebase Signal*
- *AI Start Trigger Signal*
- *AI Reference Trigger Signal*
- *AI Pause Trigger Signal*
- *Master Timebase Signal*
- *External Strobe Signal*

AI Sample Clock Signal

You can use the AI Sample Clock (ai/SampleClock) signal to initiate a measurement. Your S Series device samples the AI signals on all channels once for every occurrence of AI Sample Clock. A measurement acquisition consists of one or more samples.

The source of the AI Sample Clock signal can be internal or external. You specify whether the measurement sample begins on the rising edge or falling edge of the AI Sample Clock signal.

Using an Internal Source

By default, AI Sample Clock is created internally by dividing down the AI Sample Clock Timebase.

Several other internal signals can be routed to the sample clock. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an External Source

You can use a signal connected to any PFI or RTSI <0..6> pin as the source of AI Sample Clock. Figure 4-10 shows the timing requirements of the AI Sample Clock source.

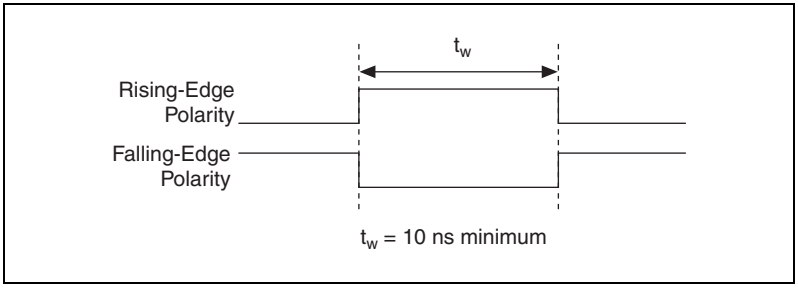


Figure 4-10. AI Sample Clock Timing Requirements

Outputting the AI Sample Clock Signal

You can configure the PFI 7/AI SAMP CLK pin to output the AI Sample Clock signal. The output pin reflects the AI Sample Clock signal regardless of what signal you specify as its source. Your DAQ device briefly pulses the PFI 7/AI SAMP CLK pin once for every occurrence of AI Sample Clock.

Figure 4-11 shows the timing of pulse behavior of the PFI 7/AI SAMP CLK pin when the pin is an output.

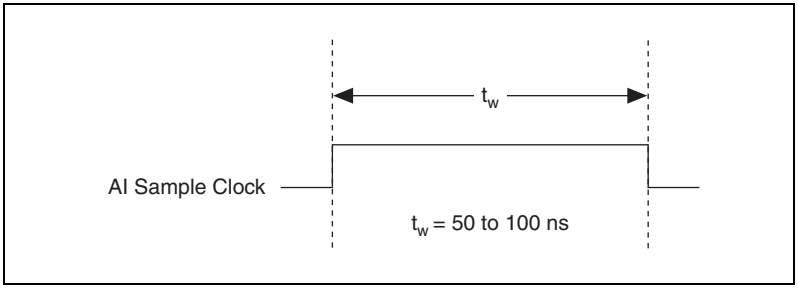


Figure 4-11. PFI 7/AI SAMP CLK as an Output

The PFI 7/AI SAMP CLK pin is configured as an input by default.

Other Timing Requirements

A counter on your device internally generates AI Sample Clock unless you select some external source. The AI Start Trigger signal starts this counter. It is stopped automatically by hardware after a finite acquisition completes or manually through software. When using an internally generated AI Sample Clock in NI-DAQmx, you can also specify a configurable delay from the AI Start Trigger to the first AI Sample Clock pulse. By default, this delay is two ticks of the AI Sample Clock Timebase signal.

Figure 4-12 shows the relationship of the AI Sample Clock signal to the AI Start Trigger signal.

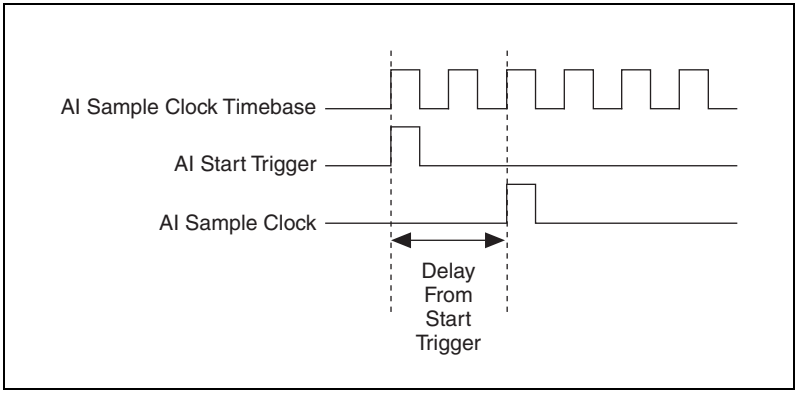


Figure 4-12. AI Sample Clock and AI Start Trigger

AI Sample Clock Timebase Signal

Any PFI can externally input the AI Sample Clock Timebase (ai/SampleClockTimebase) signal, which is not available as an output on the I/O connector. The AI Sample Clock Timebase is divided down to provide the Onboard Clock source for the AI Sample Clock. You can configure the polarity selection for AI Sample Clock Timebase as either rising or falling edge.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20MHzTimebase or the 100kHzTimebase generates AI Sample Clock Timebase unless you select some external source. Figure 4-13 shows the timing requirements for AI Sample Clock Timebase.

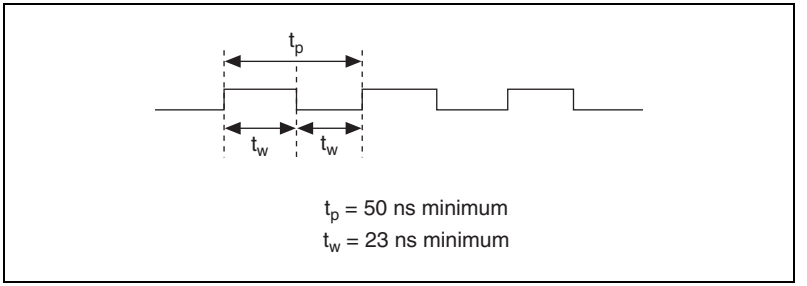


Figure 4-13. AI Sample Clock Timebase Timing Requirements

AI Start Trigger Signal

You can use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. A measurement acquisition consists of one or more samples. If you do not use triggers, you begin a measurement with a software command. After the acquisition begins, you can configure the acquisition to stop:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

Using a Digital Source

To use AI Start Trigger with a digital source, you specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Also, specify whether the measurement acquisition begins on the rising edge or falling edge of the AI Start Trigger signal.

Figure 4-14 shows the timing requirements of the AI Start Trigger source.

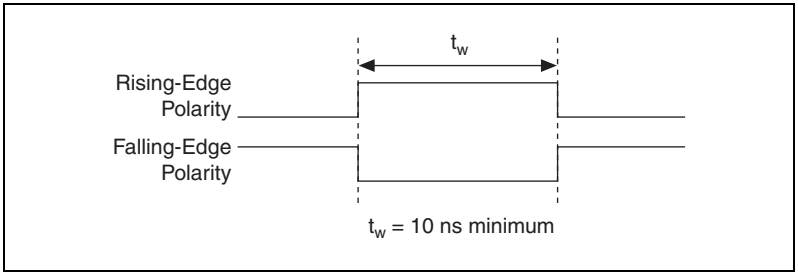


Figure 4-14. AI Start Trigger Timing Requirements

Using an Analog Source

When you use an analog trigger source, the acquisition begins on the first rising edge of the Analog Comparison Event signal. For more information, refer to the *Triggering with an Analog Source* section of Chapter 12, *Triggering*.

Outputting the AI Start Trigger Signal

You can configure the PFI 0/AI START TRIG pin to output the AI Start Trigger signal. The output pin reflects the AI Start Trigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 4-15 shows the timing behavior of the PFI 0/AI START TRIG pin when the pin is an output.

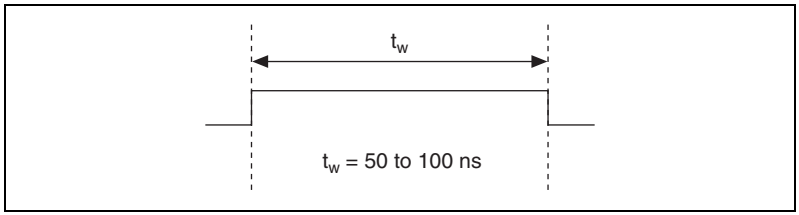


Figure 4-15. PFI 0/AI START TRIG as an Output

The PFI 0/AI START TRIG pin is configured as an input by default.

When acquisitions use a start trigger without a reference trigger, they are posttrigger acquisitions because data is acquired only after the trigger. The device also uses AI Start Trigger to initiate pretrigger DAQ operations. In most pretrigger applications, a software trigger generates AI Start Trigger. Refer to the *AI Reference Trigger Signal* section for a complete description of the use of AI Start Trigger and AI Reference Trigger in a pretrigger DAQ operation.

AI Reference Trigger Signal

You can use the AI Reference Trigger (ai/ReferenceTrigger) signal to stop a measurement acquisition. To use a reference trigger, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The number of posttrigger samples (samples that occur after the reference trigger) desired is the buffer size minus the number of pretrigger samples.

When the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. You can access this data (with some limitations) before the DAQ device discards it. Refer to the KnowledgeBase document, *Can a Pretriggered Acquisition be Continuous?*, for more information. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rdcanq`.

When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the number of posttrigger samples desired. Figure 4-16 shows the final buffer.

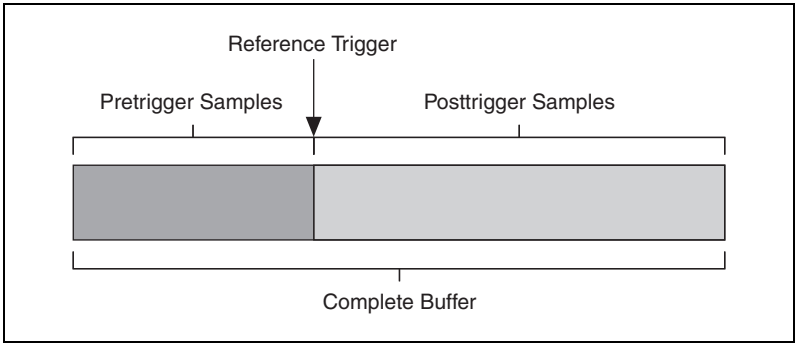


Figure 4-16. Reference Trigger Final Buffer

Using a Digital Source

To use AI Reference Trigger with a digital source, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Also, specify whether the measurement acquisition stops on the rising edge or falling edge of the AI Reference Trigger signal.

Figure 4-17 shows the timing requirements of the AI Reference Trigger source.

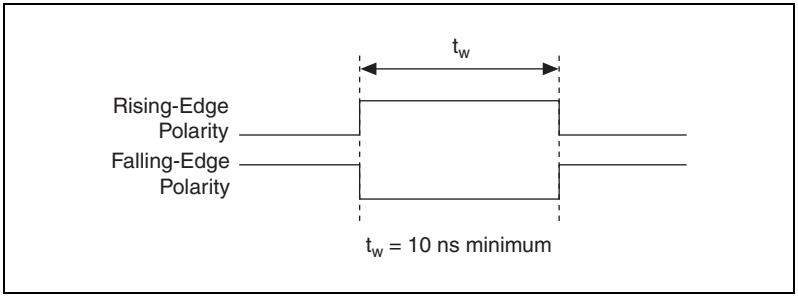


Figure 4-17. AI Reference Trigger Source Timing Requirements

Using an Analog Source

When you use an analog trigger source, the acquisition stops on the first rising edge of the Analog Comparison Event signal. For more information, refer to the *Triggering with an Analog Source* section of Chapter 12, *Triggering*.

Outputting the AI Reference Trigger Signal

You can configure the PFI 1/AI REF TRIG pin to output the AI Reference Trigger signal. The output pin reflects the AI Reference Trigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 4-18 shows the timing behavior of the PFI 1/AI REF TRIG pin when the pin is an output.

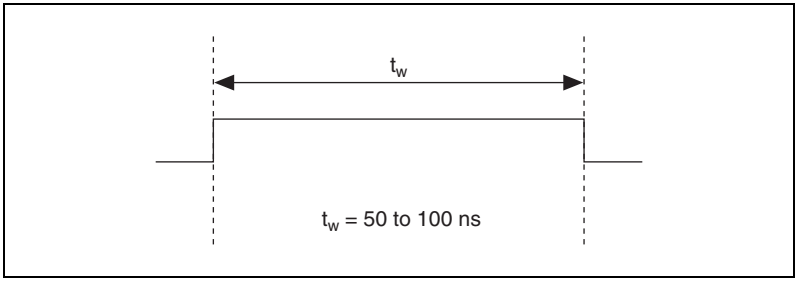


Figure 4-18. PFI/AI REF TRIG Timing Behavior

The PFI 1/AI REF TRIG pin is configured as an input by default.

AI Pause Trigger Signal

You can use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. This signal is not available as an output.

Using a Digital Source

To use AI Pause Trigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Also, specify whether the measurement sample is paused when AI Pause Trigger is at a logic high or low level.

Using an Analog Source

When you use an analog trigger source, the internal sample clock pauses when the Analog Comparison Event signal is low and resumes when the signal goes high (or vice versa). For more information, refer to the *Triggering with an Analog Source* section of Chapter 12, *Triggering*.

Note Pause triggers are only sensitive to the level of the source, not the edge.

Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the device are derived. It controls the timing for the analog input, analog output, and counter subsystems. It is available as an output on the I/O connector, but you must use one or more counters to do so.

The maximum allowed frequency for the Master Timebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the Master Timebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the Master Timebase unless you wish to synchronize multiple devices, in which case, you should use RTSI 7. Refer to Chapter 10, *Real-Time System Integration Bus (RTSI),* for more information about which signals are available through RTSI.

Figure 4-19 shows the timing requirements for Master Timebase.

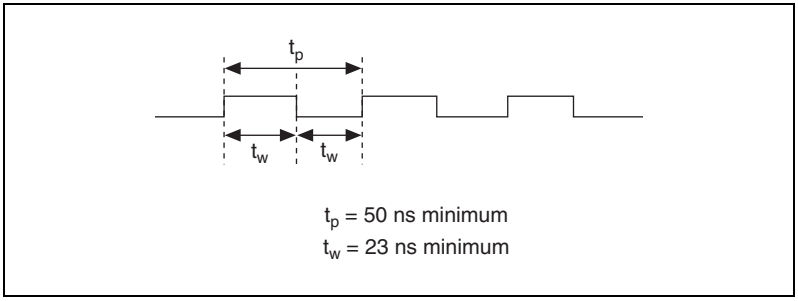


Figure 4-19. Master Timebase Timing Requirements

External Strobe Signal

External Strobe is an output-only signal on the EXT STROBE pin that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the External Strobe. External Strobe is used for signal conditioning with SCXI and is not available for use with NI-DAQmx.

Getting Started with AI Applications in Software

You can use the S Series device in the following analog input applications:

- Simultaneous sampling
- Single-point analog input
- Finite analog input
- Continuous analog input

You can perform these applications through DMA, interrupt, or programmed I/O data transfer mechanisms. Some of the applications also use start, reference, and pause triggers.

Note For more information about programming analog input applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

5

Analog Output

Figure 5-1 shows the analog output circuitry of an S Series NI 611*x*/6120 device.

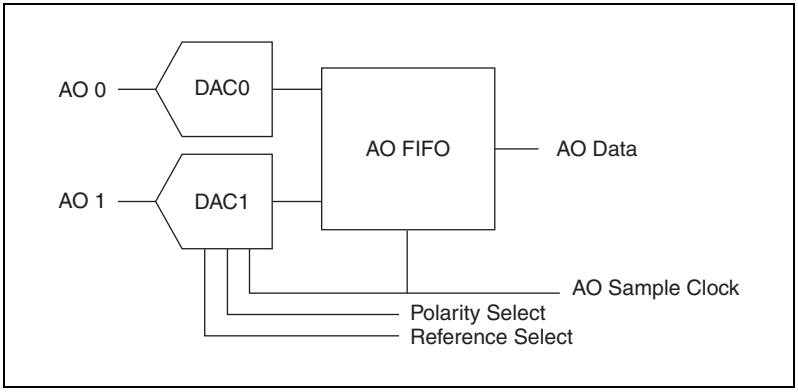


Figure 5-1. S Series Device Analog Output Block Diagram

Note Analog output is *not* a feature on the NI 6122/6123/613*x*/6143 devices.

The main blocks featured in the S Series analog output circuitry are as follows:

- **DACs**—Digital-to-analog converters (DACs) convert digital codes to analog voltages.
- **AO FIFO**—The AO FIFO enables analog output waveform generation. It is a first-in-first-out (FIFO) memory buffer between the computer and the DACs that allows you to download all the points of a waveform to your device without host computer interaction.
- **AO Sample Clock**—The DAC reads a sample from the FIFO with every cycle of the AO Sample Clock signal and generates the AO voltage. For more information, refer to the *AO Sample Clock Signal* section.

Minimizing Glitches on the Output Signal

When you use a DAC to generate a waveform, you may observe glitches on the output signal. These glitches are normal; when a DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the DACcode switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. Visit `ni.com/support` for more information about minimizing glitches.

AO Data Generation Methods

When performing an analog output operation, there are several different data generation methods available. You can either perform software-timed or hardware-timed generations:

- **Software-Timed Generations**—With a software-timed generation, software controls the rate at which data is generated. Software sends a separate command to the hardware to initiate each DAC conversion. In NI-DAQmx, software-timed generations are referred to as on demand timing. Software-timed generations are also referred to as immediate or static operations. They are typically used for writing a single value out, such as a constant DC voltage.
- **Hardware-Timed Generations**—With a hardware-timed generation, a digital hardware signal controls the rate of the generation. This signal can be generated internally on your device or provided externally.

  Hardware-timed generations have several advantages over software-timed generations:

  – The time between samples can be much shorter.

  – The timing between samples can be deterministic.

  – Hardware-timed generations can use hardware triggering. For more information, refer to Chapter 12, *Triggering*.

  Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in computer memory for acquired or to-be-generated samples.

  – Buffered—In a buffered generation, data is moved from a PC buffer to the DAQ device's onboard FIFO using DMA or interrupts before it is written to the DACs one sample at a time. Buffered generations typically allow for much faster transfer rates than non-buffered generations because data is moved in large blocks, rather than one point at a time. For more information about

DMA and interrupts, refer to the *Data Transfer Methods* section of Chapter 11, *Bus Interface*.

One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

- Finite sample mode generation refers to the generation of a specific, predetermined number of data samples. When the specified number of samples has been written out, the generation stops.
- Continuous generation refers to the generation of an unspecified number of samples. Instead of generating a set number of data samples and stopping, a continuous generation continues until you stop the operation. There are several different methods of continuous generation that control what data is written. These methods are regeneration, FIFO regeneration and non-regeneration modes.

  Regeneration is the repetition of the data that is already in the buffer. Standard regeneration is when data from the PC buffer is continually downloaded to the FIFO to be written out. New data can be written to the PC buffer at any time without disrupting the output.

  With FIFO regeneration, the entire buffer is downloaded to the FIFO and regenerated from there. After the data is downloaded, new data cannot be written to the FIFO. To use FIFO regeneration, the entire buffer must fit within the FIFO size. The advantage of using FIFO regeneration is that it does not require communication with the main host memory after the operation is started, thereby preventing any problems that may occur due to excessive bus traffic.

  With non-regeneration, old data will not be repeated. New data must be continually written to the buffer. If the program does not write new data to the buffer at a fast enough rate to keep up with the generation, the buffer will underflow and cause an error.

– Non-Buffered—In hardware-timed non-buffered generations, data is written directly to the FIFO on the device. Typically, hardware-timed non-buffered operations are used to write single samples with known time increments between them and good latency.

Analog Output Triggering

Analog output supports two different triggering actions: start and pause. An analog or digital hardware trigger can initiate these actions. All S Series devices support digital triggering, and some also support analog triggering. To find your device's triggering options, refer to the specifications document for your device.

The *AO Start Trigger Signal* and *AO Pause Trigger Signal* sections contain information about the analog output trigger signals.

Refer to Chapter 12, *Triggering*, for more information about triggers.

Connecting Analog Output Signals

The AO signals are AO 0, AO 1, and AO GND. AO 0 is the voltage output signal for AO channel 0. AO 1 is the voltage output signal for AO channel 1. AO GND is the ground reference for the AO channels.

Figure 5-2 shows how AO 0 and AO 1 are wired on an S Series device.

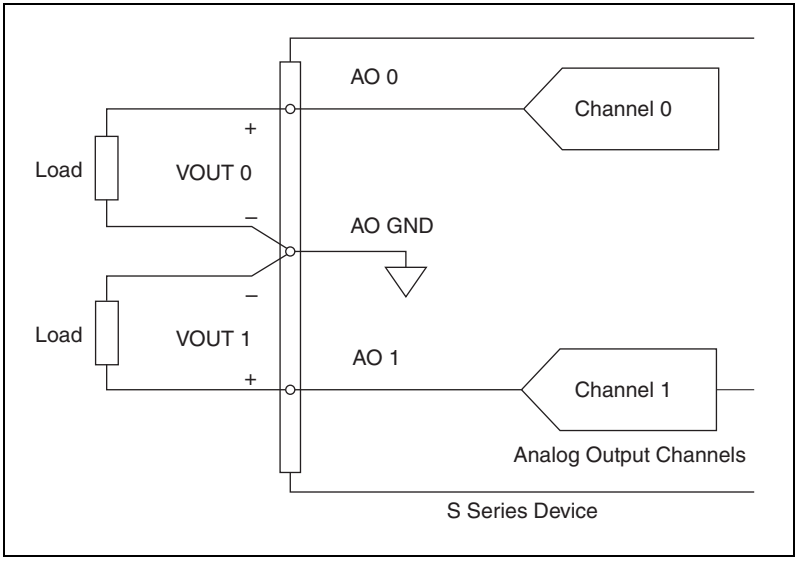


Figure 5-2. Analog Output Connections for S Series Devices

Waveform Generation Timing Signals

There is one AO Sample Clock that causes all AO channels to update simultaneously. Figure 5-3 summarizes the timing and routing options provided by the analog output timing engine.

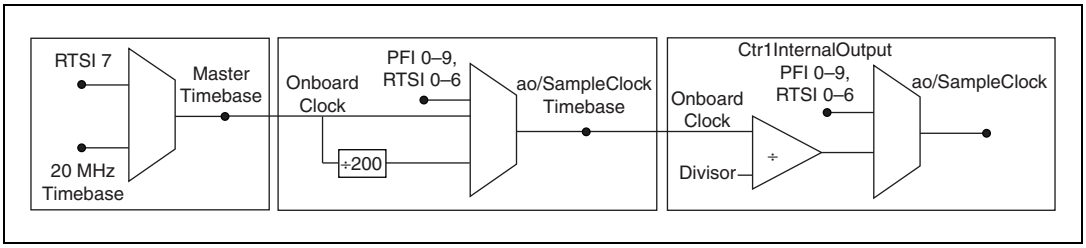


Figure 5-3. Analog Output Engine Routing Options

S Series devices feature the following waveform generation timing signals:

- *AO Start Trigger Signal*
- *AO Sample Clock Timebase Signal*
- *AO Sample Clock Signal*
- *AO Pause Trigger Signal*
- *Master Timebase Signal*

AO Sample Clock Signal

You can use the AO Sample Clock (ao/SampleClock) signal to initiate AO samples. Each sample updates the outputs of all of the DACs.

The source of the AO Sample Clock signal can be internal or external. You can specify whether the DAC update begins on the rising edge or falling edge of the AO Sample Clock signal.

Using an Internal Source

By default, AO Sample Clock is created internally by dividing down the AO Sample Clock Timebase signal.

Several other internal signals can be routed to the sample clock. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an External Source

You can use a signal connected to any PFI or RTSI <0..6> pin as the source of AO Sample Clock. Figure 5-4 shows the timing requirements of the AO Sample Clock source.

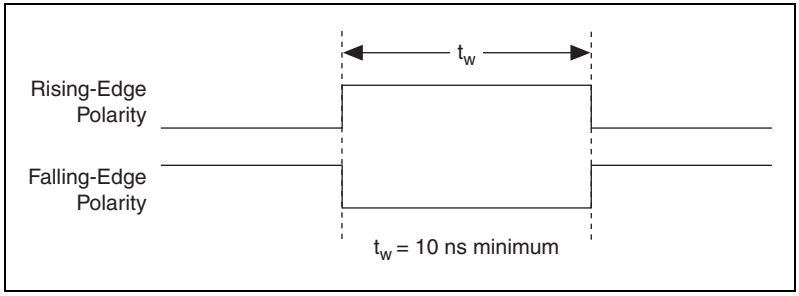


Figure 5-4. AO Sample Clock Timing Requirements

Outputting the AO Sample Clock Signal

You can configure the PFI 5/AO SAMP CLK pin to output the AO Sample Clock signal. The output pin reflects the AO Sample Clock signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 5-5 shows the timing behavior of the PFI 5/AO SAMP CLK pin when the pin is an output.

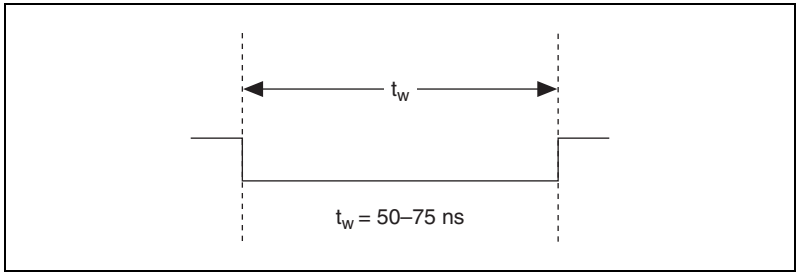


Figure 5-5. PFI 5/AO SAMP CLK as an Output

The PFI 5/AO SAMP CLK is configured as an input by default.

Other Timing Requirements

A counter on your device internally generates AO Sample Clock unless you select some external source. The AO Start Trigger signal starts this counter. It is stopped automatically by hardware after a finite acquisition completes or manually through software. When using an internally generated AO Sample Clock in NI-DAQmx, you can also specify a configurable delay from the AO Start Trigger to the first AO Sample Clock pulse. By default, this delay is two ticks of the AO Sample Clock Timebase signal.

Figure 5-6 shows the relationship of the AO Sample Clock signal to the AO Start Trigger signal.

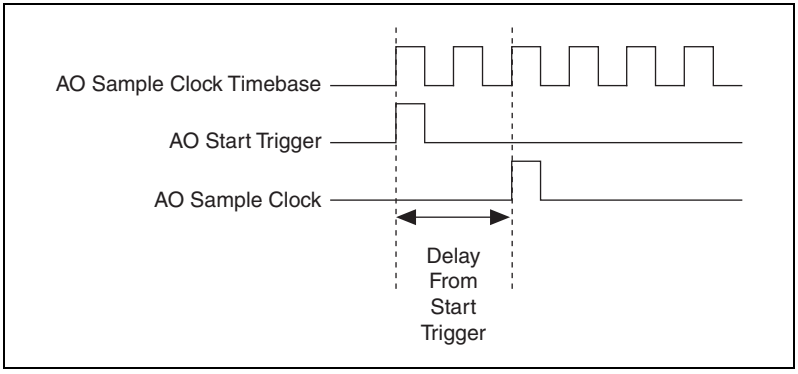


Figure 5-6. AO Sample Clock and AO Start Trigger

AO Sample Clock Timebase Signal

You can select any PFI or RTSI pin as well as many other internal signals as the AO Sample Clock Timebase (ao/SampleClockTimebase) signal. This signal is not available as an output on the I/O connector. AO Sample Clock Timebase is divided down to provide the Onboard Clock source for the AO Sample Clock. You specify whether the samples begin on the rising or falling edge of AO Sample Clock Timebase.

You might use the AO Sample Clock Timebase signal if you want to use an external sample clock signal, but need to divide the signal down. If you want to use an external sample clock signal, but do not need to divide the signal, then you should use the AO Sample Clock signal rather than the AO Sample Clock Timebase. If you do not specify an external sample clock timebase, NI-DAQmx uses the Onboard Clock.

Figure 5-7 shows the timing requirements for the AO Sample Clock Timebase signal.

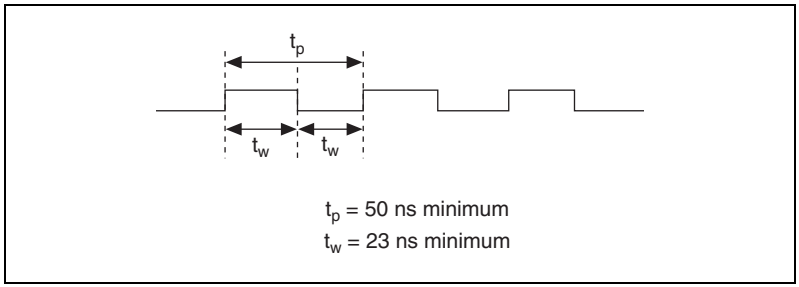


Figure 5-7. AO Sample Clock Timebase Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

Unless you select an external source, either the 20MHzTimebase or 100kHzTimebase generates the AO Sample Clock Timebase signal.

AO Start Trigger Signal

You can use the AO Start Trigger (ao/StartTrigger) signal to initiate a waveform generation. If you do not use triggers, you begin a generation with a software command.

Using a Digital Source

To use AO Start Trigger, specify a source and an edge. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Figure 5-8 shows the timing requirements of the AO Start Trigger digital source.

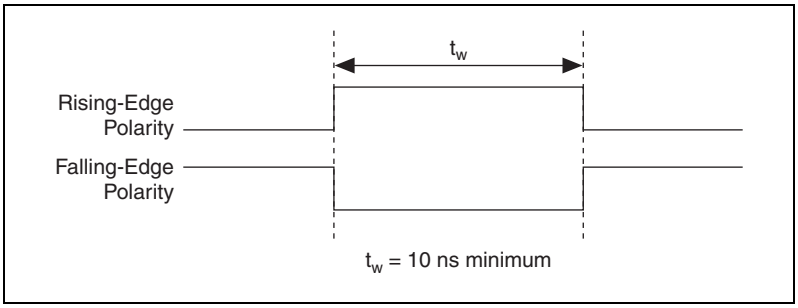


Figure 5-8. AO Start Trigger Timing Requirements

Using an Analog Source

When you use an analog trigger source, the waveform generation begins on the first rising edge of the Analog Comparison Event signal. For more information, refer to the *Triggering with an Analog Source* section of Chapter 12, *Triggering*.

Outputting the AO Start Trigger Signal

You can configure the PFI 6/AO START TRIG pin to output the AO Start Trigger signal. The output pin reflects the AO Start Trigger signal regardless of what signal you specify as its source.

The output is an active high pulse. Figure 5-9 shows the timing behavior of the PFI 6/AO START TRIG pin when the pin is an output.

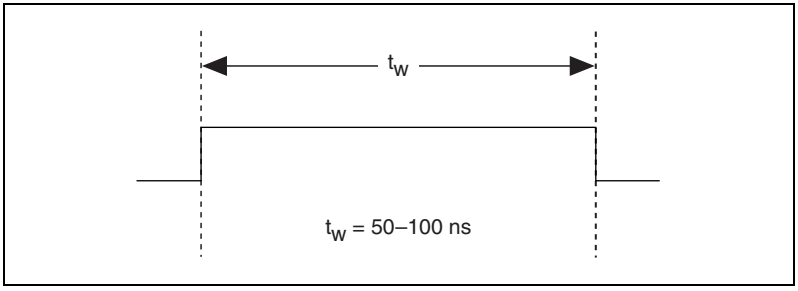


Figure 5-9. PFI 6/AO START TRIG Timing Behavior

The PFI 6/AO START TRIG pin is configured as an input by default.

AO Pause Trigger Signal

You can use the AO Pause Trigger (ao/PauseTrigger) signal to mask off samples in a DAQ sequence. That is, when AO Pause Trigger is active, no samples occur.

The AO Pause Trigger does not stop a sample that is in progress. The pause does not take effect until the beginning of the next sample. This signal is not available as an output.

Using a Digital Source

To use AO Pause Trigger, specify a source and a polarity. The source can be an external signal connected to any PFI or RTSI <0..6> pin. The source can also be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Also, specify whether the samples are paused when AO Pause Trigger is at a logic high or low level.

Using an Analog Source

When you use an analog trigger source, the samples are paused when the Analog Comparison Event signal is at a high level. For more information, refer to the *Triggering with an Analog Source* section of Chapter 12, *Triggering*.

Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the device are derived. It controls the timing for the analog input, analog output, and counter subsystems. The Master Timebase signal is available as an output on the I/O connector, but you must use at least one counter to output it.

The maximum allowed frequency for the Master Timebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the Master Timebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the Master Timebase unless you want to synchronize multiple devices, in which case, you should use RTSI 7. Refer

to Chapter 10, *Real-Time System Integration Bus (RTSI)*, for more information about which signals are available through RTSI.

Figure 5-10 shows the timing requirements for Master Timebase.

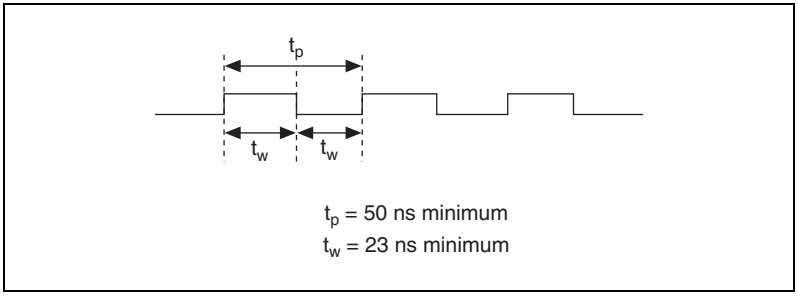


Figure 5-10. Master Timebase Timing Requirements

Getting Started with AO Applications in Software

You can use the S Series device in the following analog output applications:

- Single-point generation
- Finite generation
- Continuous generation
- Waveform generation

You can perform these generations through DMA, interrupt, or programmed I/O data transfer mechanisms. Some of the applications also use start triggers and pause triggers.

Note For more information about programming analog output applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

6

Digital I/O

S Series devices contain eight lines of bidirectional DIO signals that support the following features:

- Direction and function of each terminal, individually controllable
- **(NI 6115/612*x*/613*x* Only)** High-speed digital waveform generation
- **(NI 6115/612*x*/613*x* Only)** High-speed digital waveform acquisition

Figure 6-1 shows the circuitry of one DIO line.

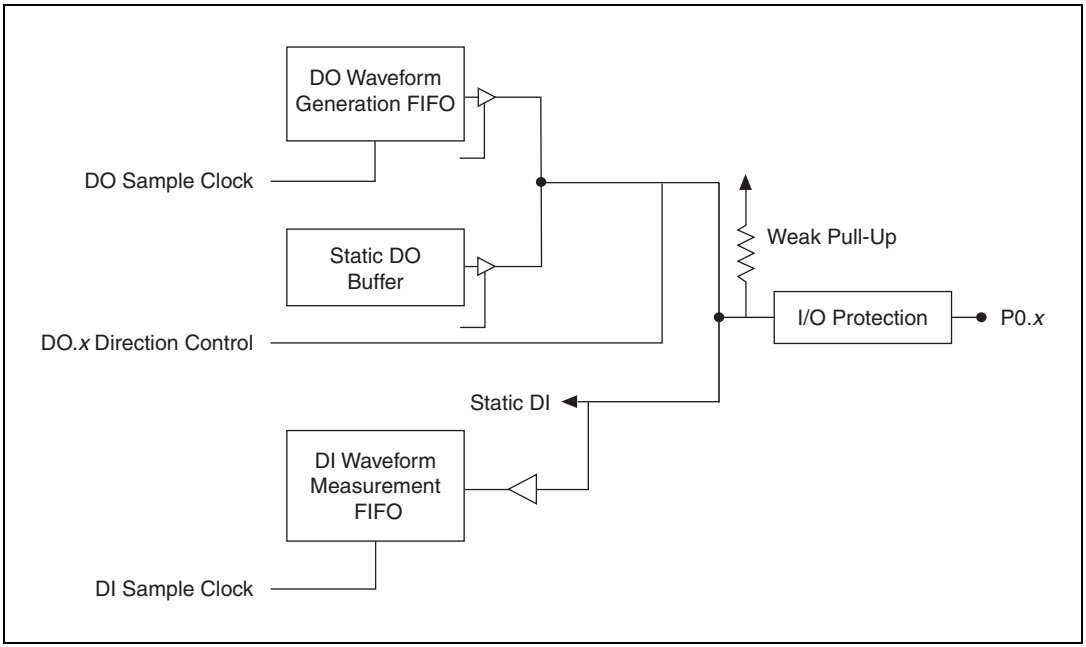


Figure 6-1. S Series Digital I/O Block Diagram

The DIO terminals are named P0.<0..7> on the I/O connector.

Static DIO

Each DIO line can be used as a static DI or DO line. You can use static DIO lines to monitor or control digital signals. Each DIO can be individually configured as a digital input (DI) or digital output (DO). All samples of static DI lines and updates of DO lines are software-timed.

P0.6 and P0.7 also can control the up/down input of general-purpose counters 0 and 1, respectively. The up/down control signals, Counter 0 Up/Down and Counter 1 Up/Down, are input-only and do not affect the operation of the DIO lines. For more information, refer to Chapter 7, *Counters*.

Digital Waveform Generation

(NI 6115/612*x*/613*x* Only) These S Series devices can generate digital waveforms. This behavior is also referred to as correlated digital I/O because there is no dedicated clock source for the digital operation. Refer to the *DO Sample Clock Signal* section for a list of possible sources.

The DO waveform generation FIFO stores the digital samples. These S Series devices can use DMA transfers to move data from the system memory to the DO waveform generation FIFO. The DAQ device moves samples from the FIFO to the DIO terminals on each rising or falling edge of a clock signal, DO Sample Clock. Refer to Chapter 11, *Bus Interface*, for more information about DMA transfers.

You can configure each DIO line to be the following:

- An input
- A static output
- A digital waveform generation output

DO Sample Clock Signal

(NI 6115/612*x*/613*x* Only) Use the DO Sample Clock (do/SampleClock) signal to update the DO pins with the next sample from the DO waveform generation FIFO. Because there is no dedicated internal clock for timed digital operations, you can use an external signal or one of several internal signals as the DO Sample Clock. You can correlate digital and analog samples in time by choosing the same signal as the source of the DO Sample Clock, AI Sample Clock, or DI Sample Clock.

If the DAQ device receives a DO Sample Clock when the FIFO is empty, the DAQ device reports an underflow error to the host software.

Using an Internal Source

To use DO Sample Clock with an internal source without making any external connections, specify the signal source and the polarity of the signal. The source can be one of the following signals:

- AI Sample Clock
- **(NI 6115/6120 Only)** AO Sample Clock
- Counter 0 Out

Program the DAQ device to update the DIO pins on the rising edge or falling edge of DO Sample Clock.

Using an External Source

You can use a signal connected to any RTSI <0..6> pin as the source of DO Sample Clock. You can generate samples on the rising or falling edge of DO Sample Clock.

Any PFI line that can be routed to RTSI can also be used as the clock source. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You must ensure that the time between two active edges of the DO Sample Clock is not too short. If the time is too short, the DO waveform generation FIFO is not able to read the next sample fast enough. Refer to the device specifications for the maximum sampling rate for your device.

Digital Waveform Acquisition

(NI 6115/612*x*/613*x* Only) These S Series devices can acquire digital waveforms. This behavior is also referred to as correlated digital I/O because there is no dedicated clock source for the digital operation. Refer to the *DI Sample Clock Signal* section for a list of possible sources.

The DI waveform acquisition FIFO stores the digital samples. These S Series devices can use DMA transfers to move data from the DI waveform acquisition FIFO to system memory. The DAQ device samples the DIO lines on each rising or falling edge of a clock signal, DI Sample Clock. Refer to Chapter 11, *Bus Interface*, for more information about DMA transfers.

You can configure each DIO line to be the following:

- An output
- A static input
- A digital waveform acquisition input

DI Sample Clock Signal

(NI 6115/612*x*/613*x* Only) Use the DI Sample Clock (di/SampleClock) signal to sample the P0.<0..7> terminals and store the result in the DI waveform acquisition FIFO. Because there is no dedicated internal clock for timed digital operations, you can use an external signal or one of several internal signals as the DI Sample Clock. You can correlate digital and analog samples in time by choosing the same signal as the source of the DI Sample Clock, AI Sample Clock, or DO Sample Clock.

If the DAQ device receives a DI Sample Clock when the FIFO is full, the DAQ device reports an overflow error to the host software.

Using an Internal Source

To use DI Sample Clock with an internal source, specify the signal source and the polarity of the signal. The source can be any of the following signals:

- AI Sample Clock
- **(NI 6115/6120 Only)** AO Sample Clock
- Counter 0 Out

Program the DAQ device to sample the DIO terminals on the rising edge or falling edge of DI Sample Clock.

Using an External Source

You can use a signal connected to any RTSI <0..6> pin as the source of DI Sample Clock. You can sample data on the rising or falling edge of DI Sample Clock.

Any PFI line that can be routed to RTSI can also be used as the clock source. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You must ensure that the time between two active edges of the DI Sample Clock is not too short. If the time is too short, the DI waveform generation FIFO is not able to store the sample fast enough. Refer to the device specifications for the maximum sampling rate for your device.

I/O Protection

Each DIO and PFI signal is protected against overvoltage, undervoltage, and overcurrent conditions as well as ESD events. However, you should avoid these fault conditions by following these guidelines:

- If you configure a PFI or DIO line as an output, do not connect it to any external signal source, ground signal, or power supply.
- If you configure a PFI or DIO line as an output, understand the current requirements of the load connected to these signals. Do not exceed the specified current output limits of the DAQ device. NI has several signal conditioning solutions for digital applications requiring high-current drive.
- If you configure a PFI or DIO line as an input, do not drive the line with voltages outside of its normal operating range. The PFI or DIO lines have a smaller operating range than the AI signals.
- Treat the DAQ device as you would treat any static-sensitive device. Always properly ground yourself and the equipment when handling the DAQ device or connecting to it.

Power-On States

At system startup and reset, the hardware sets all PFI and DIO lines to high-impedance inputs. The DAQ device does not drive the signal high or low. Each line has a weak pull-up resistor connected to it, as described in the specifications document for your device.

Connecting Digital I/O Signals

The DIO signals, P0.<0..7>, are referenced to D GND. You can individually program each line as an input or output. Figure 6-2 shows P0.<0..3> configured for digital input and P0.<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in Figure 6-2.

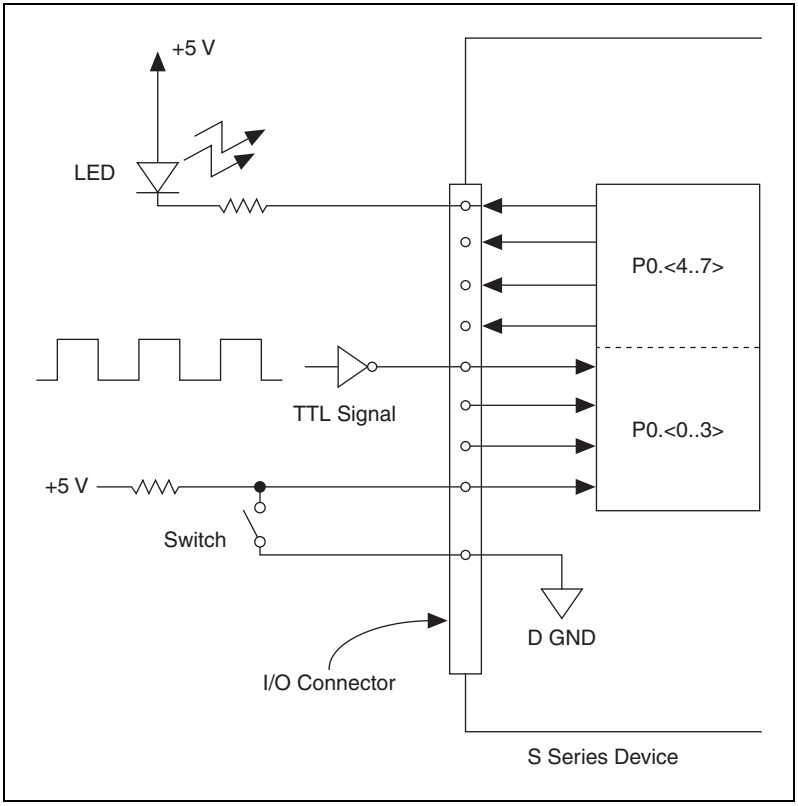


Figure 6-2. Digital I/O Signal Connections

Caution Exceeding the maximum input voltage ratings, which are listed in the specifications document for each S Series device, can damage the DAQ device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Getting Started with DIO Applications in Software

You can use the S Series device in the following digital I/O applications:

- Static digital input
- Static digital output
- Digital waveform generation
- Digital waveform acquisition

Note For more information about programming digital I/O applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

7

Counters

Figure 7-1 shows a counter on the S Series device.

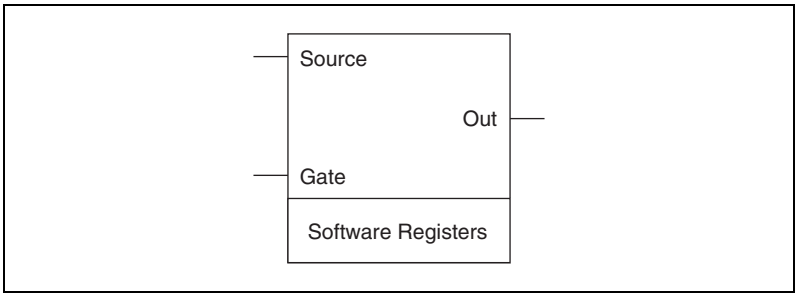


Figure 7-1. Counter Block Diagram

Counters 0 and 1 each have two inputs (source and gate), one output, and two software registers, which are used to perform different operations. Counter functionality for S Series devices is built into the DAQ-STC. For more information about the DAQ-STC, refer to Chapter 2, *DAQ System Overview*.

Counter Triggering

Counters support two different triggering actions: start and pause. A digital trigger can directly initiate these actions. An analog trigger can indirectly initiate these actions by routing the Analog Comparison Event from a triggered analog input or output task to the counter as a digital trigger.

Refer to Chapter 12, *Triggering*, for more information about triggers.

Start Trigger

A start trigger begins a finite or continuous pulse generation. After a continuous generation is initiated, the pulses continue to generate until you stop the operation in software. The specified number of pulses are generated for finite generations unless the retriggerable attribute is used. The retriggerable attribute causes the generation to restart on a subsequent start trigger.

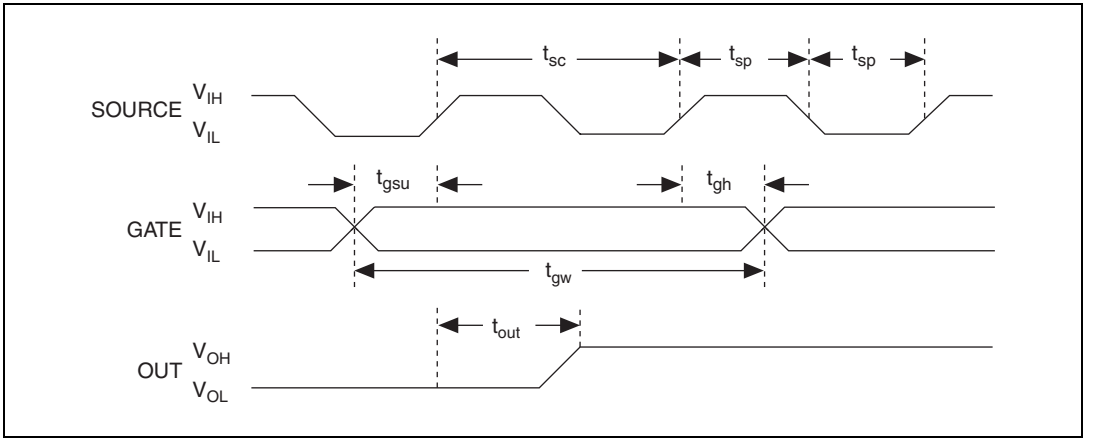
Pause Trigger

You can use pause triggers in edge counting and continuous pulse generation applications:

- For edge counting acquisitions, the counter stops counting edges while the external trigger signal is low and resumes when the signal goes high, or vice versa.
- For continuous pulse generations, the counter stops generating pulses while the external trigger signal is low and resumes when the signal goes high, or vice versa.

Counter Timing Signals

Figure 7-2 shows the timing requirements for the gate and source input signals and the timing specifications for the output signals on your device.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	10 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 7-2. Gate and Source Input Timing Requirements

The gate and out signal transitions shown in Figure 7-2 are referenced to the rising edge of the source signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, applies when you program the counter to count falling edges.

The gate input timing parameters are referenced to the signal at the source input or to one of the internally generated signals on your device. Figure 7-2 shows the gate signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal so the gate can take effect at that source edge, as shown by t_{gsu} and t_{gh}. The gate signal is not required after the active edge of the source signal.

If you use an internal timebase clock, you cannot synchronize the gate signal with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The output timing parameters are referenced to the signal at the source input or to one of the internally generated clock signals on your device. Figure 7-2 shows the out signal referenced to the rising edge of a source signal. Any out signal state changes occur within 80 ns after the rising or falling edge of the source signal.

For information about the internal routing available on the DAQ-STC counter/timers, refer to *Counter Parts in NI-DAQmx* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

S Series devices feature the following counter timing signals:

- *Counter 0 Source Signal*
- *Counter 0 Gate Signal*
- *Counter 0 Internal Output Signal*
- *Counter 0 Up/Down Signal*
- *Counter 1 Source Signal*
- *Counter 1 Gate Signal*
- *Counter 1 Internal Output Signal*
- *Counter 1 Up/Down Signal*
- *Frequency Output Signal*
- *Master Timebase Signal*

Counter 0 Source Signal

You can select any PFI as well as many other internal signals as the Counter 0 Source (Ctr0Source) signal. The Counter 0 Source signal is configured in edge-detection mode on either the rising or falling edge. The selected edge of the Counter 0 Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Counter 0 Source signal to the PFI 8/CTR 0 SOURCE pin, even if another PFI is inputting the Counter 0 Source signal. This output is set to high-impedance at startup.

Figure 7-3 shows the timing requirements for the Counter 0 Source signal.

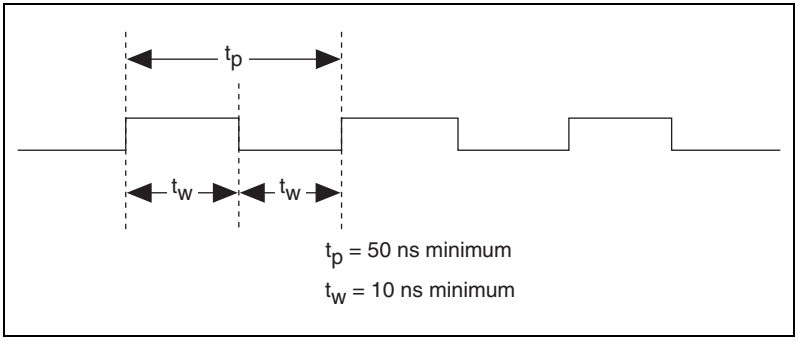


Figure 7-3. Counter 0 Source Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

For most applications, unless you select an external source, the 20MHzTimebase signal or the 100kHzTimebase signal generates the Counter 0 Source signal.

Counter 0 Gate Signal

You can select any PFI as well as many other internal signals like the Counter 0 Gate (Ctr0Gate) signal. The Counter 0 Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents.

You can export the gate signal connected to Counter 0 to the PFI 9/CTR 0 GATE pin, even if another PFI is inputting the Counter 0 Gate signal. This output is set to high-impedance at startup.

Figure 7-4 shows the timing requirements for the Counter 0 Gate signal.

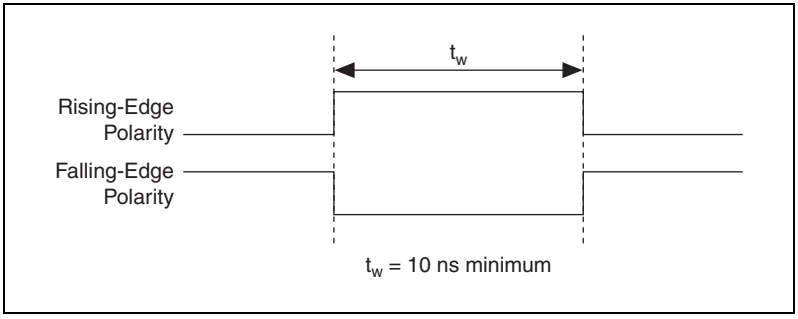


Figure 7-4. Counter 0 Gate Timing Requirements

Counter 0 Internal Output Signal

The Counter 0 Internal Output (Ctr0InternalOutput) signal is the output of Counter 0. This signal reflects the terminal count (TC) of Counter 0. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. Figure 7-5 shows the behavior of the Counter 0 Internal Output signal.

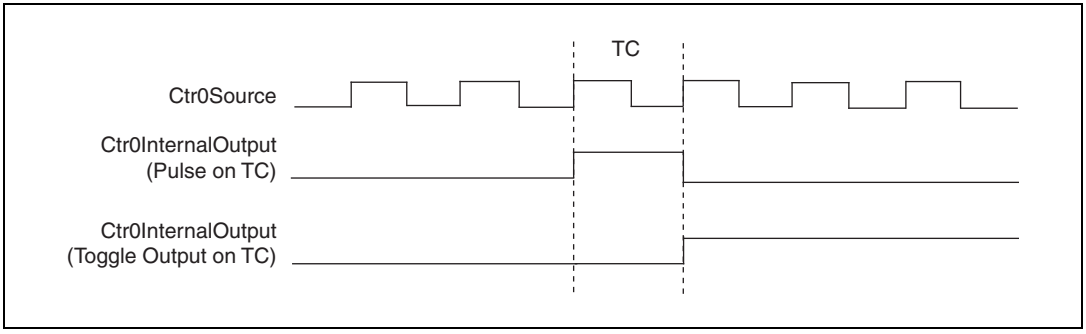


Figure 7-5. Counter 0 Internal Output Signal Behavior

You can use Counter 0 Internal Output in the following applications:

- In pulse generation mode, the counter drives Counter 0 Internal Output with the generated pulses. To enable this behavior, software configures the counter to toggle Counter 0 Internal Output on TC.

- Counter 0 Internal Output can control the timing of analog input acquisitions by driving:
  - AI Sample Clock
  - AI Start Trigger
  - AI Convert Clock
- Counter 0 and 1 can be daisy-chained together by routing Counter 0 Internal Output to Counter 1 Gate.
- Counter 0 Internal Output can drive any of the RTSI <0..6> signals to control the behavior of other devices in the system.
- Counter 0 Internal Output drives the CTR 0 OUT pin to trigger or control external devices.
- Counter 0 Internal Output can drive other internal signals.

Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

CTR 0 OUT Pin

When the CTR 0 OUT pin is an output, the Ctr0InternalOutput signal drives the pin. As an input, CTR 0 OUT can drive any of the RTSI <0..6> signals. CTR 0 OUT is set to high-impedance at startup. Figure 7-6 shows the relationship of CTR 0 OUT and Ctr0InternalOutput.

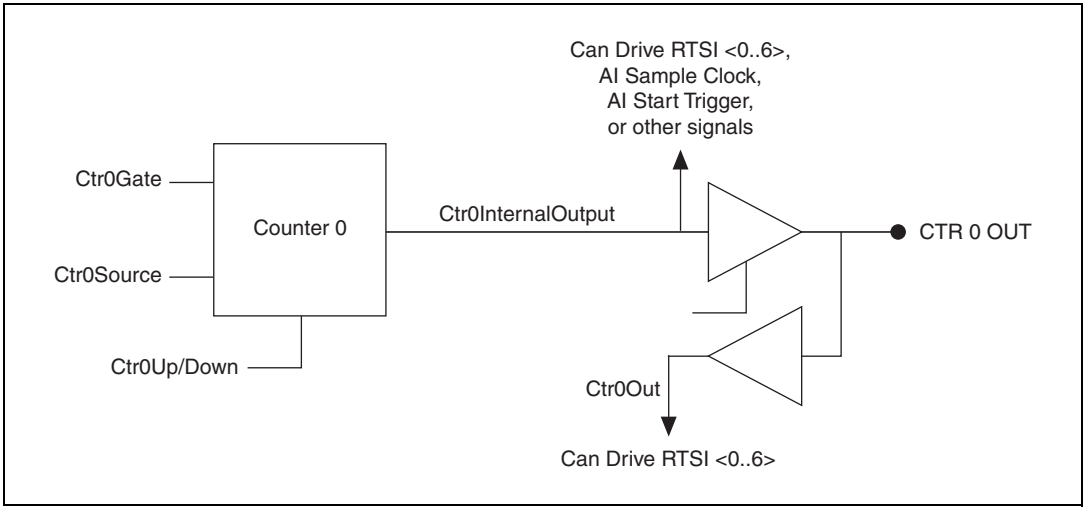


Figure 7-6. CTR 0 OUT and Ctr0InternalOutput

Counter 0 Up/Down Signal

You can externally input this signal on the P0.6 pin, but it is not available as an output on the I/O connector. When you enable externally controlled count direction, Counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. If you are using an external signal to control the count direction, do not use the P0.6 pin for output. If you do not enable externally controlled count direction, the P0.6 pin is free for general use.

Counter 1 Source Signal

You can select any PFI as well as many other internal signals as the Counter 1 Source (Ctr1Source) signal. The Counter 1 Source signal is configured in edge-detection mode on either rising or falling edge. The selected edge of the Counter 1 Source signal increments and decrements the counter value depending on the application the counter is performing.

You can export the Counter 1 signal to the PFI 3/CTR 1 SOURCE pin, even if another PFI is inputting the Counter 1 Source signal. This output is set to high-impedance at startup.

Figure 7-7 shows the timing requirements for the Counter 1 Source signal.

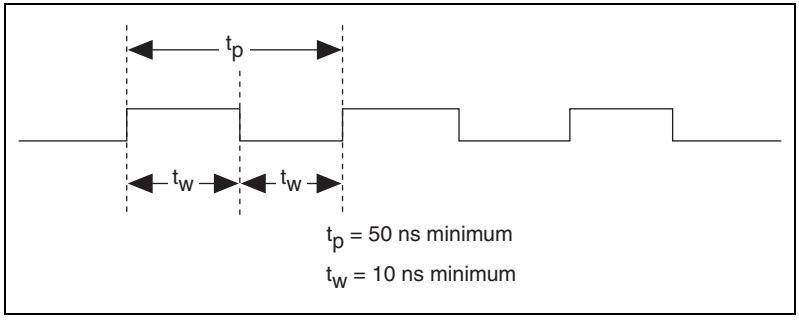


Figure 7-7. Counter 1 Source Timing Requirements

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

For most applications, unless you select an external source, the 20MHzTimebase signal or the 100kHzTimebase signal generates the Counter 1 Source signal.

Counter 1 Gate Signal

You can select any PFI as well as many other internal signals like the Counter 1 Gate (Ctr1Gate) signal. The Counter 1 Gate signal is configured in edge-detection or level-detection mode depending on the application performed by the counter. The gate signal can perform many different operations including starting and stopping the counter, generating interrupts, and saving the counter contents.

You can export the gate signal connected to Counter 1 to the PFI 4/CTR 1 GATE pin, even if another PFI is inputting the Counter 1 Gate signal. This output is set to high-impedance at startup.

Figure 7-8 shows the timing requirements for the Counter 1 Gate signal.

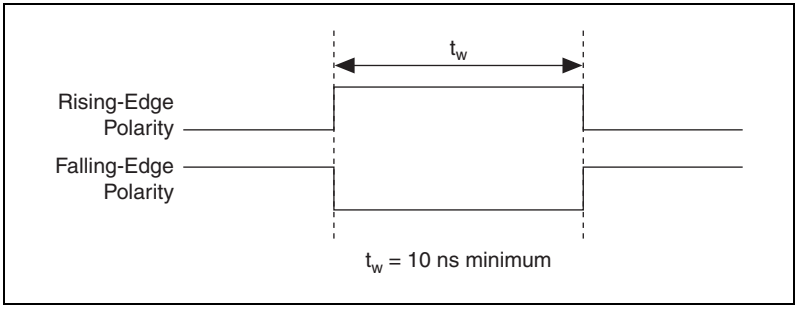


Figure 7-8. Counter 1 Gate Timing Requirements

Counter 1 Internal Output Signal

The Counter 1 Internal Output (Ctr0InternalOutput) signal is the output of Counter 1. This signal reflects the terminal count (TC) of Counter 1. The counter generates a terminal count when its count value rolls over. The two software-selectable output options are pulse on TC and toggle output

polarity on TC. The output polarity is software-selectable for both options. Figure 7-9 shows the behavior of the Counter 1 Internal Output signal.

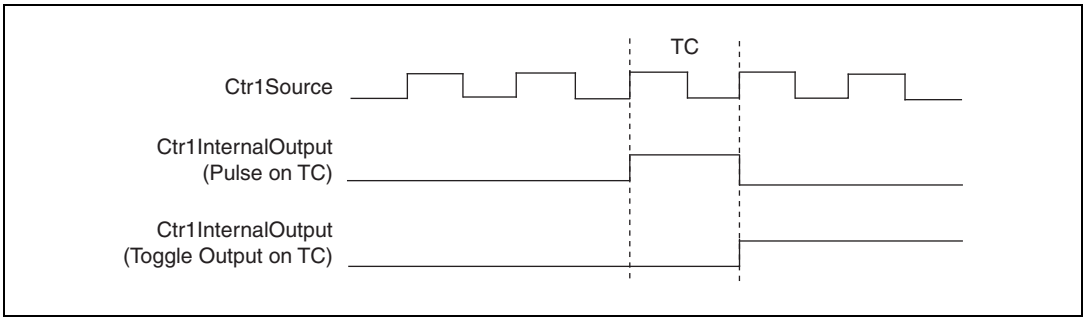


Figure 7-9. Counter 1 Internal Output Behavior

You can use Counter 1 Internal Output in the following applications:

- In pulse generation mode, the counter drives Counter 1 Internal Output with the generated pulses. To enable this behavior, software configures the counter to toggle Counter 1 Internal Output on TC.
- **(NI 6110/6111 Only)** Counter 1 Internal Output can control the timing of analog output acquisitions by driving AO Sample Clock.
- Counter 0 and 1 can be daisy-chained together by routing Counter 1 Internal Output to Counter 0 Gate.
- Counter 1 Internal Output drives the CTR 1 OUT pin to trigger or control external devices.
- Counter 1 Internal Output can drive other internal signals.

Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Counter 1 Up/Down Signal

You can externally input this signal on the P0.7 pin, but it is not available as an output on the I/O connector. When you enable externally controlled count direction, Counter 1 counts down when this pin is at a logic low and counts up when it is at a logic high. If you do not enable externally controlled count direction, the P0.7 pin is free for general use.

Frequency Output Signal

The frequency generator is a four-bit counter that can divide the output timebase by a number you select from 1 to 16. The frequency output signal (FREQ OUT) can be software-selectable from the internal 10 MHz and 100 kHz timebases.

This signal is available at any PFI <0..9> or RTSI <0..7> terminal. The frequency output signal also can be routed to DO Sample Clock and DI Sample Clock.

Master Timebase Signal

The Master Timebase (MasterTimebase) signal, or Onboard Clock, is the timebase from which all other internally generated clocks and timebases on the device are derived. It controls the timing for the analog input, analog output, and counter subsystems. It is available as an output on the I/O connector, but you must use one or more counters to do so.

The maximum allowed frequency for the Master Timebase is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The two possible sources for the Master Timebase signal are the internal 20MHzTimebase signal or an external signal through RTSI 7. Typically the 20MHzTimebase signal is used as the Master Timebase unless you wish to synchronize multiple devices, in which case, you should use RTSI 7. Refer to Chapter 10, *Real-Time System Integration Bus (RTSI)*, for more information about which signals are available through RTSI.

Figure 7-10 shows the timing requirements for Master Timebase.

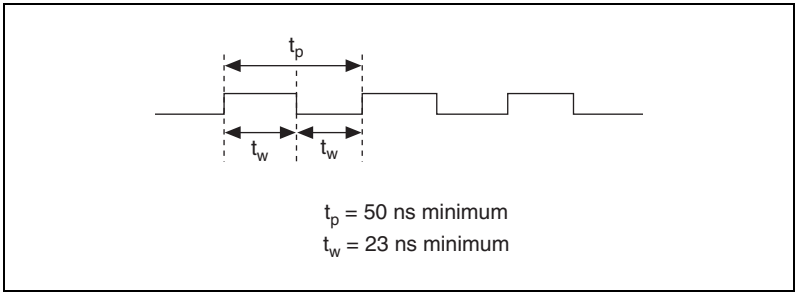


Figure 7-10. Master Timebase Timing Requirements

Getting Started with Counter Applications in Software

You can use the S Series device in the following counter-based applications:

- Counting edges
- Frequency measurement
- Period measurement
- Pulse width measurement
- Semi-period measurement
- Pulse generation

You can perform these measurements through DMA, interrupt, or programmed I/O data transfer mechanisms. The measurements can be finite or continuous in duration. Some of the applications also use start triggers and pause triggers.

Note For more information about programming counter applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

8

Programmable Function Interfaces (PFI)

The 10 Programmable Function Interface (PFI) pins allow timing signals to be routed to and from the I/O connector of a device.

PFI Inputs

An external timing signal can be input on any PFI pin and multiple timing signals can simultaneously use the same PFI pin. This flexible routing scheme reduces the need to change the physical connections to the I/O connector for different applications. Refer to the *Timing Signal Routing* section of Chapter 9, *Digital Routing*, for more information.

When using the PFI pin as an input, you can individually configure each PFI for edge or level detection and for polarity selection. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse width requirements imposed by the PFI signals, but there can be limits imposed by the particular timing signal being controlled.

PFI Outputs

You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need the Counter 0 Source signal as an output on the I/O connector, software can turn on the output driver for the PFI 8/CTR 0 SRC pin. This signal, however, cannot be output on any other PFI pin.

Not all timing signals can be output. PFI pins are labeled with the timing signal that can be output on it. For example, PFI 8 is labeled PFI 8/CTR 0 SRC. The timing signals that can be output on PFI pins are as follows:

- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Sample Clock Signal
- AO Start Trigger Signal
- AO Sample Clock Signal
- Counter 0 Source Signal
- Counter 0 Gate Signal
- Counter 1 Source Signal
- Counter 1 Gate Signal

For more information about analog input signals, refer to Chapter 4, *Analog Input*. For more information about analog output signals, refer to Chapter 5, *Analog Output*. For more information about counter signals, refer to Chapter 7, *Counters*.

Caution Do *not* drive a PFI signal externally when it is configured as an output.

For more information about PFI lines on S Series devices, refer to the *Power-On States* section of Chapter 6, *Digital I/O*.

9

Digital Routing

The digital routing circuitry manages the flow of data between the bus interface and the acquisition subsystems (AI circuitry, AO circuitry, digital I/O, and the counters). The digital routing circuitry includes the DAQ-STC functionality and uses FIFOs (if present) in each subsystem to ensure efficient data movement.

The digital routing circuitry also routes timing and control signals. The acquisition subsystems use these signals to manage acquisitions. These signals can come from the following:

- Your S Series device
- Other devices in your system through RTSI
- User input through the PFI pins

You can see which routes are possible on your device in Measurement & Automation Explorer (MAX). In MAX, expand **Devices and Interfaces» NI-DAQmx Devices** in the configuration tree. Click your device to see information on the device resources, then click the **Device Routes** tab.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The S Series device uses the RTSI bus to interconnect timing signals between devices, and it uses the programmable function interface (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the S Series device to both control and be controlled by other devices and circuits.

You can control the following timing signals internal to the DAQ-STC by an external source:

- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Sample Clock Signal
- AI Pause Trigger Signal

- AI Sample Clock Timebase Signal
- AO Start Trigger Signal
- AO Sample Clock Signal
- AO Pause Trigger Signal
- AO Sample Clock Timebase Signal
- DI Sample Clock Signal
- DO Sample Clock Signal
- Counter 0 Source Signal
- Counter 0 Gate Signal
- Counter 0 Up/Down Signal
- Counter 1 Source Signal
- Counter 1 Gate Signal
- Counter 1 Up/Down Signal
- Master Timebase Signal

You also can control these timing signals by signals generated internally to the DAQ-STC, and these selections are fully software-configurable. Figure 9-1 shows an example of the signal routing multiplexer controlling the AI Sample Clock signal.

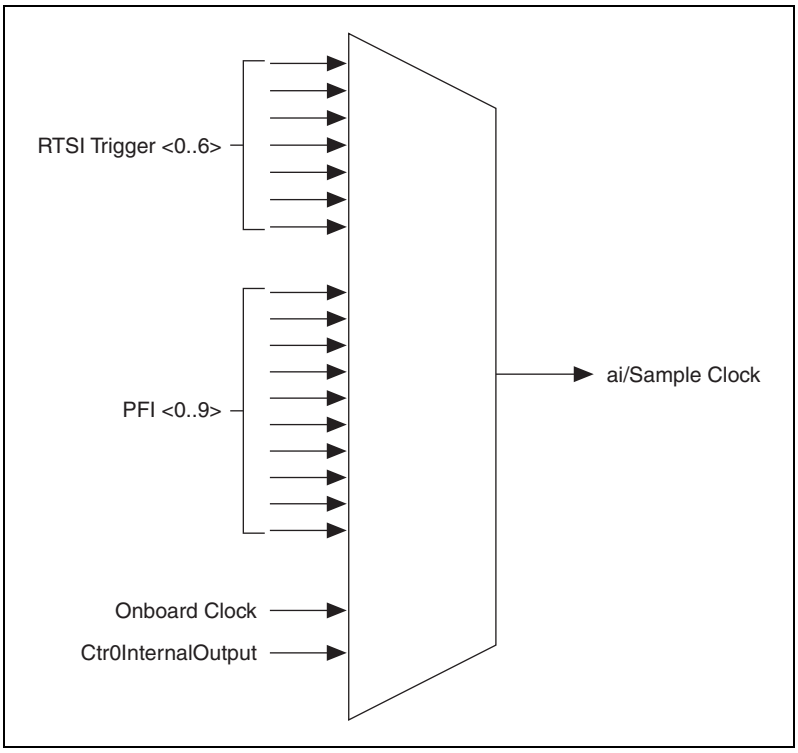


Figure 9-1. Signal Routing Multiplexer

Figure 9-1 shows that AI Sample Clock can be generated from a number of sources, including the external signals, RTSI <0..6> and PFI <0..9>, and the internal signals, Onboard Clock and Ctr0InternalOutput.

On PCI and PXI devices, many of these timing signals are also available as outputs on the PFI pins.

Note The Master Timebase signal can only be accepted as an external signal over RTSI. Refer to the *Device and RTSI Clocks* section of Chapter 10, *Real-Time System Integration Bus (RTSI)*, for information about routing this signal.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings, which are listed in the specifications document for each S Series device, can damage your device and the computer. NI is *not* liable for any damage resulting from such signal connections.

The 10 programmable function interface (PFI) pins labeled PFI <0..9> route all external control over the timing of the S Series device. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many analog input, waveform generation, and counter timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control all analog input, waveform generation, and counter timing signals.

All digital timing connections are referenced to D GND. Figure 9-2 shows this reference, and how to connect an external AI START TRIG source and an external AI SAMP CLK source to two PFI pins.

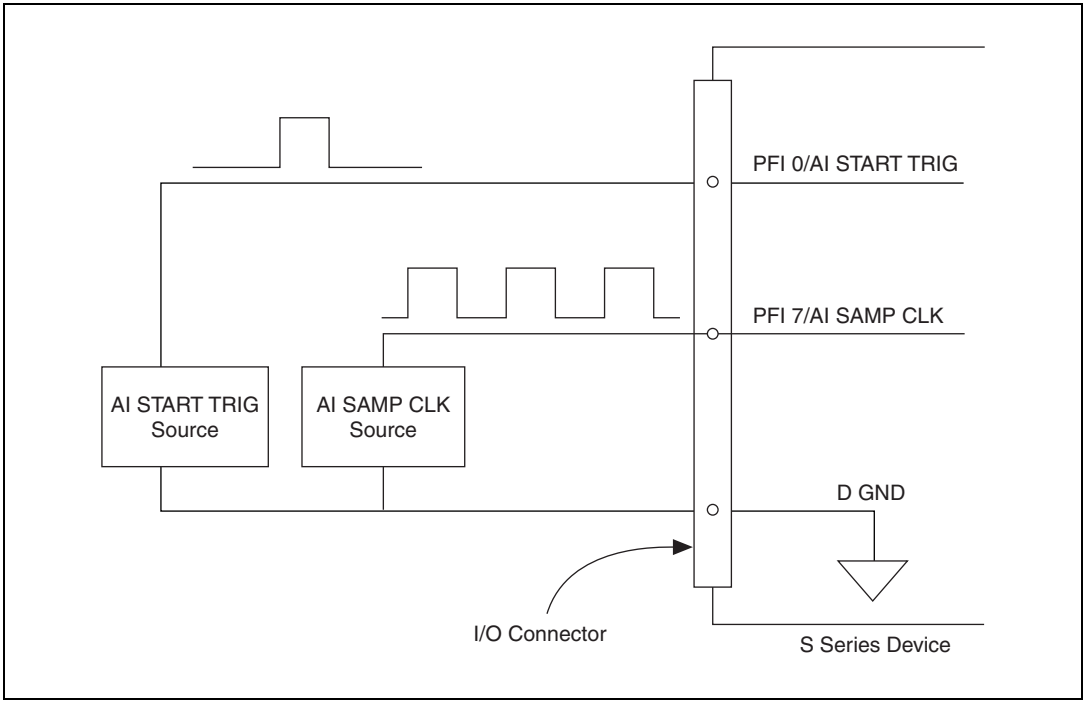


Figure 9-2. Connecting AI START TRIG and AI SAMP CLK to Two PFI Pins

Routing Signals in Software

Table 9-1 lists the basic functions you can use to route signals.

Table 9-1. Signal Routing in Software

Language	Program	Function
LabVIEW	NI-DAQmx	`DAQmx Export Signal.vi` and `DAQmx Connect Terminals.vi`
C	NI-DAQmx	`Export_Signal` and `DAQmx_Connect_Terminals`

Note For more information about routing signals in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

10

Real-Time System Integration Bus (RTSI)

NI-DAQmx devices use the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. In a PCI system, the RTSI bus consists of the RTSI bus interface and a ribbon cable. The bus can route timing and trigger signals between several functions on as many as five DAQ devices in the computer. In a PXI system, the RTSI bus consists of the RTSI bus interface and the PXI trigger signals on the PXI backplane. This bus can route timing and trigger signals between several functions on as many as seven DAQ devices in the system. For more information, refer to the KnowledgeBase document, *RTSI Connector Pinout*. Go to `ni.com/info` and enter the info code `rdrtsicp` to locate the KnowledgeBase.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any device sharing the RTSI bus. These bidirectional lines can drive or receive any of the timing and triggering signals shown below directly to or from the trigger bus.

In PCI, you can access RTSI <0..6> through the special RTSI ribbon cable. Figure 10-1 shows the PCI RTSI bus signal connection.

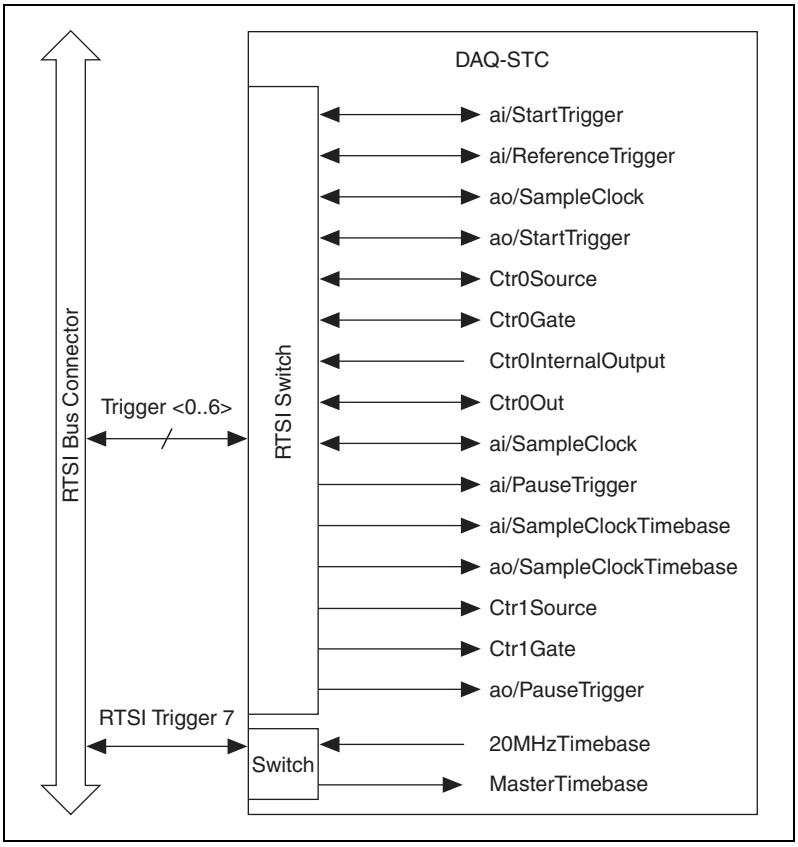


Figure 10-1. PCI RTSI Bus Signal Connection

With PXI S Series devices, RTSI <0..5> connects to PXI Trigger <0..5>, respectively, through the PXI bus on the PXI S Series device backplane. RTSI 6 connects to the PXI star trigger line, allowing the device to receive triggers from any star trigger controller plugged into Slot 2 of the chassis. For more information about the star trigger, refer to the *PXI Hardware Specification Revision 2.1*.

Figure 10-2 shows the PXI RTSI bus signal connection.

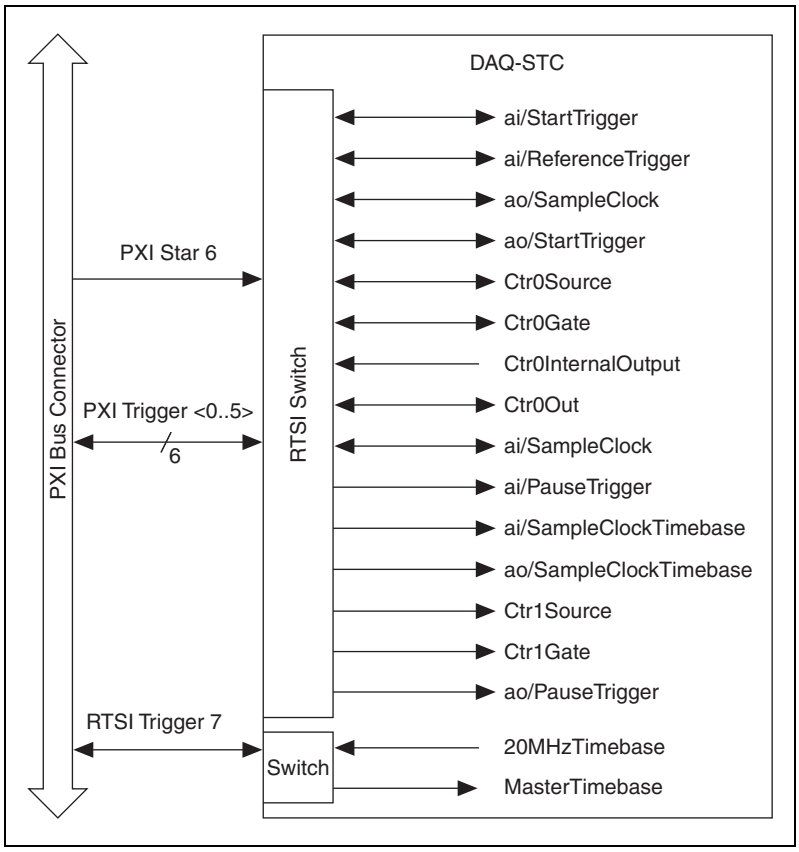


Figure 10-2. PXI RTSI Bus Signal Connection

Refer to the *Timing Signal Routing* section of Chapter 9, *Digital Routing*, for a description of the signals shown in the figures.

Device and RTSI Clocks

Many S Series device functions require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector. This timebase is also called the Master Timebase or Onboard Clock. Refer to the *Master Timebase Signal* section of Chapter 7, *Counters*, for more information.

Most S Series devices can use either their internal 20MHzTimebase signal or a timebase received over the RTSI bus. The timebase can only be routed to or received from RTSI 7, or the RTSI clock. The device uses this clock source, whether local or from the RTSI bus, as the primary frequency source. If you configure the device to use the internal timebase, you also can program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. The default configuration is to use the internal 20MHzTimebase signal without driving the timebase onto the RTSI bus.

Synchronizing Multiple Devices

With the RTSI bus and the routing capabilities of the DAQ-STC, there are several ways to synchronize multiple devices depending on your application. NI recommends that you use a common timebase as the Master Timebase signal and share any common triggers in the application. One device is designated as the master device and all other devices are designated as slave devices.

The 20MHzTimebase on the master device is the Master Timebase signal for all devices. The slave devices pull this signal from the master device across the RTSI trigger 7 line. Slave devices also pull any shared triggers across an available RTSI trigger line from the master device. When you start all of the slave devices before starting the master device, you have successfully synchronized your application across multiple devices.

11

Bus Interface

Each S Series device is designed on a complete hardware architecture that is deployed on the following platforms:

- PCI
- PXI

Using NI-DAQmx driver software, you have the flexibility to change hardware platforms and operating systems with little or no change to software code.

MITE and DAQ-PnP

PCI and PXI S Series devices use the MITE application-specific integrated circuit (ASIC) as a bus master interface to the PCI bus. PCI and PXI S Series devices are inherently Plug-and-Play (PnP) compatible. On all devices, the operating system automatically assigns the base address of the device.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1*. If you use a PXI-compatible plug-in module in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI interface on the S Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The PXI S Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. The PXI device is compatible with any CompactPCI chassis with a sub-bus that does not drive the lines used by that device. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and never enabled.

Caution Damage can result if these lines are driven by the sub-bus. NI is *not* liable for any damage resulting from improper signal connections.

Data Transfer Methods

There are three primary ways to transfer data across the PCI bus:

- **Direct Memory Access (DMA)**—DMA is a method to transfer data between the device and computer memory without the involvement of the CPU. This method makes DMA the fastest available data transfer method. National Instruments uses DMA hardware and software technology to achieve high throughput rates and to increase system utilization. DMA is the default method of data transfer for DAQ devices that support it.
- **Interrupt Request (IRQ)**—IRQ transfers rely on the CPU to service data transfer requests. The device notifies the CPU when it is ready to transfer data. The data transfer speed is tightly coupled to the rate at which the CPU can service the interrupt requests. If you are using interrupts to acquire data at a rate faster than the rate the CPU can service the interrupts, your systems may start to freeze.
- **Programmed I/O**—Programmed I/O is a data transfer mechanism where the user's program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on demand) operations.

Changing Data Transfer Methods between DMA and IRQ

There are a limited number of DMA channels per device (refer to the specifications document for your device). Each operation (specifically, AI, AO, and so on) that requires a DMA channel uses that method until all of the DMA channels are used. After all of the DMA channels are used, you will get an error if you try to run another operation requesting a DMA channel. If appropriate, you can change one of the operations to use interrupts. For NI-DAQmx, use the **Data Transfer Mechanism** property node.

12

Triggering

A trigger is a signal that causes a device to perform an action, such as starting an acquisition. You can program your DAQ device to generate triggers on any of the following:

- A software command
- A condition on an external digital signal
- A condition on an external analog signal

You can also program your DAQ device to perform an action in response to a trigger. The action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

For more information about analog input triggering, refer to Chapter 4, *Analog Input*. For more information about analog output triggering, refer to Chapter 5, *Analog Output*. For more information about counter triggering, refer to Chapter 7, *Counters*.

Note Not all S Series devices support analog triggering. For information about the triggering capabilities of your device, refer to the specifications document for your device.

Triggering with a Digital Source

S Series devices can generate a trigger on a digital signal. You must specify a source and an edge. The digital source can be any of the input PFIs or RTSI <0..6> signals.

The edge can be either the rising edge or falling edge of the digital signal. A rising edge is a transition from a low logic level to a high logic level. A falling edge is a high to low transition.

Figure 12-1 shows a falling-edge trigger.

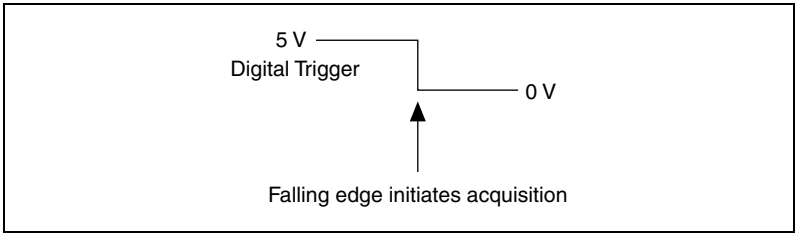


Figure 12-1. Falling-Edge Trigger

You can also program your DAQ device to perform an action in response to a trigger from a digital source. The action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

Triggering with an Analog Source

Some S Series devices can generate a trigger on an analog signal. Figure 12-2 shows the analog trigger circuitry.

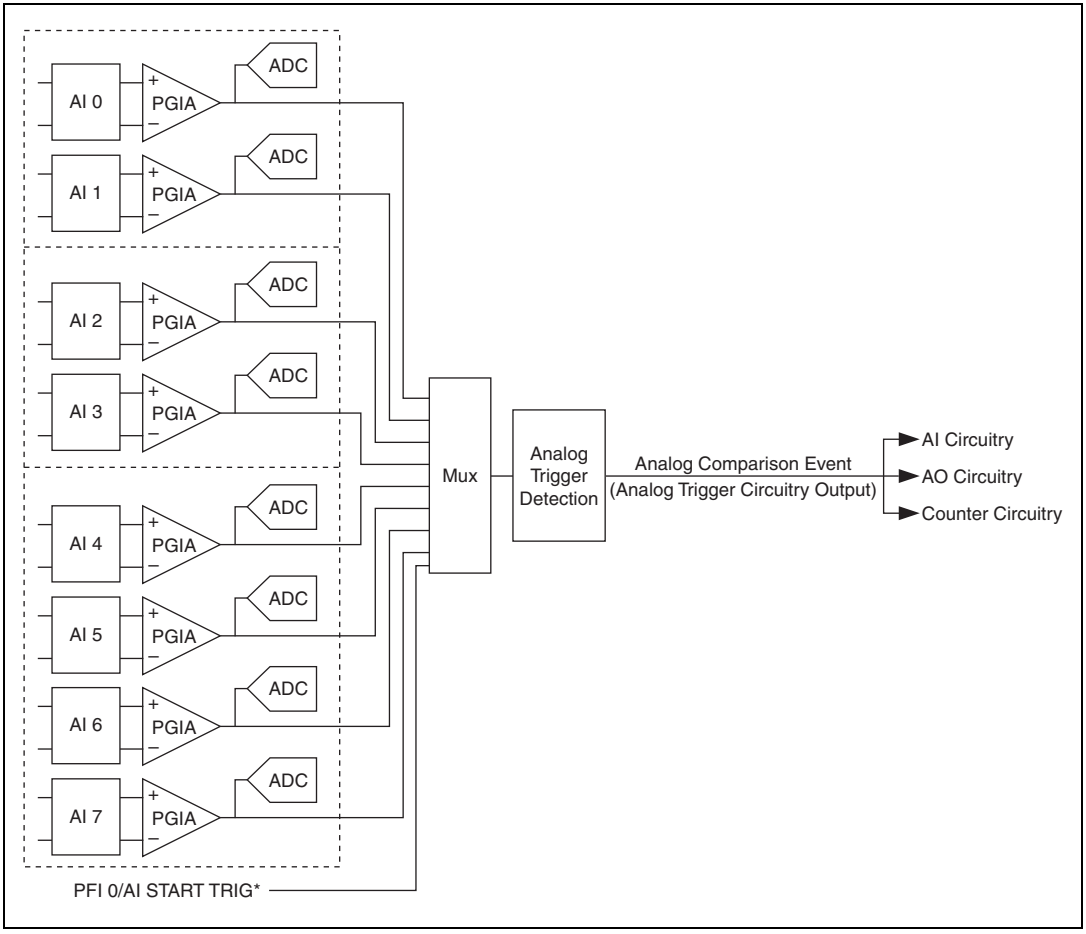


Figure 12-2. Analog Trigger Circuitry

You must specify a source and an analog trigger type. The source can be any analog input channel. On NI 611*x*/6120 devices, the source can also be the PFI 0/AI START TRIG pin.

PFI 0/AI START TRIG Pin

(NI 611*x*/6120 Only) This pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, resulting in false triggering when the pin is unconnected. To avoid false triggering, ensure that this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input using the application software.

Analog Input Channel

You can select any analog input channel to drive the instrumentation amplifier. The instrumentation amplifier amplifies the signal as determined by the input mode and the input polarity and range. The output of the instrumentation amplifier then drives the analog trigger detection circuit. By using the instrumentation amplifier, you can trigger on very small voltage changes in the input signal. For more information, refer to the *Analog Trigger Accuracy* section.

Analog Trigger Actions

The output of the Analog Trigger Detection circuit is the Analog Comparison Event signal. You can program your S Series device to perform an action in response to the Analog Comparison Event signal. The action can affect the following:

- Analog input acquisitions
- Analog output generation
- Counter behavior

Note Refer to *Timing and Triggering* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Analog Trigger Types

You can configure the analog trigger circuitry to different triggering modes.

Level Triggering

You can configure the analog trigger circuitry to detect when the analog signal is below or above a level you specify.

In below-level analog triggering mode, the trigger is generated when the signal value is less than **Level**.

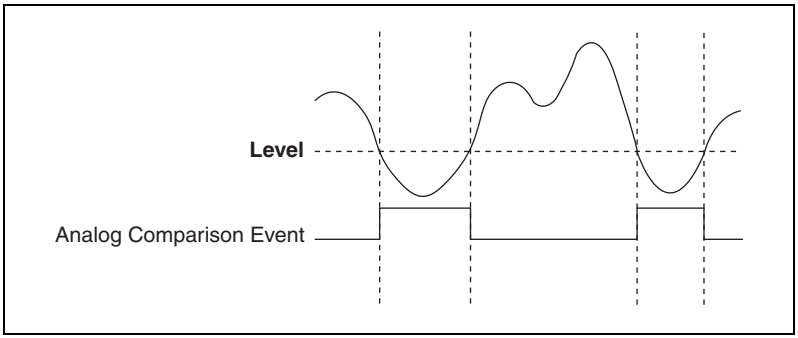


Figure 12-3. Below-Level Analog Triggering Mode

In above-level analog triggering mode, the trigger is generated when the signal value is greater than **Level**.

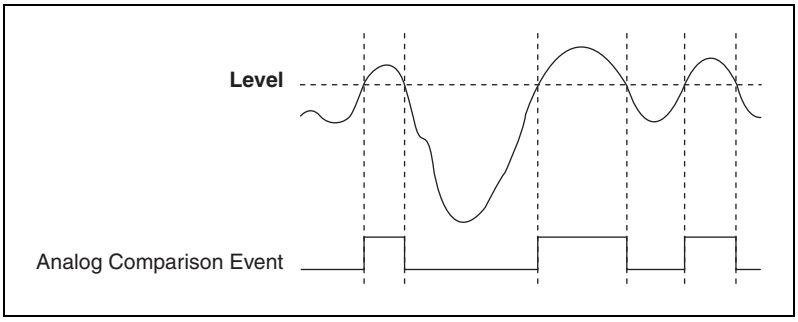


Figure 12-4. Above-Level Analog Triggering Mode

Level Triggering with Hysteresis

Hysteresis adds a programmable window above or below the trigger level that a valid trigger signal must pass through and is often used to reduce false triggering due to noise or jitter in the signal.

When using **Hysteresis** with a rising slope, the trigger asserts when the signal starts below **Level** and then crosses above **Level**. The trigger deasserts when the signal crosses below **Level** minus hysteresis.

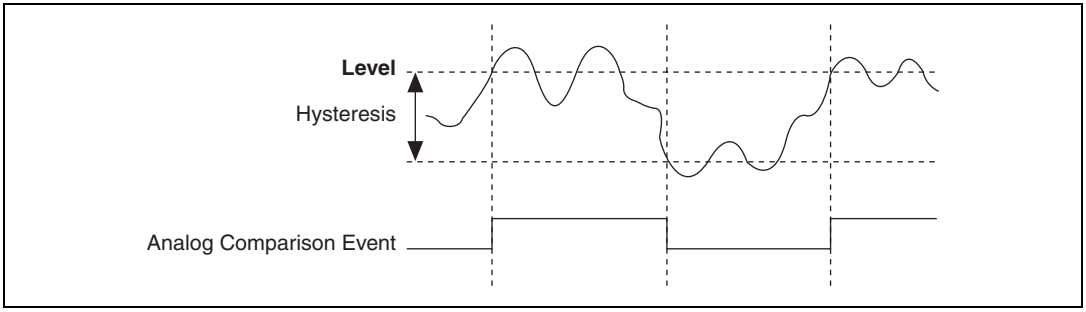


Figure 12-5. High Hysteresis

When using **Hysteresis** with a falling slope, the trigger asserts when the signal starts above **Level** and then crosses below **Level**. The trigger deasserts when the signal crosses above **Level** plus hysteresis.

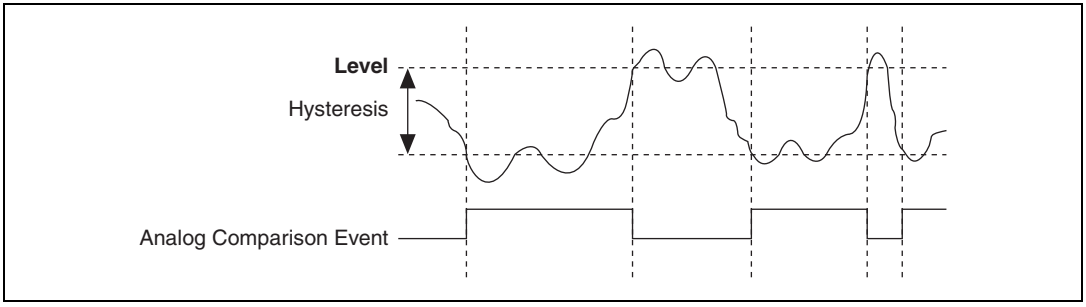


Figure 12-6. Low Hysteresis

Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two voltage levels. Specify the levels by setting the window **Top** value and the window **Bottom** value.

Figure 12-7 demonstrates a trigger that asserts when the signal enters the window.

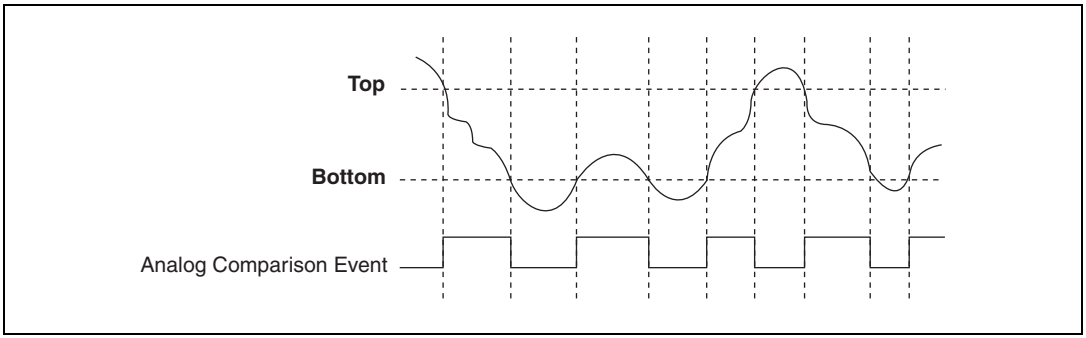


Figure 12-7. Window Trigger

Analog Trigger Accuracy

The analog trigger circuitry compares the voltage of the trigger source to the output of programmable trigger DACs. When you configure the level (or the high and low limits in window trigger mode), the device adjusts the output of the trigger DACs. Refer to the specifications document for your device to find the accuracy and resolution of the analog trigger DACs.

To improve accuracy you can perform the following:

- Use an AI channel (with a small input range) instead of PFI 0/AI START TRIG as your trigger source. The DAQ device does not amplify the PFI 0/AI START TRIG signal. When using an AI channel, the PGIA amplifies the AI channel signal before driving the analog trigger circuitry. If you configure the AI channel to have a small input range, you can trigger on very small voltage changes in the input signal.
- Software-calibrate the analog trigger circuitry. No hardware calibration is provided for the analog trigger circuitry. In addition, the propagation delay from when a valid trigger condition is met to when the analog trigger circuitry emits the Analog Comparison Event may have an impact on your measurements if the trigger signal has a high slew rate. If you find these conditions have a noticeable impact on your measurements, you can perform software calibration on the analog trigger circuitry by configuring your task as normal and applying a known signal for your analog trigger. Comparing the observed results against the expected results, you can calculate the necessary offsets to apply in software to fine-tune the desired triggering behavior.

A

Device-Specific Information

This appendix includes device-specific information about the following S Series devices:

- NI 6110/6111
- NI 6115/6120
- NI 6122/6123
- NI 6132/6133
- NI 6143

NI 6110/6111

The NI 6110/6111 is a Plug-and-Play, multifunction analog, digital, and timing I/O device for PCI bus computers.

The NI 6110 features the following:

- Four simultaneously sampling analog inputs with one 12-bit A/D converter (ADC) per channel
- Two 16-bit D/A converters (DACs) with voltage outputs
- Eight lines of TTL-compatible DIO
- Two general-purpose 24-bit counter/timers

The NI 6111 features the following:

- Two simultaneously sampling analog inputs with one 12-bit A/D converter (ADC) per channel
- Two 16-bit D/A converters (DACs) with voltage outputs
- Eight lines of TTL-compatible DIO
- Two general-purpose 24-bit counter/timers

Because the NI 6110/6111 has no DIP switches, jumpers, or potentiometers, it can be easily calibrated and configured in software.

NI 6110/6111 Analog Output

The NI PCI-6110/6111 supplies two channels of AO voltage at the I/O connector. The range is fixed at bipolar ±10 V.

NI 6110/6111 I/O Connector Pinouts

Figure A-1 shows the pin assignments for the 68-pin connector on the NI 6110.

Figure A-1. NI 6110 Pinout

Figure A-2 shows the pin assignments for the 68-pin connector on the NI 6111.

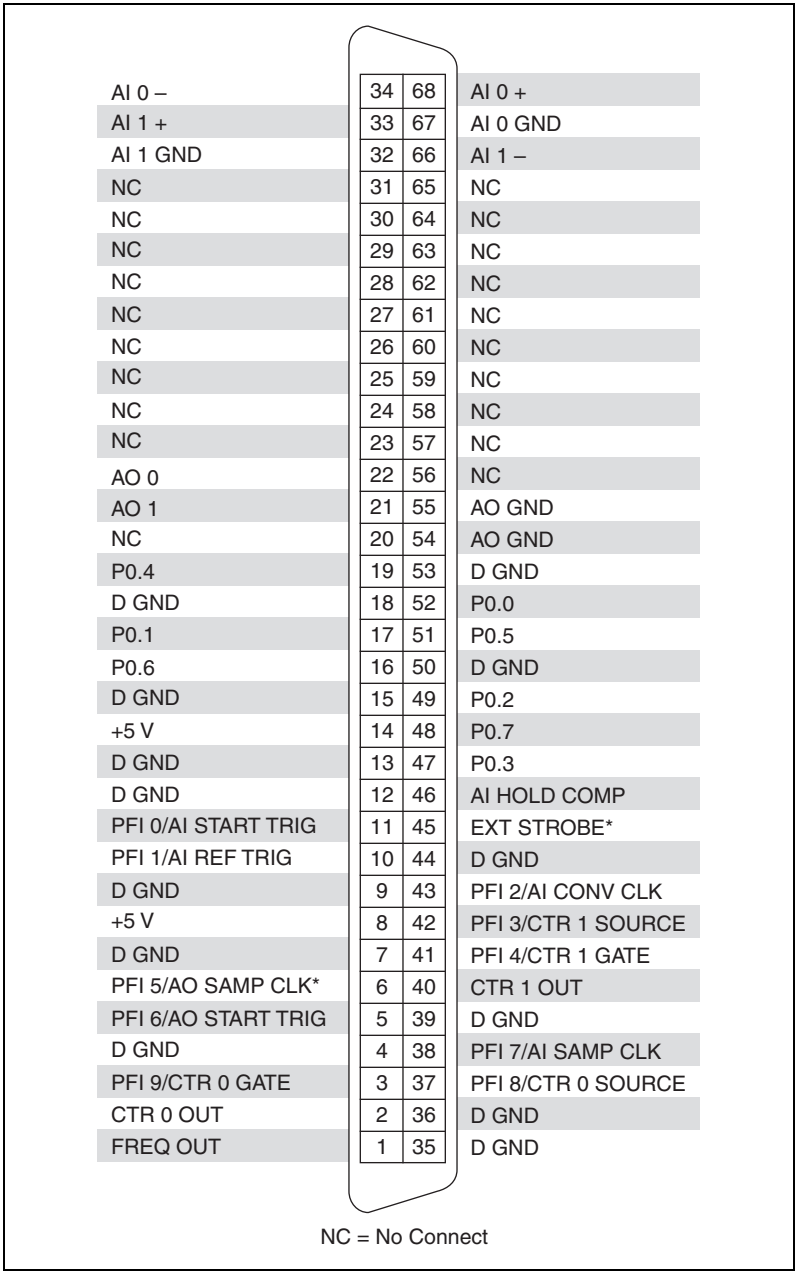


Figure A-2. NI 6111 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

50-Pin MIO I/O Connector Pinout

Figure A-3 shows the 50-pin I/O connector that is available when you use the SH6850 cable assembly with NI 6110/6111 devices.

AI <0..3> GND	1	2	AI <0..3> GND
AI 0 +	3	4	AI 0 –
AI 1 +	5	6	AI 1 –
AI 2 +[1]	7	8	AI 2 –[1]
AI 3 +[1]	9	10	AI 3 –[1]
PFI 0/AI START TRIG	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	AO 0
AO 1	21	22	NC
AO GND	23	24	D GND
P0.0	25	26	P0.1
P0.2	27	28	P0.3
P0.4	29	30	P0.5
P0.6	31	32	P0.7
D GND	33	34	+5 V
+5 V	35	36	AI HOLD COMP
EXT STROBE*	37	38	PFI 0/AI START TRIG
PFI 1/AI REF TRIG	39	40	PFI 2/AI CONV CLK
PFI 3/CTR 1 SOURCE	41	42	PFI 4/CTR 1 GATE
CTR 1 OUT	43	44	PFI 5/AO SAMP CLK
PFI 6/AO START TRIG	45	46	PFI 7/AI SAMP CLK
PFI 8/CTR 0 SOURCE	47	48	PFI 9/CTR 0 GATE
CTR 0 OUT	49	50	FREQ OUT

[1] NC on NI 6111

Figure A-3. 50-Pin I/O Connector

Note Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an S Series device in Traditional NI-DAQ (Legacy), refer to Table 3-2, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

NI 6110/6111 Block Diagrams

Figure A-4 shows the NI 6110 block diagram.

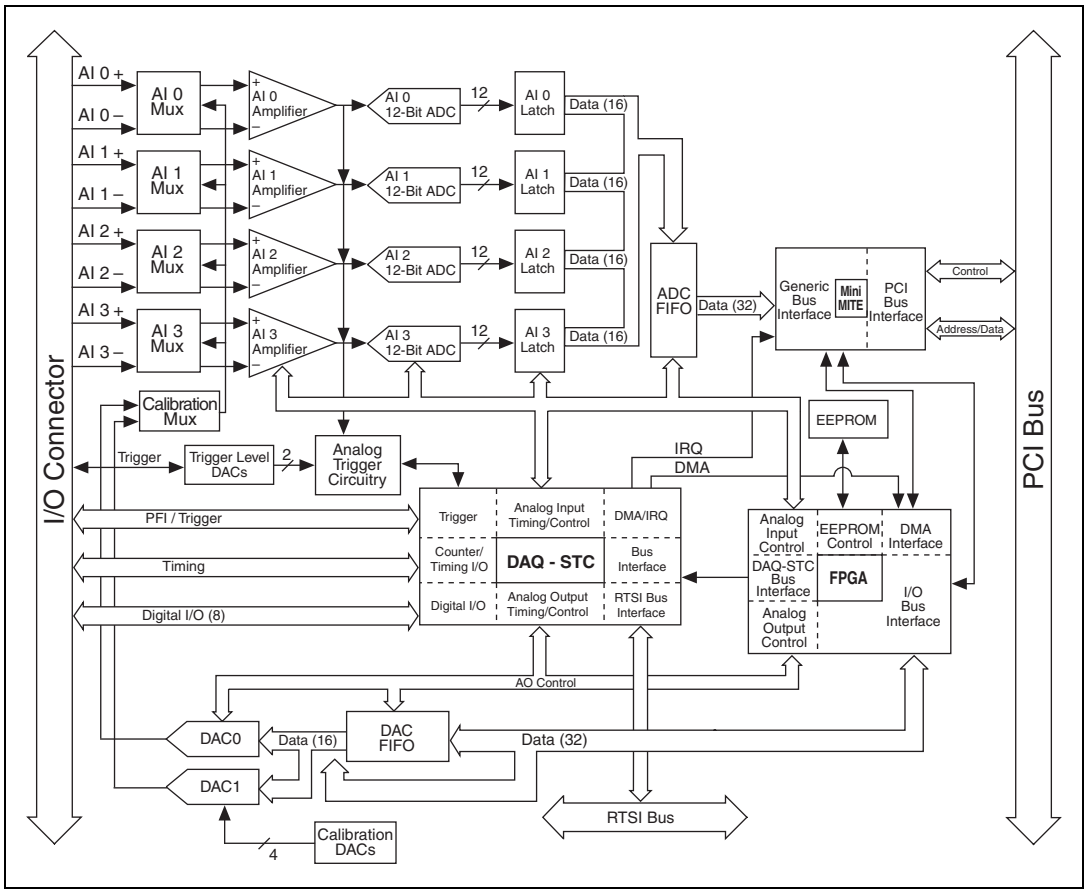


Figure A-4. NI 6110 Block Diagram

Figure A-5 shows the NI 6111 block diagram.

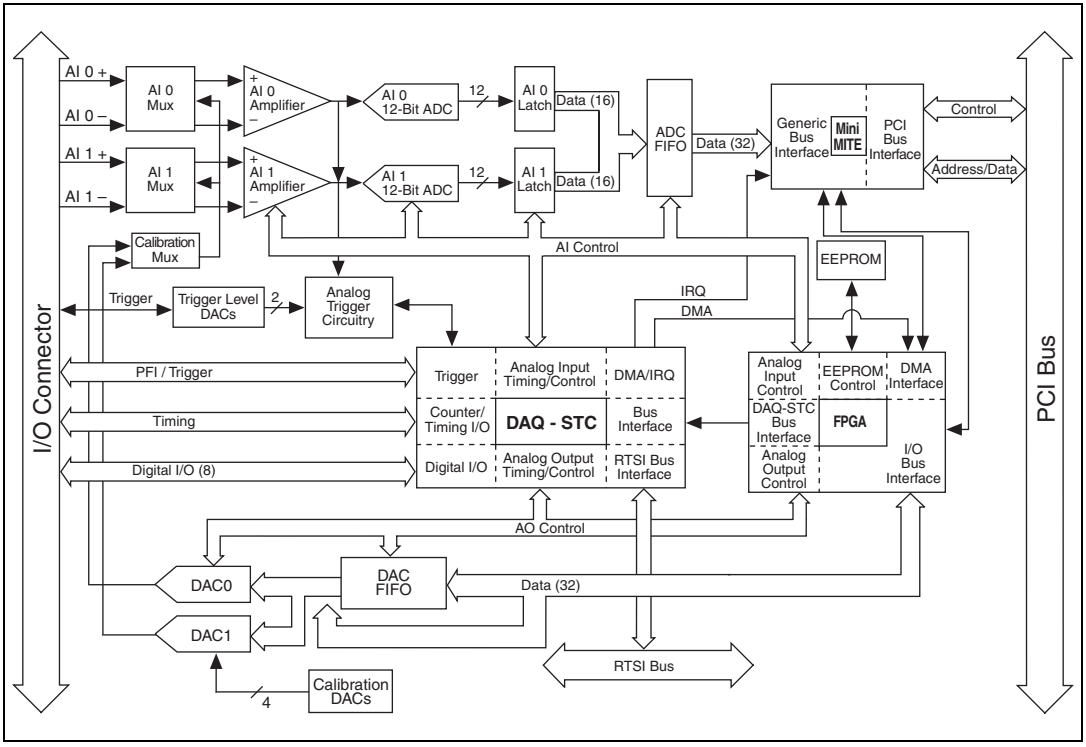


Figure A-5. NI 6111 Block Diagram

NI 6110/6111 Cables and Accessories

This section describes some of the cable and accessory options for the NI 6110/6111. For more specific information about these products, refer to `ni.com`.

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

Using BNCs

You can connect BNC cables to your DAQ device using BNC accessories such as the BNC-2110, BNC-2120, and BNC-2090A.

Using Screw Terminals

You can connect signals to your DAQ device using a screw terminal accessory such as the following:

- **CB-68LP**, **CB-68LPR**—Low-cost screw terminal block
- **SCB-68**—Shielded screw terminal block with breadboard areas
- **TBX-68**—DIN rail mountable screw terminal block
- **TB-2705**—PXI screw terminal block with metal housing

Cabling

To connect your DAQ device to the accessories listed in this section, use one of the following cables:

- **SH68-68-EPM**—Shielded cable
- **SH68-68R1-EP**—Shielded cable with one right angle connector
- **R6868**—Unshielded cable

Using RTSI

Use RTSI bus cables to connect the timing and synchronization signals on your DAQ device to other Measurement, Vision, Motion, and CAN devices for PCI.

Custom Cabling/Connectors Options

The CA-1000 is a versatile connector/enclosure system. It allows the user to define I/O connectors on a per-channel basis. Internally, the system allows for flexible custom wiring configuration.

If you want to develop your own cable, follow these guidelines for best results:

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

NI recommends that you use one of the following connectors with the I/O connector on your device:

- Honda 68-position, solder cup, female connector
- Honda backshell
- AMP VHDCI connector

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

NI 6110/6111 Specifications

Refer to the *NI 6110/6111 Specifications* for more detailed information about the devices.

NI 6115/6120

The NI 6115/6120 is a Plug-and-Play, multifunction analog, digital, and timing I/O device for PCI and PXI bus computers.

The NI 6115 features the following:

- Four simultaneously sampling analog inputs with one 12-bit A/D converter (ADC) per channel
- Two 12-bit D/A converters (DACs) with voltage outputs
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers
- Increased common-mode noise rejection through pseudodifferential signal connection

The NI 6120 features the following:

- Four simultaneously sampling analog inputs with one 16-bit A/D converter (ADC) per channel
- Two 16-bit D/A converters (DACs) with voltage outputs
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers
- Increased common-mode noise rejection through pseudodifferential signal connection

Because the NI 6115/6120 has no DIP switches, jumpers, or potentiometers, it can be easily calibrated and configured in software.

NI 6115/6120 Analog Output

The NI 6115/6120 supplies two channels of AO voltage at the I/O connector. The range is fixed at bipolar ±10 V.

The AO channels on the NI 6115 contain 12-bit DACs that are capable of 4 MS/s for one channel or 2.5 MS/s for each of two channels. The NI 6120 DACs are 16-bit, and they have the same AO capabilities as the NI 6115. Refer to the *NI 6115/6120 Specifications* for more detailed information about the AO capabilities of the NI 6115/6120.

Note The AO channels do not have analog or digital filtering hardware and do produce images in the frequency domain related to the update rate.

The NI 6115/6120 includes high-density memory modules allowing for long waveform generations.

NI 6115/6120 I/O Connector Pinout

Figure A-6 shows the pin assignments for the 68-pin connector on the NI 6115/6120.

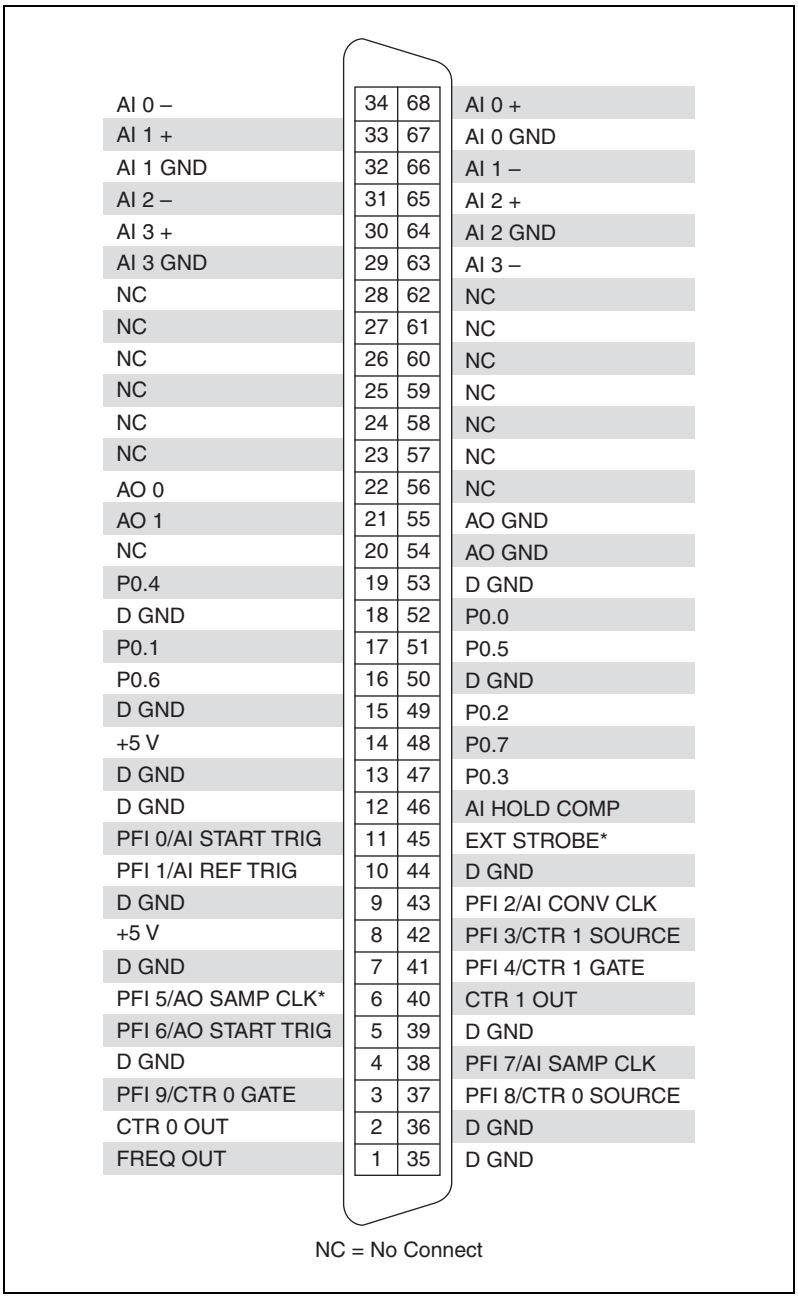


Figure A-6. NI 6115/6120 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

NI 6115/6120 Block Diagrams

Figure A-7 shows the NI 6115 block diagram.

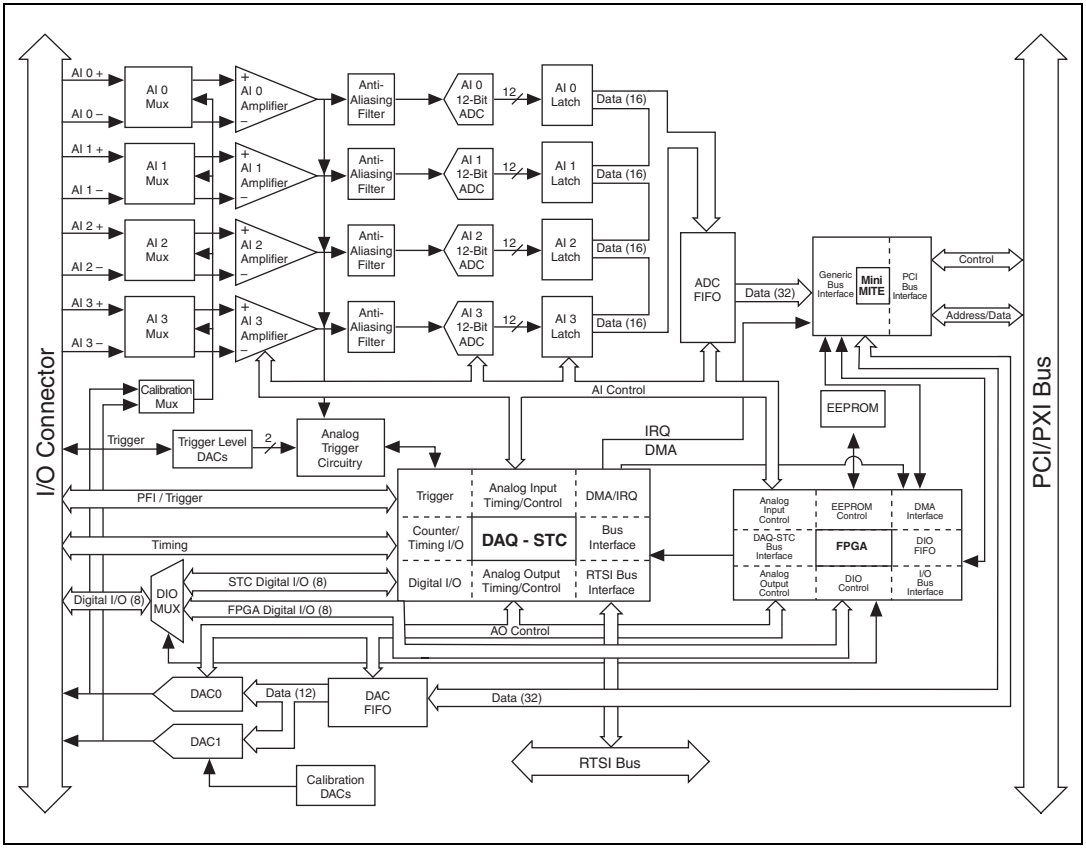


Figure A-7. NI 6115 Block Diagram

Figure A-8 shows the NI 6120 block diagram.

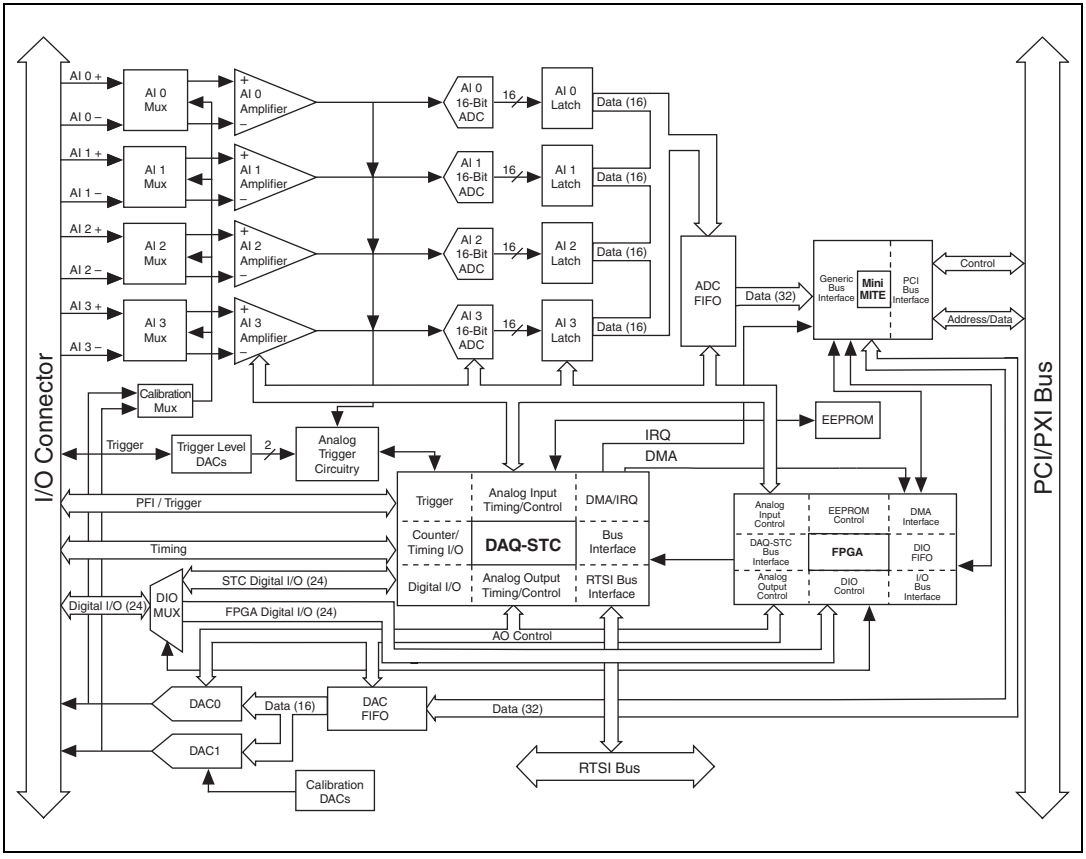


Figure A-8. NI 6120 Block Diagram

NI 6115/6120 Cables and Accessories

This section describes some of the cable and accessory options for the NI 6115/6120. For more specific information about these products, refer to `ni.com`.

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

Using BNCs

You can connect BNC cables to your DAQ device using BNC accessories such as the BNC-2110, BNC-2120, and BNC-2090A.

Using Screw Terminals

You can connect signals to your DAQ device using a screw terminal accessory such as the following:

- **CB-68LP**, **CB-68LPR**—Low-cost screw terminal block
- **SCB-68**—Shielded screw terminal block with breadboard areas
- **TBX-68**—DIN rail mountable screw terminal block
- **TB-2705**—PXI screw terminal block with metal housing

Using SMBs

You can connect SMB cables to your PXI DAQ device using the TB-2708.

Cabling

To connect your DAQ device to the accessories listed in this section, use one of the following cables:

- **SH68-68-EPM**—Shielded cable
- **SH68-68R1-EP**—Shielded cable with one right angle connector
- **R6868**—Unshielded cable

Using RTSI

Use RTSI bus cables to connect the timing and synchronization signals on your DAQ device to other Measurement, Vision, Motion, and CAN devices for PCI.

Custom Cabling/Connectors Options

The CA-1000 is a versatile connector/enclosure system. It allows the user to define I/O connectors on a per-channel basis. Internally, the system allows for flexible custom wiring configuration.

If you want to develop your own cable, follow these guidelines for best results:

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

NI recommends that you use one of the following connectors with the I/O connector on your device:

- Honda 68-position, solder cup, female connector
- Honda backshell
- AMP VHDCI connector

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

NI 6115/6120 Specifications

Refer to the *NI 6115/6120 Specifications* for more detailed information about the devices.

NI 6122/6123

The NI 6122/6123 is a Plug-and-Play multifunction analog, digital, and timing I/O device for PCI and PXI bus computers.

The NI 6122 features the following:

- Four simultaneously sampling analog inputs with one 16-bit A/D converter (ADC) per channel
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers

The NI 6123 features the following:

- Eight simultaneously sampling analog inputs with one 16-bit A/D converter (ADC) per channel
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers

Because the NI 6122/6123 devices have no DIP switches, jumpers, or potentiometers, they can be easily calibrated and configured in software.

NI 6122/6123 I/O Connector Pinouts

Figure A-9 shows the pin assignments for the 68-pin I/O connector on the NI 6122.

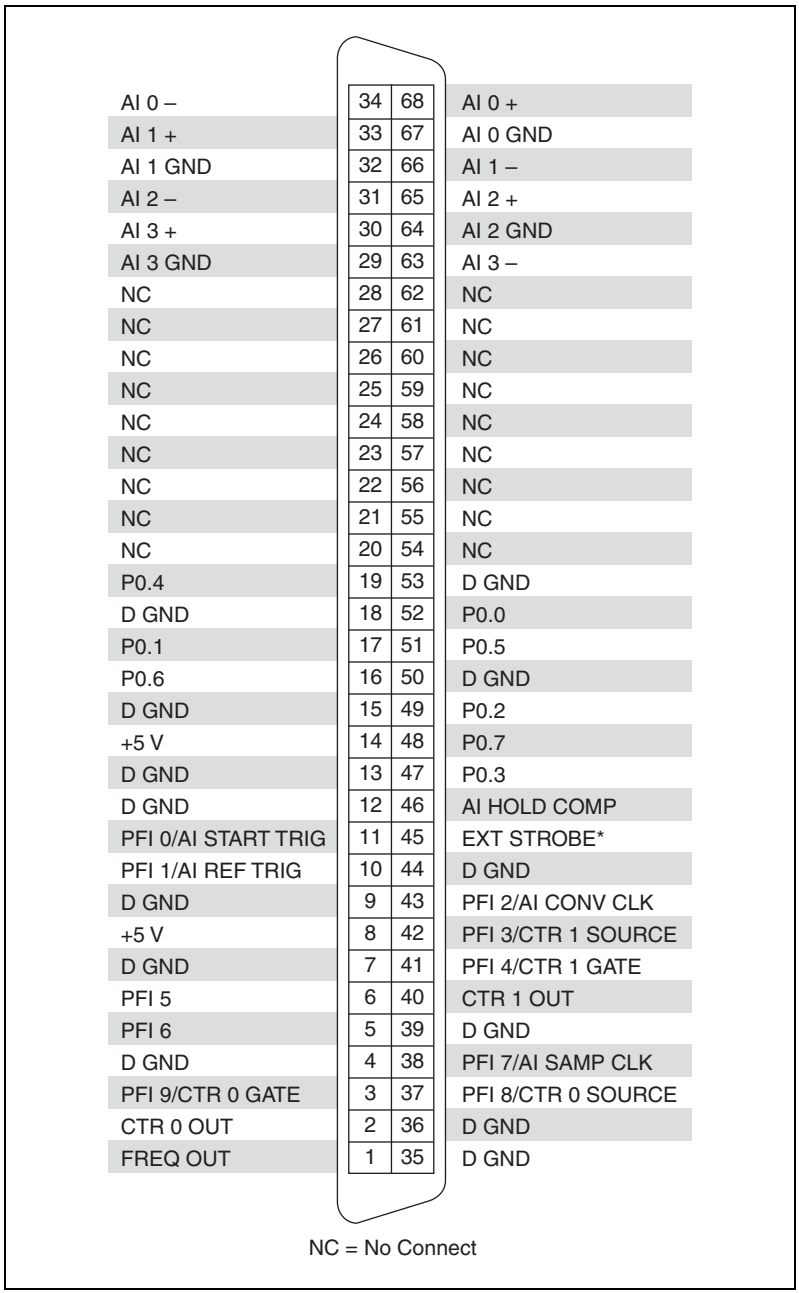


Figure A-9. NI 6122 Pinout

Figure A-10 shows the pin assignments for the 68-pin I/O connector on the NI 6123.

Figure A-10. NI 6123 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

50-Pin MIO I/O Connector Pinout

Figure A-11 shows the 50-pin I/O connector that is available when you use the SH6850 cable assembly with NI 6122/6123 devices.

AI <0..3> GND	1	2	AI <0..3> GND
AI 0 +	3	4	AI 0 –
AI 1 +	5	6	AI 1 –
AI 2 +	7	8	AI 2 –
AI 3 +	9	10	AI 3 –
PFI 0/AI START TRIG	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	AO 0
AO 1	21	22	NC
AO GND	23	24	D GND
P0.0	25	26	P0.1
P0.2	27	28	P0.3
P0.4	29	30	P0.5
P0.6	31	32	P0.7
D GND	33	34	+5 V
+5 V	35	36	AI HOLD COMP
EXT STROBE*	37	38	PFI 0/AI START TRIG
PFI 1/AI REF TRIG	39	40	PFI 2/AI CONV CLK
PFI 3/CTR 1 SOURCE	41	42	PFI 4/CTR 1 GATE
CTR 1 OUT	43	44	PFI 5/AO SAMP CLK
PFI 6/AO START TRIG	45	46	PFI 7/AI SAMP CLK
PFI 8/CTR 0 SOURCE	47	48	PFI 9/CTR 0 GATE
CTR 0 OUT	49	50	FREQ OUT

Figure A-11. 50-Pin I/O Connector

Note Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an S Series device in Traditional NI-DAQ (Legacy), refer to Table 3-2, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

NI 6122/6123 Block Diagram

Figure A-12 shows the NI 6122/6123 block diagram.

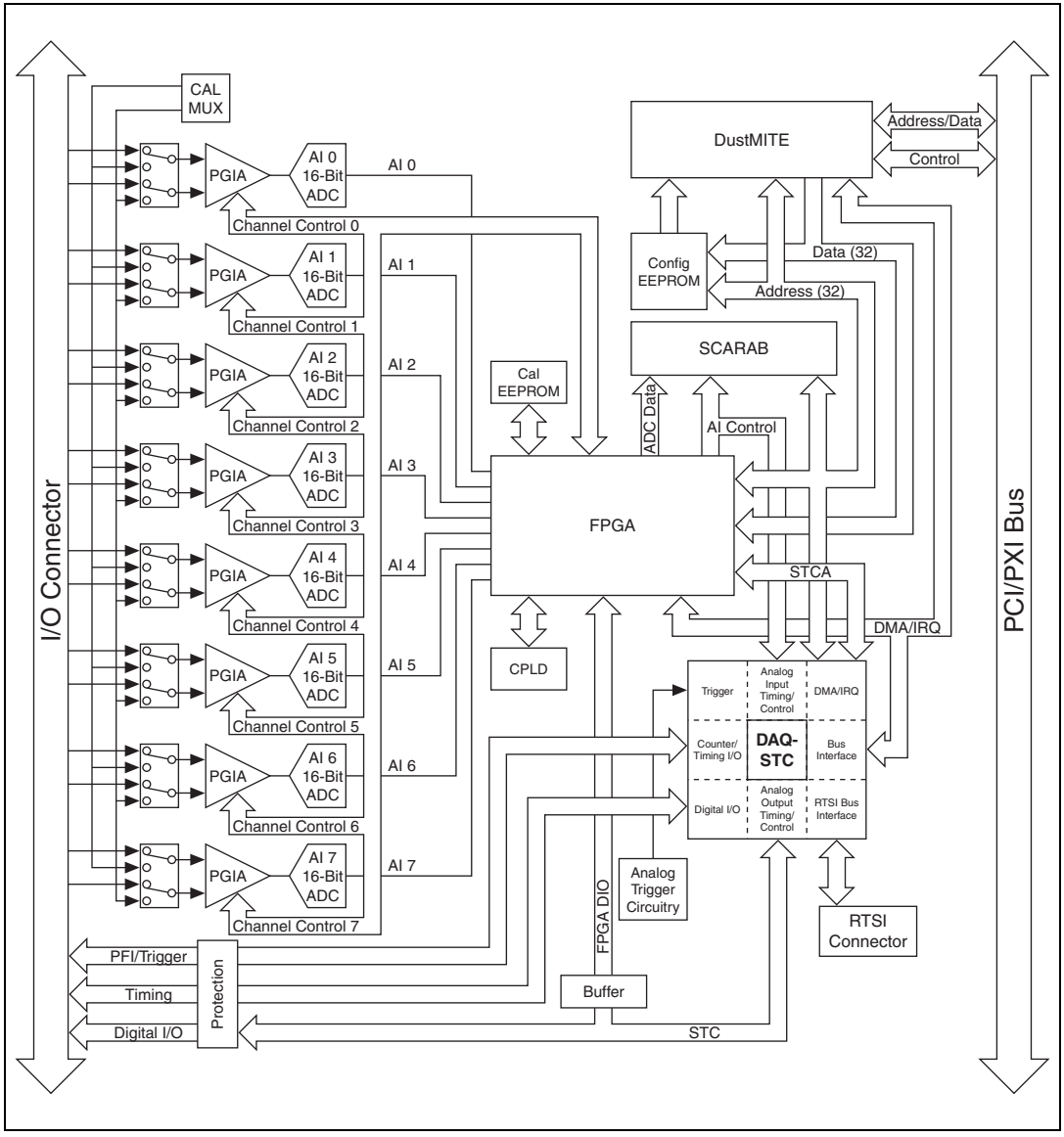


Figure A-12. NI 6122/6123 Block Diagram

Note AI <4..7> appear only on the NI 6123.

NI 6122/6123 Cables and Accessories

This section describes some of the cable and accessory options for the NI 6122/6123. For more specific information about these products, refer to `ni.com`.

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

Using BNCs

You can connect BNC cables to your DAQ device using BNC accessories such as the BNC-2110, BNC-2120, and BNC-2090A.

Using Screw Terminals

You can connect signals to your DAQ device using a screw terminal accessory such as the following:

- **CB-68LP**, **CB-68LPR**—Low-cost screw terminal block
- **SCB-68**—Shielded screw terminal block with breadboard areas
- **TBX-68**—DIN rail mountable screw terminal block
- **TB-2705**—PXI screw terminal block with metal housing

Using SMBs

You can connect SMB cables to your PXI DAQ device using the TB-2709.

Cabling

To connect your DAQ device to the accessories listed in this section, use one of the following cables:

- **SH68-68-EPM**—Shielded 68-conductor cable
- **SH68-68R1-EP**—Shielded right-angle 68-conductor cable
- **SH6868**—Shielded 68-conductor cable
- **R6868**—68-conductor ribbon cable

Using RTSI

Use RTSI bus cables to connect the timing and synchronization signals on your DAQ device to other Measurement, Vision, Motion, and CAN devices for PCI.

Custom Cabling/Connectors Options

The CA-1000 is a versatile connector/enclosure system. It allows the user to define I/O connectors on a per-channel basis. Internally, the system allows for flexible custom wiring configuration.

If you want to develop your own cable, follow these guidelines for best results:

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

NI recommends that you use one of the following connectors with the I/O connector on your device:

- Honda 68-position, solder cup, female connector
- Honda backshell
- AMP VHDCI connector

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

NI 6122/6123 Specifications

Refer to the *NI 6122/6123 Specifications* for more detailed information about the devices.

NI 6132/6133

The NI 6132/6133 is a Plug-and-Play multifunction analog, digital, and timing I/O device for PCI and PXI bus computers.

The NI 6132 features the following:

- Four simultaneously sampling analog inputs with one 14-bit A/D converter (ADC) per channel
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers

The NI 6133 features the following:

- Eight simultaneously sampling analog inputs with one 14-bit A/D converter (ADC) per channel
- Eight lines of TTL-compatible correlated DIO
- Two general-purpose 24-bit counter/timers

Because the NI 6132/6133 devices have no DIP switches, jumpers, or potentiometers, they can be easily calibrated and configured in software.

NI 6132/6133 I/O Connector Pinouts

Figure A-13 shows the pin assignments for the 68-pin I/O connector on the NI 6132.

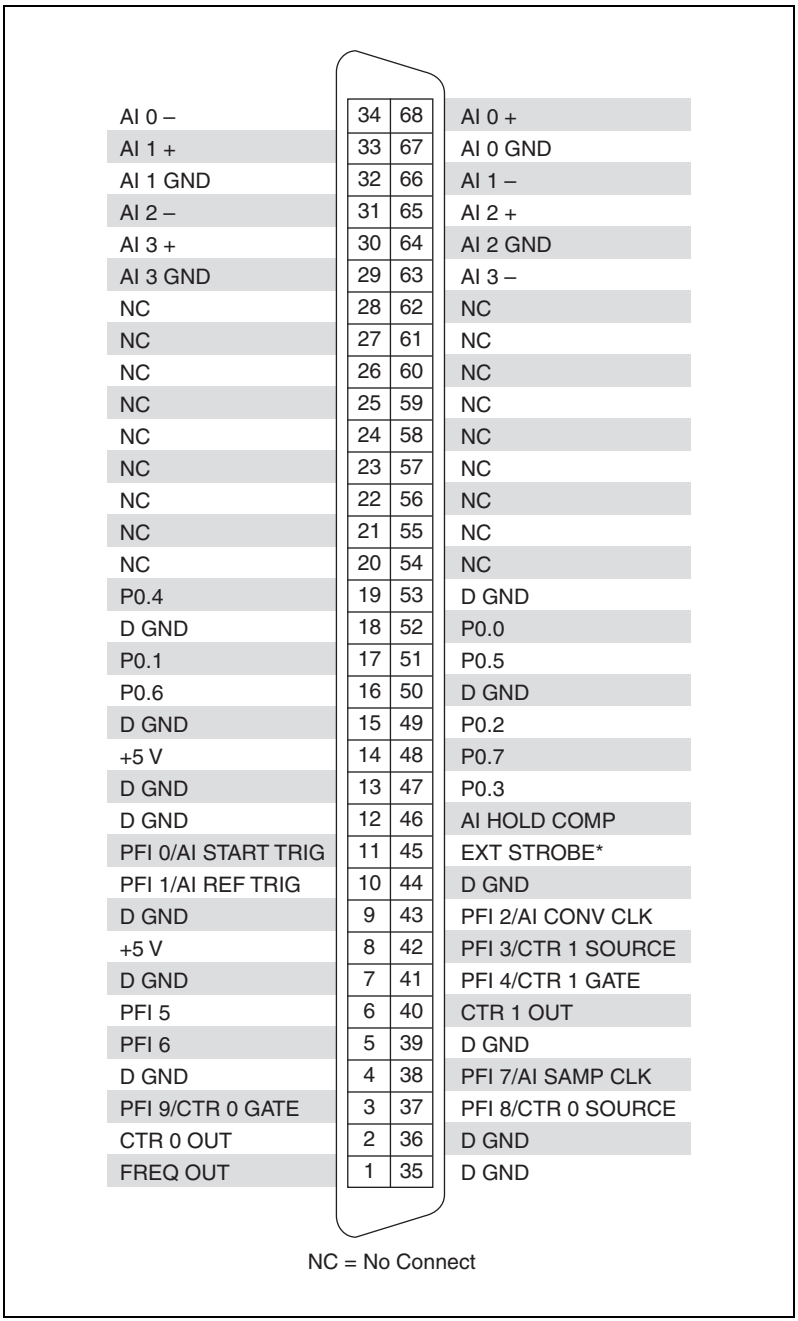


Figure A-13. NI 6132 Pinout

Figure A-11 shows the pin assignments for the 68-pin I/O connector on the NI 6133.

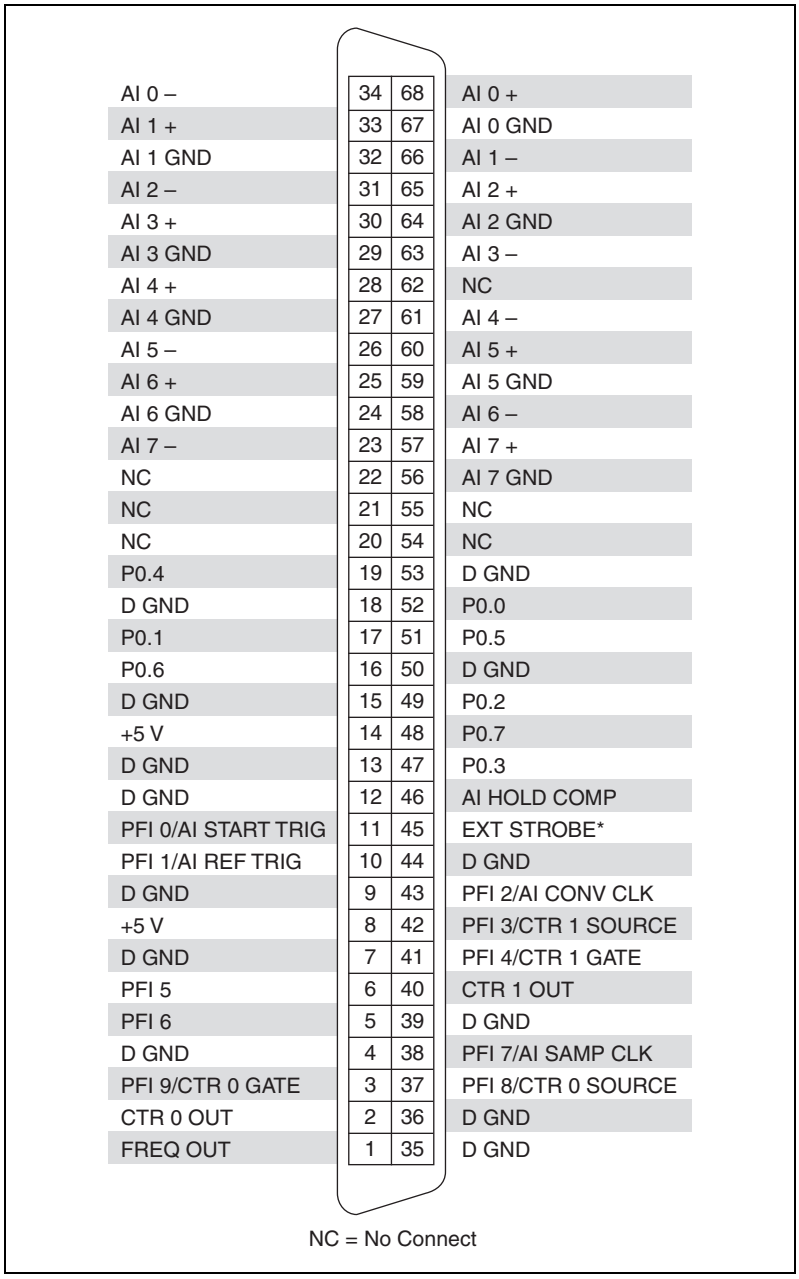


Figure A-14. NI 6133 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

50-Pin MIO I/O Connector Pinout

Figure A-15 shows the 50-pin I/O connector that is available when you use the SH6850 cable assembly with NI 6132/6133 devices.

AI <0..3> GND	1	2	AI <0..3> GND
AI 0 +	3	4	AI 0 –
AI 1 +	5	6	AI 1 –
AI 2 +	7	8	AI 2 –
AI 3 +	9	10	AI 3 –
PFI 0/AI START TRIG	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	AO 0
AO 1	21	22	NC
AO GND	23	24	D GND
P0.0	25	26	P0.1
P0.2	27	28	P0.3
P0.4	29	30	P0.5
P0.6	31	32	P0.7
D GND	33	34	+5 V
+5 V	35	36	AI HOLD COMP
EXT STROBE*	37	38	PFI 0/AI START TRIG
PFI 1/AI REF TRIG	39	40	PFI 2/AI CONV CLK
PFI 3/CTR 1 SOURCE	41	42	PFI 4/CTR 1 GATE
CTR 1 OUT	43	44	PFI 5/AO SAMP CLK
PFI 6/AO START TRIG	45	46	PFI 7/AI SAMP CLK
PFI 8/CTR 0 SOURCE	47	48	PFI 9/CTR 0 GATE
CTR 0 OUT	49	50	FREQ OUT

Figure A-15. 50-Pin I/O Connector

Note Some hardware accessories may not yet reflect the NI-DAQmx terminal names. If you are using an S Series device in Traditional NI-DAQ (Legacy), refer to Table 3-2, *Terminal Name Equivalents*, for the Traditional NI-DAQ (Legacy) signal names.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

NI 6132/6133 Block Diagram

Figure A-16 shows the NI 6132/6133 block diagram.

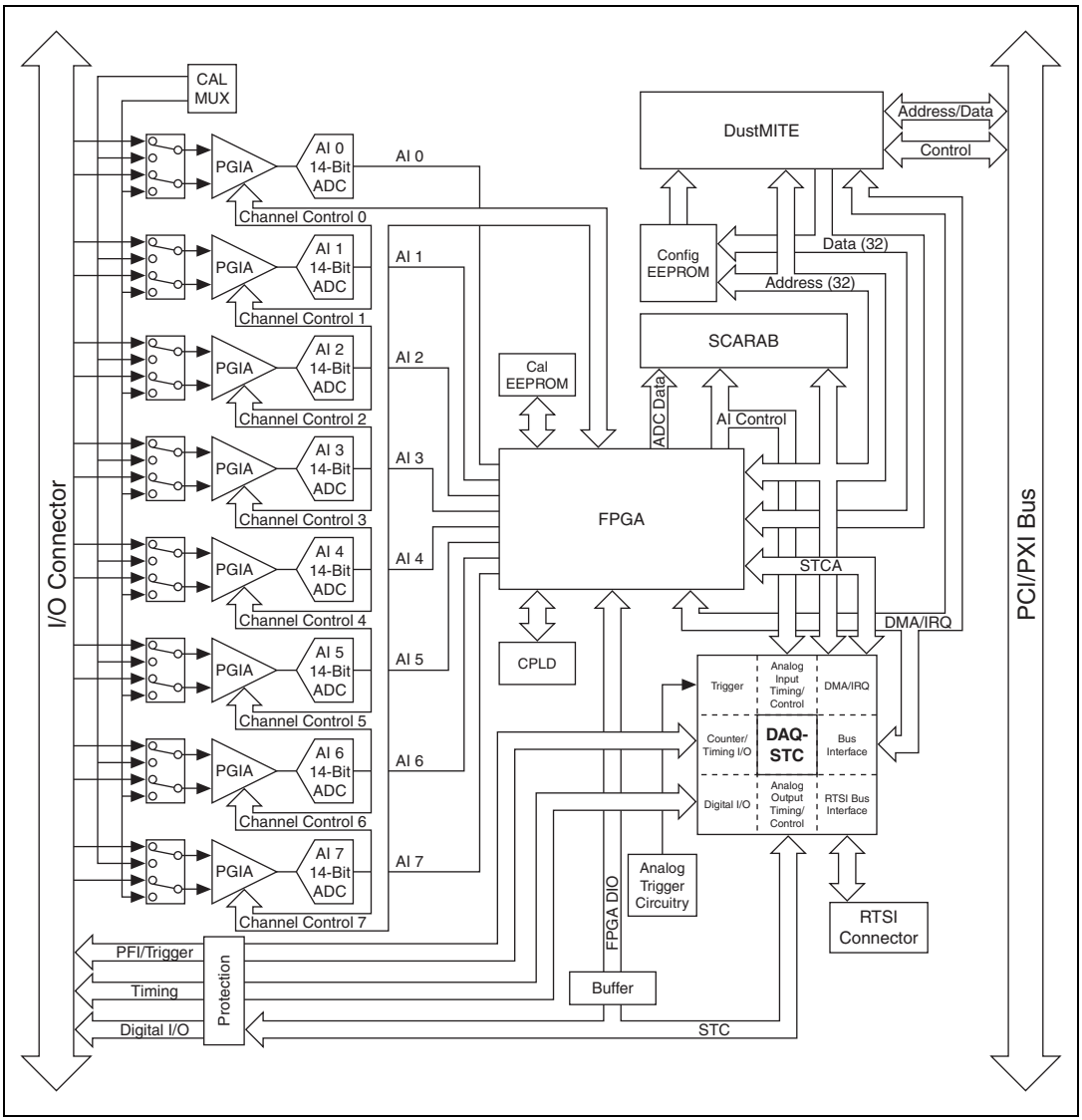


Figure A-16. NI 6132/6133 Block Diagram

Note AI <4..7> appear only on the NI 6133.

NI 6132/6133 Cables and Accessories

This section describes some of the cable and accessory options for the NI 6132/6133. For more specific information about these products, refer to `ni.com`.

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

Using BNCs

You can connect BNC cables to your DAQ device using BNC accessories such as the BNC-2110, BNC-2120, and BNC-2090A.

Using Screw Terminals

You can connect signals to your DAQ device using a screw terminal accessory such as the following:

- **CB-68LP**, **CB-68LPR**—Low-cost screw terminal block
- **SCB-68**—Shielded screw terminal block with breadboard areas
- **TBX-68**—DIN rail mountable screw terminal block
- **TB-2705**—PXI screw terminal block with metal housing

Using SMBs

You can connect SMB cables to your PXI DAQ device using the TB-2709.

Cabling

To connect your DAQ device to the accessories listed in this section, use one of the following cables:

- **SH68-68-EPM**—Shielded 68-conductor cable
- **SH68-68R1-EP**—Shielded right-angle 68-conductor cable
- **SH6868**—Shielded 68-conductor cable
- **R6868**—68-conductor ribbon cable

Using RTSI

Use RTSI bus cables to connect the timing and synchronization signals on your DAQ device to other Measurement, Vision, Motion, and CAN devices for PCI.

Custom Cabling/Connectors Options

The CA-1000 is a versatile connector/enclosure system. It allows the user to define I/O connectors on a per-channel basis. Internally, the system allows for flexible custom wiring configuration.

If you want to develop your own cable, follow these guidelines for best results:

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

NI recommends that you use one of the following connectors with the I/O connector on your device:

- Honda 68-position, solder cup, female connector
- Honda backshell
- AMP VHDCI connector

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

NI 6132/6133 Specifications

Refer to the *NI 6132/6133 Specifications* for more detailed information about the devices.

NI 6143

The NI 6143 is a Plug-and-Play multifunction analog, digital, and timing I/O device for PCI and PXI bus computers.

The NI 6143 features the following:

- Eight simultaneously sampling analog inputs with one 16-bit A/D converter (ADC) per channel
- Eight lines of TTL-compatible DIO
- Two general-purpose 24-bit counter/timers

Because the NI 6143 has no DIP switches, jumpers, or potentiometers, it can be easily calibrated and configured in software.

NI 6143 I/O Connector Pinout

Figure A-17 shows the pin assignments for the 68-pin I/O connector on the NI 6143.

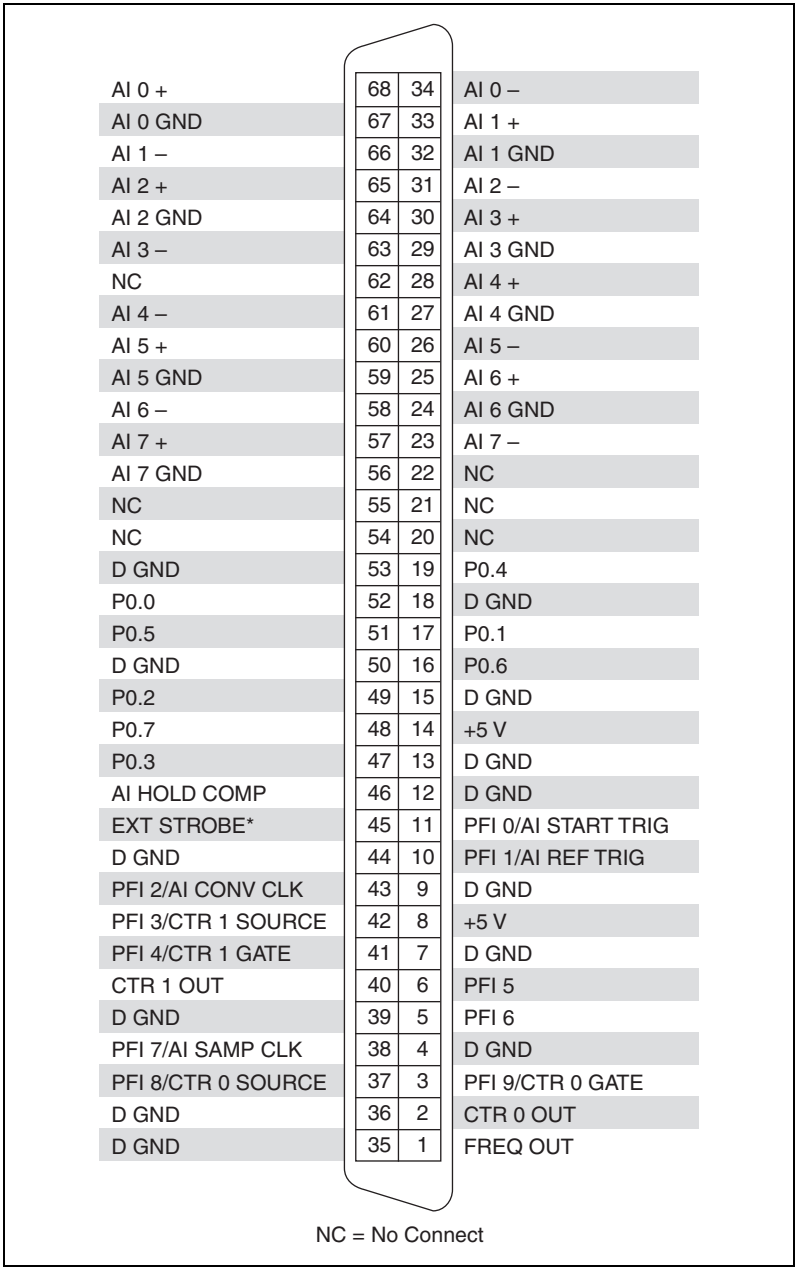


Figure A-17. NI 6143 Pinout

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *I/O Connector*.

NI 6143 Block Diagram

Figure A-18 shows the NI 6143 block diagram.

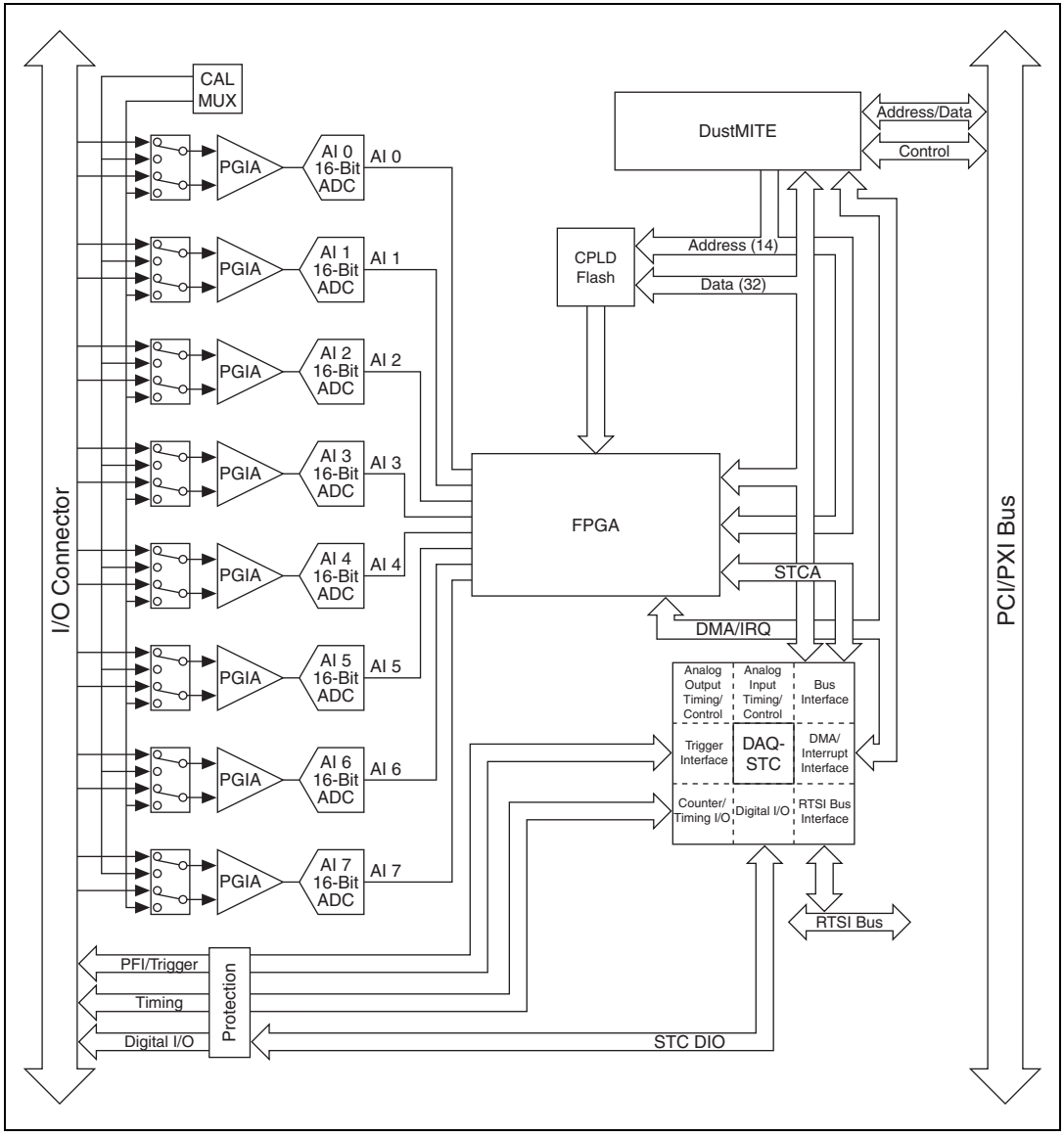


Figure A-18. NI 6143 Block Diagram

NI 6143 Cables and Accessories

This section describes some of the cable and accessory options for the NI 6143. For more specific information about these products, refer to `ni.com`.

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

Using BNCs

You can connect BNC cables to your DAQ device using BNC accessories such as the BNC-2110, BNC-2120, and BNC-2090A.

Using Screw Terminals

You can connect signals to your DAQ device using a screw terminal accessory such as the following:

- **CB-68LP**, **CB-68LPR**—Low-cost screw terminal block
- **SCB-68**—Shielded screw terminal block with breadboard areas
- **TBX-68**—DIN rail mountable screw terminal block
- **TB-2706**—PXI screw terminal block with metal housing

Cabling

To connect your DAQ device to the accessories listed in this section, use one of the following cables:

- **SHC68-68-EPM**—Individually shielded, twisted-pair VHDCI to SCSI-II cable
- **SHC68-68-EP**—Shielded VHDCI to SCSI-II cable

Using RTSI

Use RTSI bus cables to connect the timing and synchronization signals on your DAQ device to other Measurement, Vision, Motion, and CAN devices for PCI.

Custom Cabling/Connectors Options

The CA-1000 is a versatile connector/enclosure system. It allows the user to define I/O connectors on a per-channel basis. Internally, the system allows for flexible custom wiring configuration.

If you want to develop your own cable, follow these guidelines for best results:

- Use shielded twisted-pair wires for each differential AI pair. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

NI recommends that you use one of the following connectors with the I/O connector on your device:

- Honda 68-position, solder cup, female connector
- Honda backshell
- AMP VHDCI connector

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

NI 6143 Specifications

Refer to the *NI 6143 Specifications* for more detailed information about the device.

B

Technical Support and Professional Services

Visit the following sections of the award-winning National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support as well as exclusive access to on demand training modules via the Services Resource Center. NI offers complementary membership for a full year after purchase, after which you may renew to continue your benefits.

    For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.
- **Training and Certification**—Visit ni.com/training for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

°	Degree.
>	Greater than.
<	Less than.
–	Negative of, or minus.
Ω	Ohms.
/	Per.
%	Percent.
±	Plus or minus.
+	Positive of, or plus.

A

A	Amperes—The unit of electric current.
A/D	Analog-to-digital.
AC	Alternating current.

ADC	Analog-to-digital converter—An electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
ADE	Application Development Environment—A software environment incorporating the development, debug, and analysis tools for software development. LabVIEW, Measurement Studio, and Visual Studio are examples.
AI	1. Analog input. 2. Analog input channel signal.
aliasing	The consequence of sampling that causes signals with frequencies higher than half the sampling frequency to appear as lower frequency components in a frequency spectrum.
AO	Analog output.
ASIC	Application-Specific Integrated Circuit—A proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).
building ground	*See* earth ground.

C

C	Celsius
CalDAC	Calibration DAC.

channel	1. Physical—A terminal or pin at which you can measure or generate an analog or digital signal. A single physical channel can include more than one terminal, as in the case of a differential analog input channel or a digital port of eight lines. The name used for a counter physical channel is an exception because that physical channel name is not the name of the terminal where the counter measures or generates the digital signal. 2. Virtual—A collection of property settings that can include a name, a physical channel, input terminal connections, the type of measurement or generation, and scaling information. You can define NI-DAQmx virtual channels outside a task (global) or inside a task (local). Configuring virtual channels is optional in Traditional NI-DAQ (Legacy) and earlier versions, but is integral to every measurement you take in NI-DAQmx. In Traditional NI-DAQ (Legacy), you configure virtual channels in MAX. In NI-DAQmx, you can configure virtual channels either in MAX or in a program, and you can configure channels as part of a task or separately.
chassis ground	Any connection back to the protective conductor earth ground. *See also* earth ground.
cm	Centimeter.
CMOS	Complementary metal-oxide semiconductor.
CMRR	Common-mode rejection ratio—A measure of the capability of an instrument to reject a signal that is common to both input leads.
CompactPCI	A Eurocard configuration of the PCI bus for industrial applications.
correlated DIO	A feature that allows you to clock digital I/O on the same clock as analog I/O.
counter/timer	A circuit that counts external pulses or clock pulses (timing).
coupling	The manner in which a signal is connected from one circuit to another. When applied to instrument products or DAQ cards, it refers to the input signal coupling technique.

D

DAC	Digital-to-analog converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.

DAQ device	A device that acquires or generates data and can contain multiple channels and conversion devices. DAQ devices include plug-in devices, PCMCIA cards, and DAQPad devices, which connect to a computer USB port. SCXI modules are considered DAQ devices.
DAQ-STC	Data acquisition system timing controller—An application-specific integrated circuit (ASIC) for the system timing requirements of a general A/D and D/A system.
data acquisition (DAQ)	1. Acquiring and measuring analog or digital electrical signals from sensors, transducers, and test probes or fixtures. 2. Generating analog or digital electrical signals.
dB	Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2 for signals in volts.
dBc	Decibel carrier—Level difference referenced to a carrier level, c.
DC	Direct current—Although the term speaks of current, many different types of DC measurements are made, including DC Voltage, DC current, and DC power.
device	1. An instrument or controller you can access as a single entity that controls or monitors real-world I/O points. A device often is connected to a host computer through some type of communication network. 2. *See* DAQ device and measurement device.
D GND	Digital ground signal.
DI	Digital input.
differential mode	DIFF. An analog input mode consisting of two terminals, both of which are isolated from computer ground, whose difference is measured.
DIO	Digital input/output.
DIP	Dual inline package.
DMA	Direct memory access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.

DNL	Differential nonlinearity—A measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB.
DO	Digital output.
driver	Software unique to the device or type of device, and includes the set of commands the device accepts.

E

earth ground	A direct electrical connection to the earth which provides a reference voltage level (called zero potential or ground potential) against which all other voltages in a system are established and measured. Also referred to as building ground.
EEPROM	Electrically erasable programmable read–only memory–ROM that can be erased with an electrical signal and reprogrammed.
ESD	Electrostatic Discharge—A high-voltage, low-current discharge of static electricity that can damage sensitive electronic components. Electrostatic discharge voltage can easily range from 1,000 to 10,000 V.

F

F	Farad—A measurement unit of capacitance.
FIFO	First-in-first-out memory buffer—A data buffering technique that functions like a shift register where the oldest values (first in) come out first. Many DAQ products use FIFOs to buffer digital data from an A/D converter, or to buffer the data before or after bus transmission.
floating signal sources	Signal sources with voltage signals that are not connected to an absolute reference of system ground. Also called nonreferenced signal sources. Some common examples of floating signal sources are batteries, transformers, and thermocouples.
FPGA	Field-programmable gate array.

G

gain	The factor by which a signal is amplified, often expressed in dB. Gain as a function of frequency is commonly referred to as the magnitude of the frequency response function.
grounded signal sources	Signal sources with voltage sources that are referenced to a system ground such as the earth or building ground. Also called referenced signal sources.

H

h	Hour.
Hz	Hertz.

I

I/O	Input/output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
in.	Inches.
INL	Integral nonlinearity—For an ADC, deviation of codes of the actual transfer function from a straight line.
I_{OH}	Current, output high.
I_{OL}	Current, output low.
IRQ	Interrupt request.

L

LED	Light-emitting diode—A semiconductor light source.
LSB	Least significant bit.

M

m	Meter.
master	A functional part of a MXI/VME/VXIbus device that initiates data transfers on the backplane. A transfer can be either a read or a write.
measurement device	DAQ devices such as the E Series multifunction I/O (MIO) devices, SCXI signal conditioning modules, and switch modules.
module	A board assembly and its associated mechanical parts, front panel, optional shields, and so on. A module contains everything required to occupy one or more slots in a mainframe. SCXI and PXI devices are modules.
MSB	Most significant bit.
mux	Multiplexer—A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

NI	National Instruments.
NI-DAQ	Driver software included with all NI measurement devices. NI-DAQ is an extensive library of VIs and functions you can call from an application development environment (ADE), such as LabVIEW, to program all the features of an NI measurement device, such as configuring, acquiring and generating data from, and sending data to the device.
NI-DAQmx	The latest NI-DAQ driver with new VIs, functions, and development tools for controlling measurement devices. The advantages of NI-DAQmx over earlier versions of NI-DAQ include the DAQ Assistant for configuring channels and measurement tasks for your device for use in LabVIEW, LabWindows/CVI, and Measurement Studio; increased performance such as faster single-point analog I/O; and a simpler API for creating DAQ applications using fewer functions and VIs than earlier versions of NI-DAQ.

noise	An undesirable electrical signal. Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

P

PCI	Peripheral Component Interconnect—A high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It offers a theoretical maximum transfer rate of 132 Mbytes/s.
pd	Pull-down.
PFI	Programmable function interface.
PGIA	Programmable gain instrumentation amplifier.
physical channel	*See* channel.
port	1. A communications connection on a computer or a remote controller. 2. A digital port consisting of four or eight lines of digital input and/or output.
ppm	Parts per million.
pseudodifferential channels	Pseudodifferential channels are all referred to a common ground, but this ground is not directly connected to the computer ground. Often this connection is made by a relatively low value resistor to give some isolation between the two grounds.
pu	Pull-up.
PXI	PCI eXtensions for Instrumentation—PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

Q

quantization	The process of converting an analog signal to a digital representation. Normally performed by an analog-to-digital converter (A/D converter or ADC).

R

range	The maximum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics.
referenced signal sources	Signal sources with voltage signals that are referenced to a system ground such as the earth or a building ground. Also called ground signal sources.
rise time	The time for a signal to transition from 10% to 90% of the maximum signal amplitude.
rms	Root mean square.
RTSI bus	Real-Time System Integration bus—The National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions.

S

s	Seconds.
S	Samples.
S/s	Samples per second—Used to express the rate at which a digitizer or D/A converter or DAQ device samples an analog signal.
scatter-gather	The term used to describe very high-speed DMA burst-mode transfers that are made only by the bus master, and where noncontiguous blocks of memory are transparently mapped by the controller to appear as a seamless piece of memory.
SCXI	Signal Conditioning eXtensions for Instrumentation—The National Instruments product line for conditioning low-level signals within an external chassis near sensors so that only high-level signals are sent to DAQ devices in the noisy PC environment. SCXI is an open standard available for all vendors.
sensor	A device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on) and produces a corresponding electrical signal.
settling time	The amount of time required for a voltage to reach its final value within specified limits.

signal conditioning	The manipulation of signals to prepare them for digitizing.
system noise	A measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded.

T

task	NI-DAQmx—A collection of one or more channels, timing, and triggering and other properties that apply to the task itself. Conceptually, a task represents a measurement or generation you want to perform.
terminal count	The highest value of a counter.
t_{gh}	Gate hold time.
t_{gsu}	Gate setup time.
t_{gw}	Gate pulse width.
THD	Total harmonic distortion—The ratio of the total rms signal due to harmonic distortion to the overall rms signal, in dB or percent.
THD+N	Signal-to-THD plus noise—The ratio in decibels of the overall rms signal to the rms signal of harmonic distortion, plus noise introduced.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
t_{off}	An offset (delayed) pulse; the offset is t nanoseconds from the falling edge of the AI CONV CLK* signal.
t_{out}	Output delay time.
t_p	Period of a pulse train.
Traditional NI-DAQ (Legacy)	An upgrade to the earlier version of NI-DAQ. Traditional NI-DAQ (Legacy) has the same VIs and functions and works the same way as NI-DAQ 6.9.*x*. You can use both Traditional NI-DAQ (Legacy) and NI-DAQmx on the same computer, which is not possible with NI-DAQ 6.9.*x*.
transducer	*See* sensor.
TRIG	Trigger signal.

t_{sc}	Source clock period.
t_{sp}	Source pulse width.
TTL	Transistor-transistor logic—A digital circuit composed of bipolar transistors wired in a certain manner. A typical medium-speed digital technology. Nominal TTL logic levels are 0 and 5 V.

V

V	Volts.
V_{CC}	Nominal +5 V power supply provided by the PC motherboard.
V_{cm}	Common-mode noise and ground potential.
VDC	Volts direct current.
VI, virtual instrument	1. A combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument. 2. A LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program.
V_{IH}	Volts, input high.
V_{IL}	Volts, input low.
V_{in}	Volts in.
V_m	Measured voltage.
V_{OH}	Volts, output high.
V_{OL}	Volts, output low.
V_{OUT}	Volts out.
V_{rms}	Volts, root mean square.
V_s	Ground-referenced signal source.
virtual channel	*See* channel.

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