TelCom Semiconductor, Inc.

EVALUATION KIT AVAILABLE

TC520A

SERIAL INTERFACE ADAPTER FOR TC500 A/D CONVERTER FAMILY

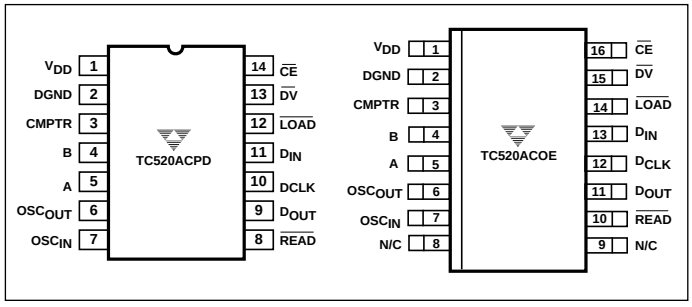
FEATURES

- **Converts TC500/500A/510/514 to Serial Operation**
- **Programmable Conversion Rate and Resolution for Maximum Flexibility**
- **Supports up to 17 Bits of Accuracy Plus Polarity Bit**
- **Low Power Operation: Typically 7.5mW**
- **14-Pin DIP or 16-Pin SOIC Packages**
- **Polled or Interrupt Mode Operation**

ORDERING INFORMATION

Part No.	Package	Operating Temp. Range
TC520ACOE	16-Pin SOIC (Wide)	0°C to +70°C
TC520ACPD	14-Pin DIP	0°C to +70°C
TC500EV	***Evaluation Kit for TC500 Family***	

PIN CONFIGURATION



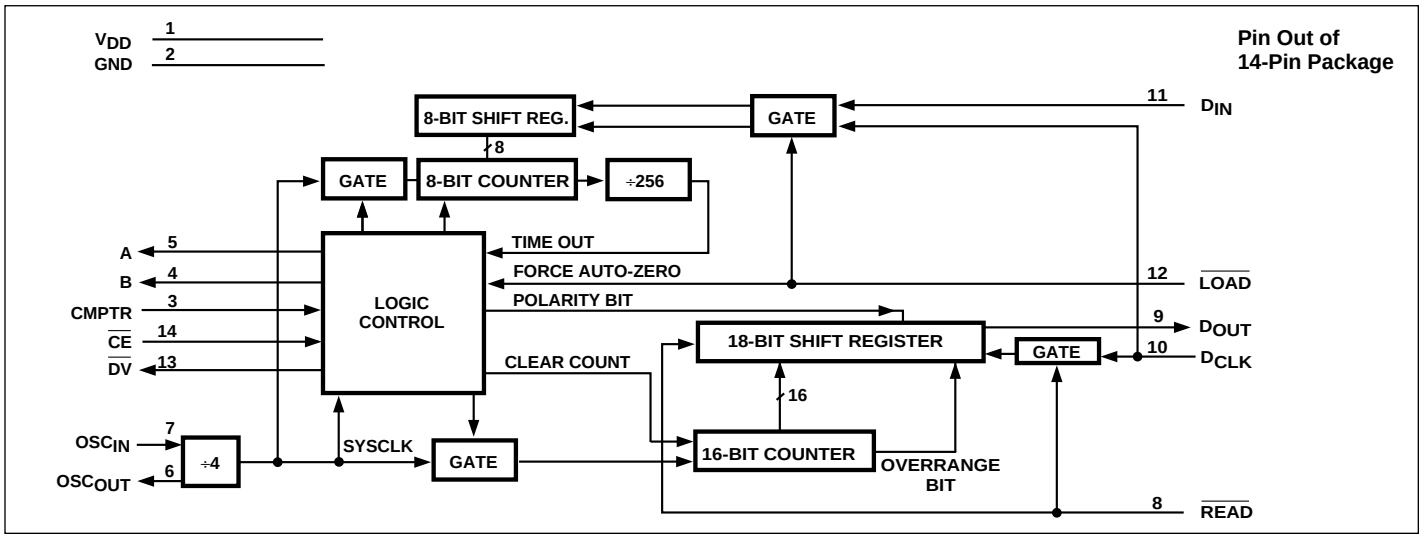
GENERAL DESCRIPTION

The TC520A Serial Interface Adapter provides logic control for TelCom's TC500/500A/510/514 family of dual slope, integrating A/D converters. It directly manages TC500 converter phase control signals A, B, and CMPTR thereby reducing host processor task loading and software complexity. Communication with the TC520A is accomplished over a 3 wire serial port. Key converter operating parameters are programmable for complete user flexibility.

Data conversion initiated when the $\overline{CE}$ input is brought low. The converted data (plus overrange and polarity bits) are held in an 18 bit shift register until read by the processor, or until the next conversion is completed. Data may be clocked out of the TC520A at any time, and at any rate the user prefers. A Data Valid ($\overline{DV}$) output is driven active at the start of each conversion cycle indicating the 18 bit shift register update has just been completed. This signal may be polled by the processor, or can be used as data ready interrupt.

The TC520A timebase can be derived from an external frequency source of up to 6MHz; or can operate from its own external crystal. It requires a single 5V logic supply and dissipates less than 7.5mW.

FUNCTIONAL BLOCK DIAGRAM



NOTE: All electrical data is included for reference only. Values are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage (V_{DD}) ..... +6.0V
Input Voltage, All Inputs (V_{IN}) ..... – 0.3V to V_{DD} +0.3V
Operating Temperature Range (T_A) ..... 0°C to +70°C
Storage Temperature Range (T_{STG}) ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) (T_{SDR}) ..... +300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Operational Specifications is not implied. Any exposure to Absolute Maximum Rating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = 5V, f_{osc} = 1 MHz, T_A = +25°C, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD}	Operating Voltage Range	4.5	5	5.5	V
I_{DD}	Supply Current	—	0.8	1.5	mA
Input Characteristics					
V_{IL}	Low Input Voltage	—	—	0.8	V
V_{IH}	High Input Voltage	2.0	—	—	V
I_{IL}	Input Leakage Current	—	—	10	µA
I_{PD}	Pull-down Current ($\overline{CE}$)	—	5	—	µA
I_{PU}	Pull-up Current ($\overline{READ}$, $\overline{LOAD}$)	—	5	—	µA
Output Characteristics (I_{OUT} = 250 µA, V_{DD} = 5V)					
V_{OL}	Low Output Voltage	—	0.2	0.3	V
V_{OH}	High Output Voltage	3.5	4.3	—	V
t_R, t_F	C_L = 10pF, Rise/Fall Times	—	—	250	nsec
Oscillator (OSC_{IN}, OSC_{OUT})					
f_{XTL}	Crystal Frequency	—	1.0	4.0	MHz
f_{OSC}	External Frequency (OSC_{IN})	—	—	6.0	MHz
Timing Characteristics					
t_{RD}	READ Delay Time	250	—	—	nsec
t_{RS}	$\overline{Data}$ Read Setup Time	1	—	—	µsec
t_{DRS}	D_{CLK} to D_{OUT} Delay	450	—	—	nsec
t_{LS}	LOAD Setup Time	1	—	—	µsec
t_{DLS}	$\overline{Data}$ Load Setup Time	50	—	—	nsec
t_{PWL}	D_{CLK} Pulse Width Low Time	150	—	—	nsec
t_{PWH}	D_{CLK} Pulse Width High Time	150	—	—	nsec
t_{LDL}	Load Default Low Time	250	—	—	nsec
t_{LDS}	Load Default Setup Time	250	—	—	nsec
Parameter					
t_{IZ}	Integrator ZERO Time	—	0.5	—	msec
t_{AZI}	Autozero (RESET) Time at Power-Up	—	100	—	msec

DETAILED DESCRIPTION

The TC520A input and output signals are outlined in the table below.

PIN DESCRIPTIONS

Pin No. 14-Pin PDIP Package	Pin No. 16-Pin SOIC Package	Symbol	Description
1	1	V_{DD}	Input. +5V ±10% power supply input with respect to DGND.
2	2	DGND	Input. Digital Ground.
3	3	CMPTR	Input, active high or low (depending on polarity of the voltage input to A/D converter). This pin connects directly to the zero-crossing comparator output (CMPTR) of the TC5xx A/D converter. A High-to-Low state change on this pin causes the TC520A to terminate the de-integrate phase of conversion.
4	4	B	Output, active high. The A and B outputs of the TC520A connect directly to the A and B inputs of the TC5xx A/D converter connected to the TC520A. The binary code on A, B determines the conversion phase of the TC5xx A/D converter: (A, B) = 01 places the TC5xx A/D converter into the Auto Zero phase; (A, B) =10 for Integrate phase (INT); (A, B) =11 for De-integrate phase (D_{INT}) and (A, B) = 00 for Integrator Zero phase (IZ). Please see the TC500 family data sheets for a complete description of these phases of operation.
5	5	A	Output, active high. See pin 4 description above.
6	6	OSC_{OUT}	Input. This pin connects to one side of an AT-cut crystal having a effective series resistance of 100Ω (typ) and a parallel capacitance of 20pF (typ). If an external frequency source is used to clock the TC520A, this pin must be left floating.
7	7	OSC_{IN}	Input. This pin connects to the other side of the crystal described in pin 6 above. The TC520A may also be clocked from an external frequency source connected to this pin. The external frequency source must be a pulse train having a duty cycle of 30% (minimum); rise and fall times of 15nsec and a min/max amplitude of 0 to V_{IH}. If an external frequency source is used, pin 6 must be left floating. A maximum operating frequency of 4MHz (crystal) or 6MHz (external clock source) is permitted.
	8	N/C	No connection on 16 pin package version.
	9	N/C	No connection on 16 pin package version.
8	10	$\overline{READ}$	Input, active low, level and negative edge triggered. A high-to low transition on $\overline{READ}$ loads serial port output shift register with the most recent converted data. Data is loaded such that the first bit transmitted from the TC520A to the processor is the overrange bit (OVR), followed by the polarity bit (POL) (high = input positive; low = input negative). This is followed by a 16 bit data word (MSB first). (OVR is available at the D_{OUT} as soon as $\overline{READ}$ is brought low. This bit may be used as the 17th data bit if so desired.) The D_{OUT} pin of the serial port is enabled only when $\overline{READ}$ is held low. Otherwise, D_{OUT} remains in a high impedance state. A serial port read access cycle is terminated at any time by bringing $\overline{READ}$ high.
9	11	D_{OUT}	Output, logic level. Serial port output pin. This pin is enabled only when $\overline{READ}$ is low (see $\overline{READ}$ pin description).
10	12	D_{CLK}	Input, positive and negative edge triggered. Serial port clock. With $\overline{READ}$ low, serial data is clocked into the TC520A at each low-to-high transition of D_{CLK}, and clocked out of the TC520A on each high-to-low transition of D_{CLK}. A maximum serial port D_{CLK} frequency of 3MHz is permitted.

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PIN DESCRIPTIONS (Cont.)

Pin No. 14-Pin PDIP Package	Pin No. 16-Pin SOIC Package	Symbol	Description
11	13	D_{IN}	Input, logic level. Serial port input pin. The TC5xx A/D converter integration time (TINT) and Autozero time (TAZ) values are determined by the LOAD VALUE byte clocked into this pin. This initialization must take place at power up, and can be rewritten (or modified and rewritten) at any time. The LOAD VALUE is clocked into D_{IN} MSB first.
12	14	$\overline{LOAD}$	Input, active low; level and edge triggered. The LOAD VALUE is clocked into the 8 bit shift register on board the TC520A while $\overline{LOAD}$ is held low. The LOAD VALUE is then transferred into the TC520A internal timebase counter (and becomes effective) when $\overline{LOAD}$ is returned high. If so desired, $\overline{LOAD}$ can be momentarily pulsed low (eliminating the need to clock a LOAD VALUE into D_{IN}). In this case, the current state of D_{IN} is clocked into the TC520A timebase counter selecting either a count of 65536 (D_{IN} = High), or count of 32768 (D_{IN} = Low).
13	15	$\overline{DV}$	Output, active low. $\overline{DV}$ is brought any time the TC520A is in the AZ phase of conversion. This occurs when either the TC520A initiates a normal AZ phase by setting A, B, equal to 01; or when $\overline{CE}$ is pulled high (which overrides the normal A, B sequencing and forces an AZ state). $\overline{DV}$ is returned high when the TC520A exits AZ.
14	16	$\overline{CE}$	Input, active low, level triggered. Conversion will be continuously performed as long as $\overline{CE}$ remains low. Pulling $\overline{CE}$ high causes the conversion process to be halted, and forces the TC520 into the AZ mode for as long as $\overline{CE}$ remains high. $\overline{CE}$ should be taken high whenever it is necessary to momentarily suspend conversion (for example: to change the address lines of an input multiplexer). $\overline{CE}$ should be pulled high only when the TC520A enters an AZ phase (i.e. when $\overline{DV}$ is low). This is necessary to avoid excessively long integrator discharge times which could result in erroneous conversion. This pin should be grounded if unused. It should be left floating if a 0.01µF RESET capacitor is connected to it (see *Applications* section).

DETAILED DESCRIPTION (Cont.)

TC520A Timing

The TC520A consists of a serial port and state machine. The state machine provides control timing to both the TC5xx A/D converter connected to the TC520A, as well as sequential timing for TC520A internal operation. All timing is derived from the frequency source at OSC_{IN} and OSCout. This frequency source can be either an externally-provided clock signal, or external crystal. If an external clock is used, it must be connected to the OSC_{IN} pin and OSC_{OUT} must remain floating.

If a crystal is used, it must be connected between the OSC_{IN} and OSC_{OUT} and physically located as close to the OSC_{IN} and OSC_{OUT} pins as possible. The incoming frequency is internally divided by 4 and the resulting clock (SYSCLK) controls all timing functions.

TC5xx A/D Converter Control Signals

The TC520A control outputs (A, B) and control input (CMPTR) connect directly to the corresponding pins of the TC5xx A/D converter. A conversion is consummated when A, B have been sequenced through the required 4 phases of conversion: Auto Zero (AZ), Integrate (INT), De-integrate (D_{INT}) and Integrator Zero (IZ) (See Figure 1). The Auto Zero phase compensates for offset errors in the TC5xx A/D converter. The integrate phase connects the voltage to be converted to the TC5xx A/D converter input (resulting in an integrator output dv/dt directly proportional to the magnitude of the applied input voltage). Actual A/D conversion (counting) is initiated at the start of the D_{INT} phase and terminates when the integrator output crosses 0V. The integrator output is then forced to 0V during the IZ phase and the converter is ready for another cycle. Please see the TC500/500A/510/514 data sheet for a complete description of these phases.

The number of SYSCLK periods (counts) for the AZ and INT phases is determined by the LOAD VALUE. The LOAD VALUE is a single byte that must be loaded into the most significant byte of 16 bit counter on-board the TC520A during initialization. The lower byte of this counter is pre-loaded to a value of 0FFH (256_{10}) and cannot be changed.

The LOAD VALUE (upper 8 bits of the counter) can be programmed over a range of 0FFH to 00H (corresponding to

a range of AZ = INT = 256 counts to 65536 counts). (See Figure 2). The LOAD VALUE sets the number of counts for *both* the AZ and INT phases and directly affects resolution and speed of conversion. The *greater* the number of counts allowed for AZ and INT; the *greater* the A/D resolution, but the *slower* the conversion speed.

The time period required for the D_{INT} phase is a function of the amount of voltage stored on the integrator during the INT phase, and the value of V_{REF}. The D_{INT} phase is initiated by the TC520A immediately after the INT phase, and terminated when the TC5xx A/D converter changes the state of the CMPTR input of the TC520A (indicating a zero crossing). In general, the maximum number of counts chosen for D_{INT} is twice that of INT (with V_{REF} chosen at V_{IN} (max)/2). Choosing these values guarantees a full count (maximum resolution) during D_{INT} when $V_{IN} = V_{IN}$(max).

The IZ phase is initiated immediately following the D_{INT} phase maintained until the CMPTR input transitions high. This indicates the integrator is initialized and ready for another conversion cycle. This phase typically takes 2msec.

Serial Port Control Signals

Communication to and from the TC520A is accomplished over a 3 wire serial port. Data is clocked into D_{IN} on the rising edge of D_{CLK} and clocked out of D_{OUT} on the falling edge of D_{CLK}. $\overline{READ}$ must be low to read from the serial port and can be taken high at any time, which terminates the read cycle, and releases D_{OUT} to a high impedance state. Conversion data is shifted to the processor from D_{OUT} in the following order: Overrange bit (which can also be used as the 17th data bit), Polarity bit, conversion data (MSB first).

APPLICATIONS

TC500 Series A/D Converter Component Selection

The TC500/500A/510/514 data sheet details the equations necessary to calculate values for integration resistor (R_{INT}) and capacitor (C_{INT}); auto zero and reference capacitors C_{REF} and C_{AZ} and voltage reference V_{REF}. All equations apply when using the TC520A, except integration time (T_{INT}) and Autozero time (T_{AZ}) are functions of the SYSCLK period (timebase frequency and LOAD VALUE). TelCom offers a ready-to-use TC5xx A/D converter design tool on a 3 1/2 inch diskette (Windows format). The TC500 Design Spreadsheet is an Excel-based spreadsheet that calculates values for all components as well as the TC520A LOAD VALUE. It also calculates overall converter performance such as noise rejection, converter speed, etc. This software is included in the TC500EV hardware evaluation kit and is also available free of charge from your local TelCom representative.

TC520A Initialization

Initialization of the TC520A consists of:

(1) Power-On RESET of the TC500/520A (forcing the TC520A into an AZ phase).

(2) Initializing the TC520A LOAD VALUE.

Power-On RESET

The TC520A powers-up with A, B = 00 (IZ Phase), awaiting a high logic state on CMPTR, which must be initiated by forcing the TC520A into the AZ phase. This can be accomplished in one of two ways:

(1) External hardware (processor or logic) can momentarily taking $\overline{LOAD}$ or $\overline{CE}$ low for a minimum of 100 msec (tAZI); or

(2) A .01µF RESET capacitor can be connected from $\overline{CE}$ to V_{CC} to generate a power-on pulse on $\overline{CE}$.

Load Value Initialization

The LOAD VALUE is the preset value (high byte of the SYSCLK timing counter) which determines the number of counts allocated to the AZ and INT phases of conversion. This value can be calculated using the TC520A spreadsheet within the TC500 Design Spreadsheet software, or can be set-up as shown in the following example:

(1) **Select V_{REF}, TD_{INT}**
Choose the TC5xx A/D converter reference voltage (V_{REF}) to be half of the maximum A/D converter input voltage. For example, if V_{IN} max = 2.5V; choose V_{REF} = 1.75V. This forces the maximum de-integration time (TD_{INT}) to be equal to twice the maximum integration time (T_{INT}) ensuring a full count (maximum resolution) during D_{INT}.

(2) **Calculate T_{INT}**
The TC520A counter length is 16 bits (65536). Allowing the full 65536 counts for TD_{INT} results in a maximum T_{INT} = 65536/2 or 32768.

(3) **Select SYSCLK Frequency**
SYSCLK frequency directly affects conversion time. The faster the SYSCLK, the faster the conversion time. The upper limit SYSCLK frequency is determined by the worst case delay of the TC500 comparator (which for the TC500 and TC500A is 3.2µsec). While a faster value for SYSCLK can be used, operation is optimized (error minimized) by choosing a SYSCLK period (1/SYSCLK frequency) that is greater than 3.2µsec. Choosing T_{SYSCLK} =

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4µsec makes the SYSCLK frequency equal to 250kHz. This makes the external crystal (or frequency source) equal to 1.0MHz (since SYSCLK = crystal frequency/4). Calculating integration time (in msec) using T_{SYSCLK} = 4µsec, T_{INT} = µsec x 32768 = 131msec.

(4) **Calculate Load Value**
Plug the T_{INT} and T_{SYSCLK} values into the equation and convert the resulting value to hexadecimal:

$$\text{LOAD VALUE} = \frac{[(65536 - (T_{INT}/T_{SYSCLK})]}{256}$$

In this example, LOAD VALUE = $128_{(10)}$ = 10H. Therefore, a LOAD VALUE of 10H is loaded to the TC520A. If the desired T_{INT} was 100msec instead of 131msec, the LOAD VALUE would be 9EH, and so on. The TC520A LOAD VALUE must be initialized on power-up, and can be re-initialized as often as desired thereafter. This is accomplished by bringing the $\overline{LOAD}$ input low while transmitting the appropriate LOAD VALUE to the TC520A as shown in Figure 1 and Figure 2.

Polled vs. Interrupt Operation

The TC520A can be accessed at any time by the host microprocessor. This makes operation in a polled environment especially easy since the most recently converted data is available to the processor as needed. The TC520A can also be used in an interrupt environment by connecting $\overline{DV}$ to the $\overline{IRQ}$ line of the processor. Since AZ is the first phase of a new conversion cycle, the most recently converted data will be available as soon as $\overline{DV}$ goes low. If so desired, the interrupt service routine can also modify the LOAD VALUE during the $\overline{DV}$ = low interval.

Opto-Isolated Applications

The 3 wire serial port of the TC520A can be opto-isolated for applications requiring isolated data acquisition. The additional control lines ($\overline{LOAD}$, $\overline{DV}$, $\overline{READ}$) are normally not needed in such applications, but can also be brought across the isolation barrier with the addition of a second isolator.

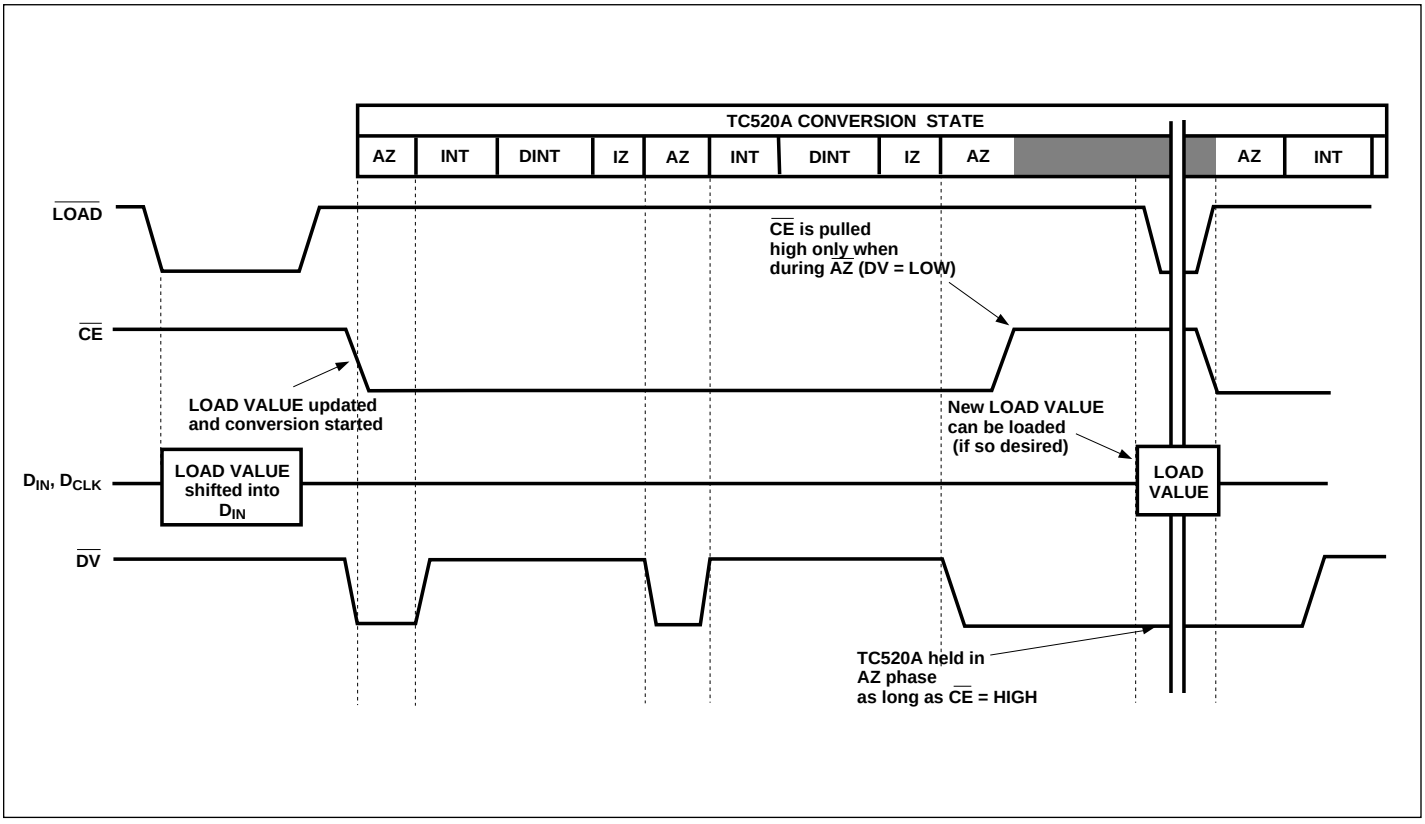


Figure 1. TC520A Initialization and Start/Stop Conversion Timing Relationships

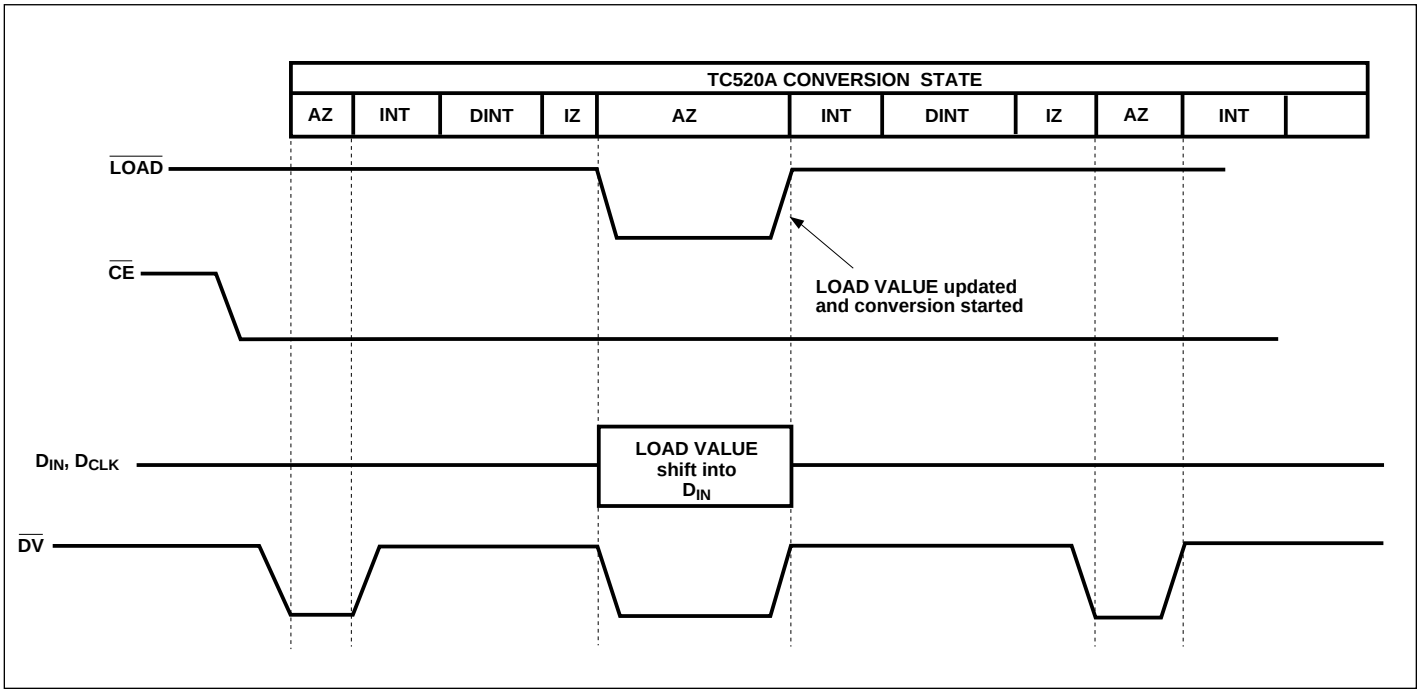


Figure 2. Load Value Modify Cycle

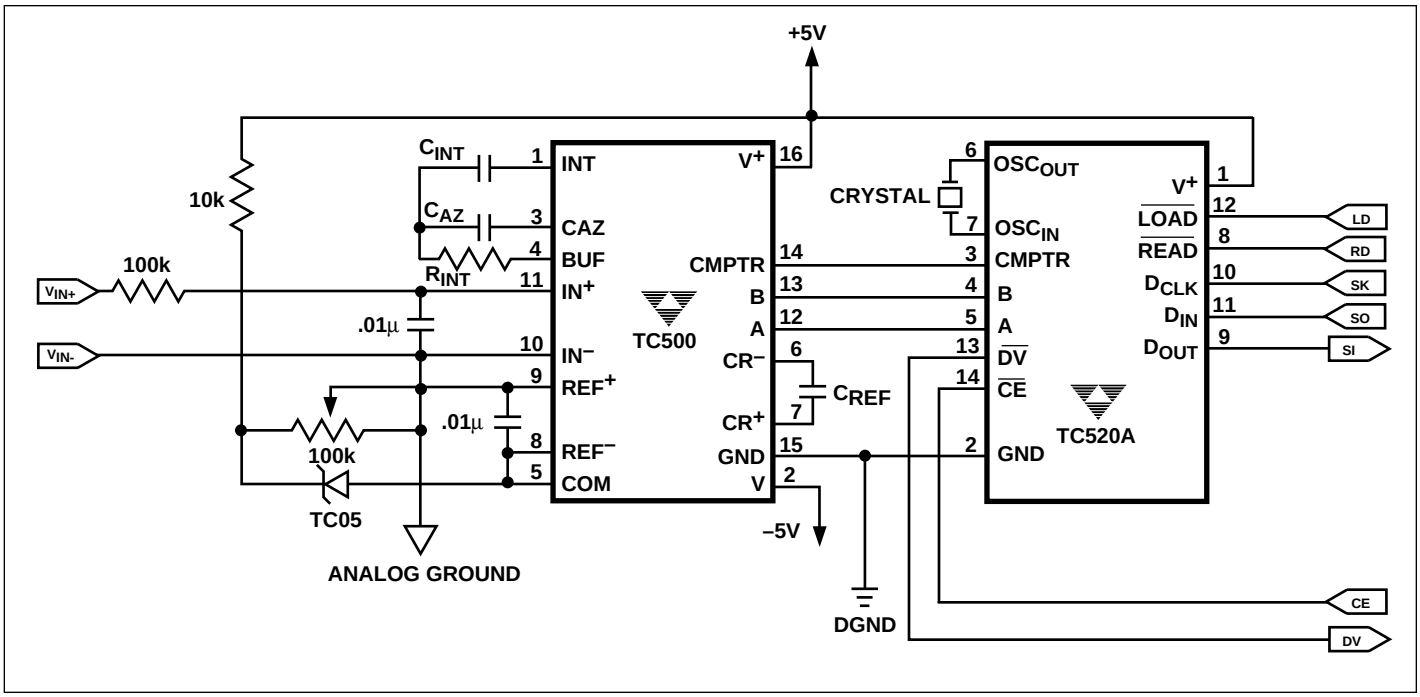


Figure 3. Typical System Application

TC520A

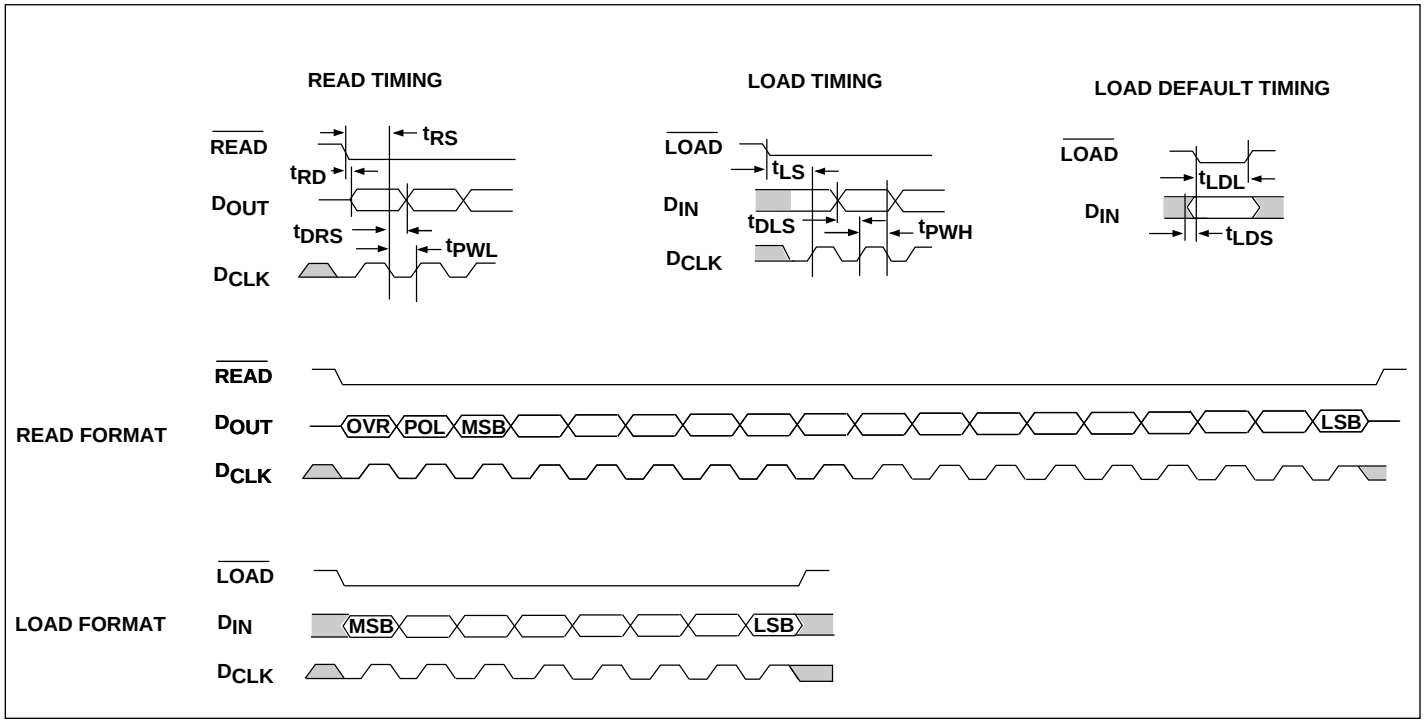
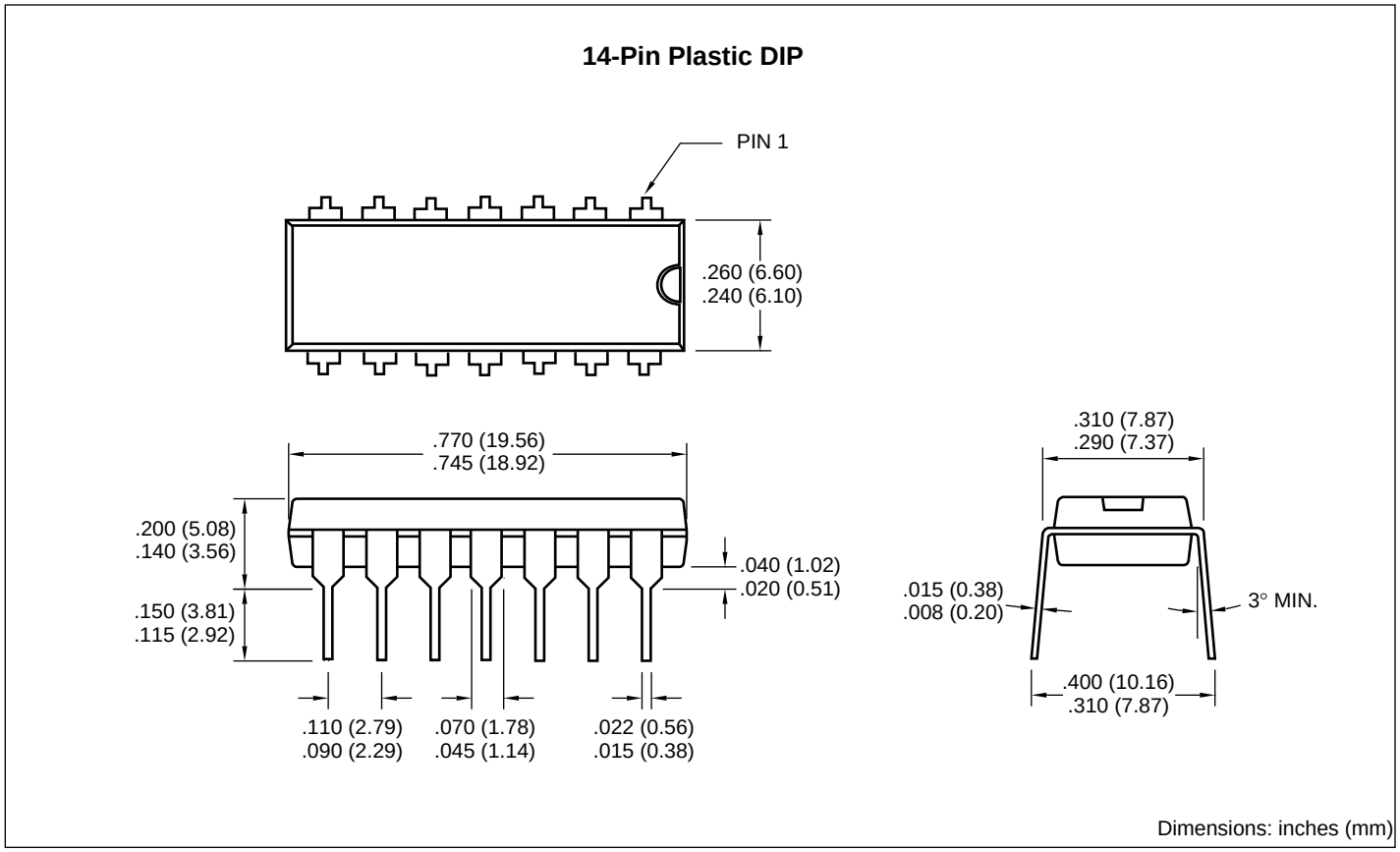


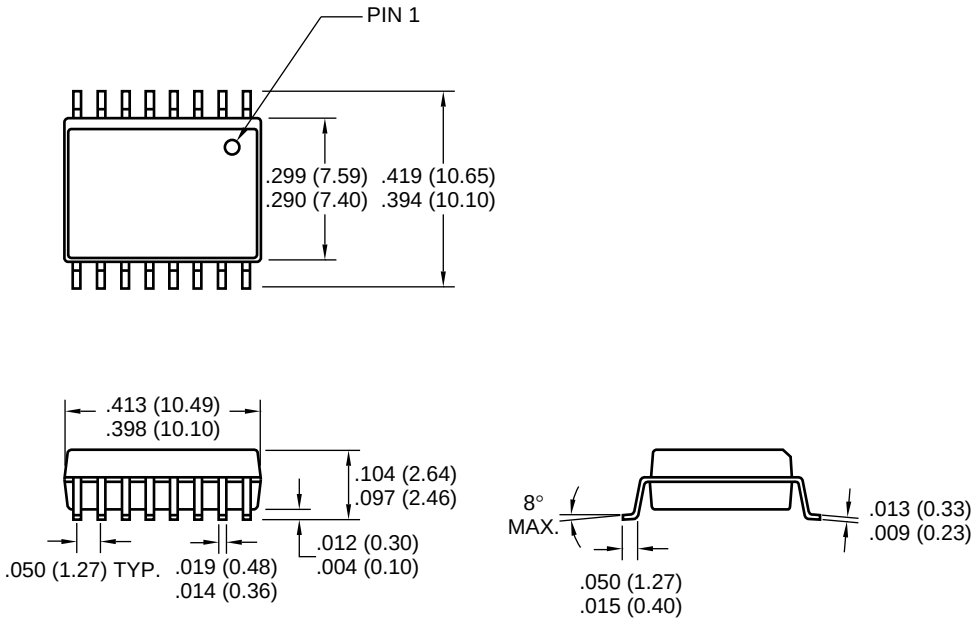
Figure 4. TC520A Timing Diagram

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS (Cont.)

16-Pin SOIC Wide



Dimensions: inches (mm)

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