PXIe-5163 Specifications

2022-07-11

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PXIe-5163 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges, bandwidths, and bandwidth-limiting filters
- Sample rate set to 1 GS/s
- Onboard sample clock locked to onboard reference clock
- 15-minute warm-up time at ambient temperature

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C
- Calibration cycle maintained
- Chassis configured:[1]
  - PXI Express chassis fan speed set to HIGH
  - Foam fan filters removed if present
  - Empty slots contain PXI chassis slot blockers and filler panels
- External calibration performed at 23 °C ± 3 °C
- Within ±5 °C of temperature at last self-calibration as reported by onboard temperature sensor

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ±1.25%, typical 1 MΩ ±0.5%, typical
Input capacitance (1 MΩ)	20.2 pF ±2.5 pF, typical

Input coupling	AC DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR)

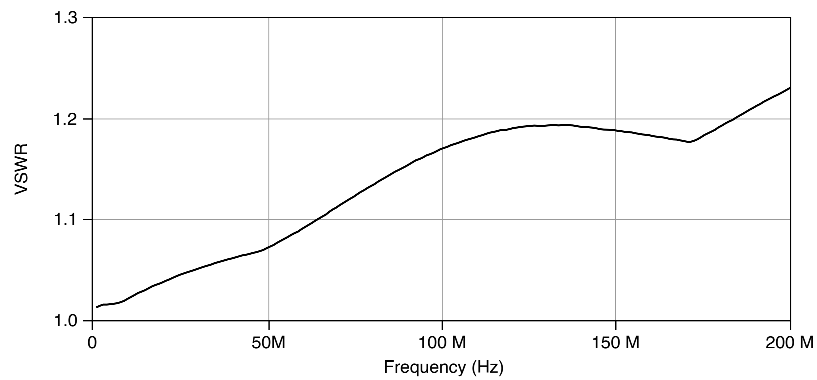
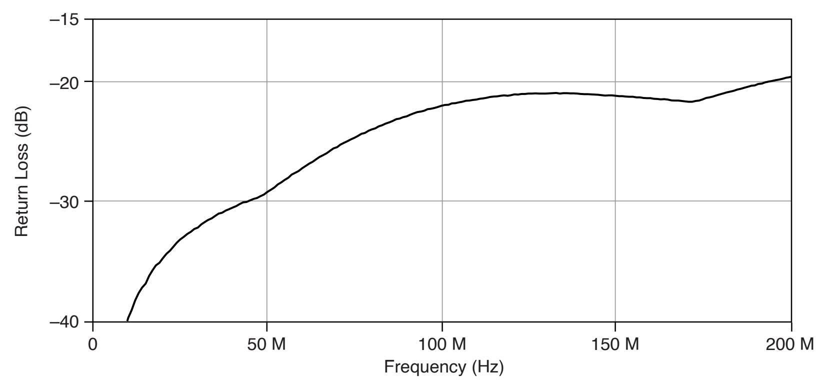


Figure 1. 50 Ω Input Return Loss



Voltage Levels

50 Ω FS input range (V_{pk-pk})	0.25 V 0.5 V 1 V 2.5 V 5 V

Input Range (V_{pk-pk})	Vertical Offset Range[2] (V)
0.25 V	±5
0.5 V	±5
1 V	±5
2.5 V	±10 or ±248.75
5 V	±10 or ±247.5
10 V	±10 or ±245
25 V	±50 or ±237.5
50 V	±50 or ±225
100 V	±50 or ±200

Table 1. 1 MΩ FS Input Range and Vertical Offset Range

Maximum input overload

50 Ω	|Peaks| ≤5 V
1 MΩ [3]	250 V RMS

Notice Signals exceeding the maximum input overload may cause damage to the device.

Accuracy

Resolution	14 bits

DC accuracy[4], [5]

50 Ω	±[(0.5% × |**Reading**|) + (0.2% of FS)], warranted
1 MΩ	±[(0.65% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (0.2% of FS) + 0.15 mV], warranted

DC drift[6]	±0.0013 dB per °C at 50 kHz
AC amplitude accuracy[4]	±0.225 dB at 50 kHz, warranted

Crosstalk Crosstalk is measured on one channel with a test signal applied to the other channel and the same range setting on both channels.

Frequency	Level
1 MHz	-100 dB
10 MHz	-100 dB
100 MHz	-85 dB
200 MHz	-75 dB

Table 2. 50 Ω Crosstalk

Frequency	Level	
	0.25 V to 10 V (V_{pk-pk})	25 V to 100 V (V_{pk-pk})
1 MHz	-85 dB	-70 dB
10 MHz	-85 dB	-70 dB
100 MHz	-75 dB	-55 dB
200 MHz	-70 dB	-50 dB

Table 3. 1 MΩ Crosstalk

Bandwidth and Transient Response

Bandwidth (-3 dB)[7],[8]	200 MHz, warranted

Bandwidth-limiting filters[7],[8]

Lowpass filters	20 MHz

	30 MHz
	150 MHz
Highpass filters	90 Hz
	450 Hz

Passband amplitude flatness (at <150 MHz)[7],[8]

50 Ω	±0.5 dB, warranted
1 MΩ	±0.7 dB, typical

AC-coupling cutoff (-3 dB)

50 Ω [9]	40 kHz
1 MΩ [8]	7.5 Hz

Rise/fall time[10]	2 ns

Figure 1. 50 Ω Full Bandwidth Frequency Response, 1 $V_{pk\text{-}pk}$, Measured

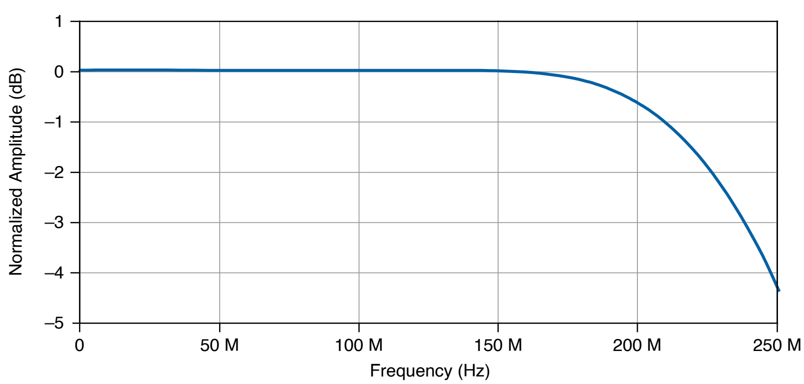


Figure 1. 50 Ω Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

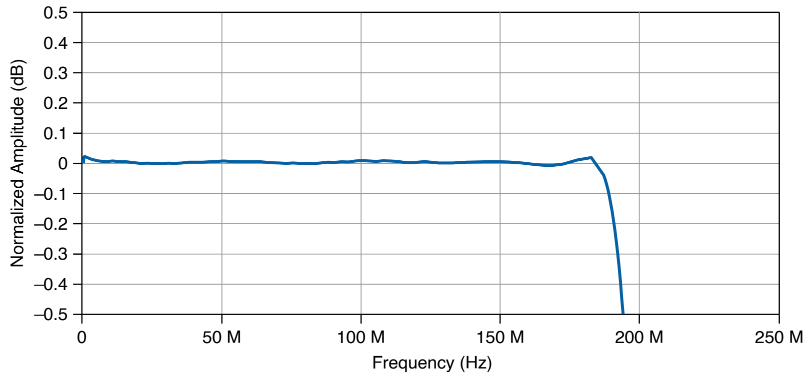


Figure 1. 50 Ω 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

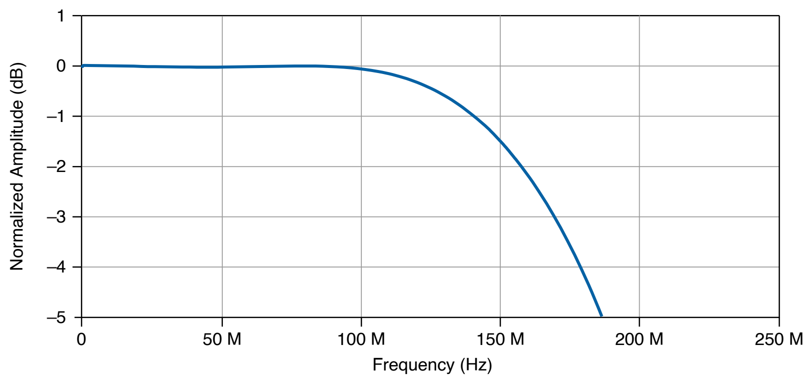


Figure 1. 1 MΩ Full Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

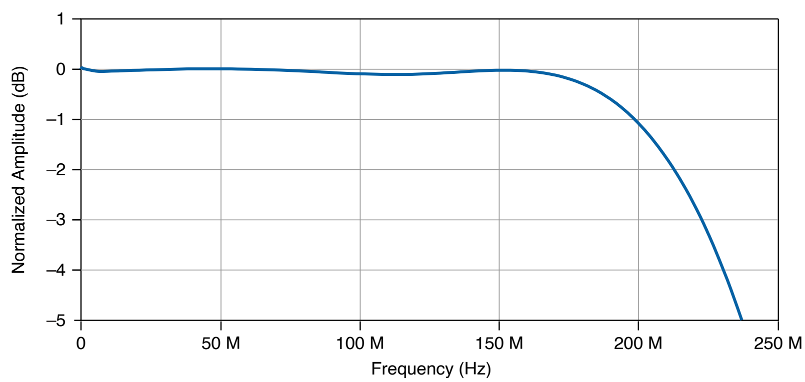


Figure 1. 1 MΩ Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

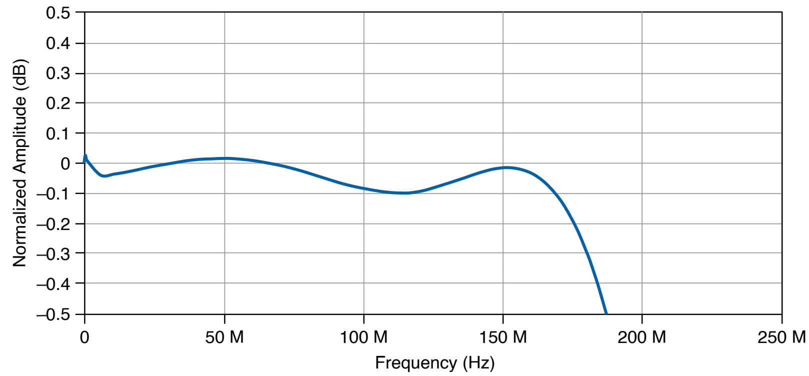
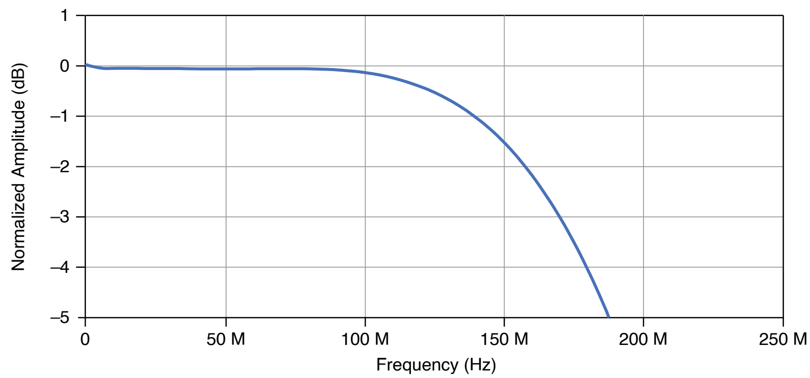


Figure 1. 1 MΩ 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured



Spectral Characteristics

50 Ω Spectral Characteristics Excludes ADC interleaving spurs. 1

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)
0.25 V	-70
0.5 V	-73
1 V	-73
2.5 V	-73
5 V	-70

Table 4. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	≥50 MHz to ≤100 MHz, Full Bandwidth (dBc)
0.25 V	-73	-69
0.5 V	-73	-72
1 V	-72	-70
2.5 V	-72	-68
5 V	-72	-69

Table 5. Total Harmonic Distortion (THD)[12]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	10.5	10.7
0.5 V	10.7	10.9
1 V	10.7	11.0
2.5 V	10.9	11.1
5 V	10.8	11.0

Table 6. Effective Number of Bits (ENOB)[11]

Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

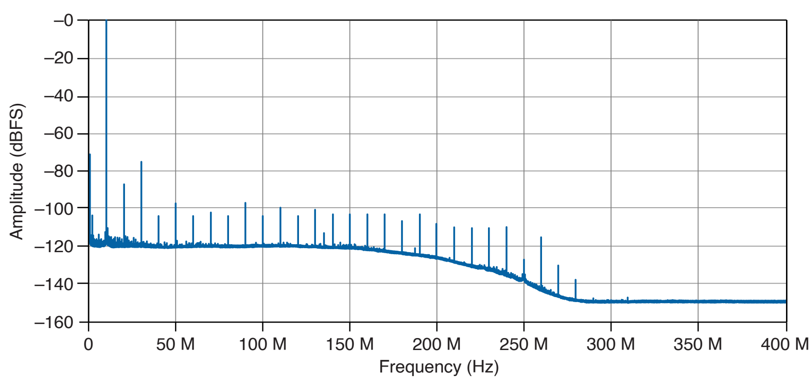


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk}Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured

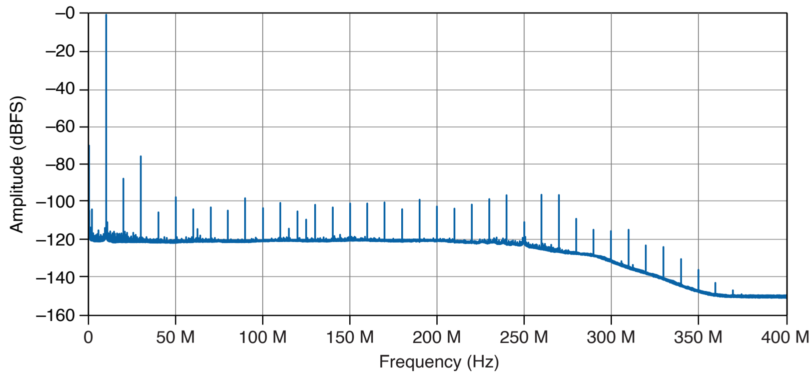
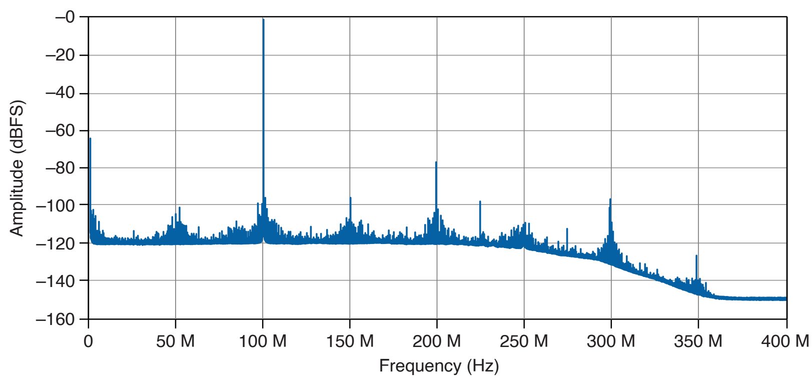


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk}Input Range, Full Bandwidth, 99.9 MHz Input Tone at -1 dBFS, Measured



1 MΩ Spectral Characteristics 1 , Verified using a 50 Ω source and 50 Ω feed-through terminator.

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)
0.25 V	-61
0.5 V	-56
1 V	-49
2.5 V	-58
5 V	-52

Table 7. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	≥50 MHz to ≤100 MHz, Full Bandwidth (dBc)
0.25 V	-72	-62
0.5 V	-67	-56
1 V	-60	-50
2.5 V	-69	-58
5 V	-63	-53

Table 8. Total Harmonic Distortion (THD)[12]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	10.5	10.7
0.5 V	10.7	10.9
1 V	10.7	11.0
2.5 V	10.9	11.1
5 V	10.8	11.0

Table 9. Effective Number of Bits (ENOB)[11]

Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

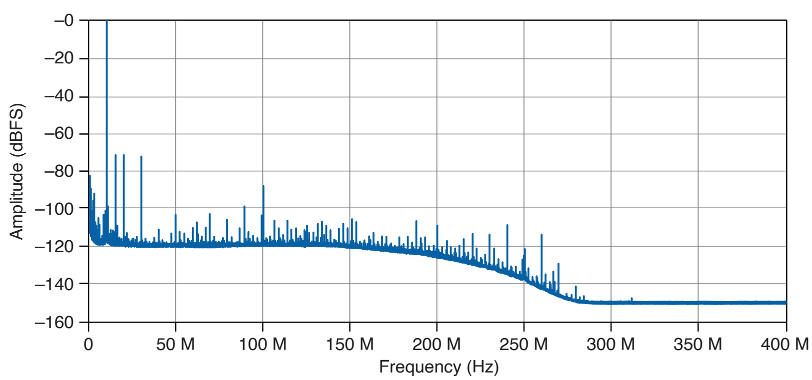
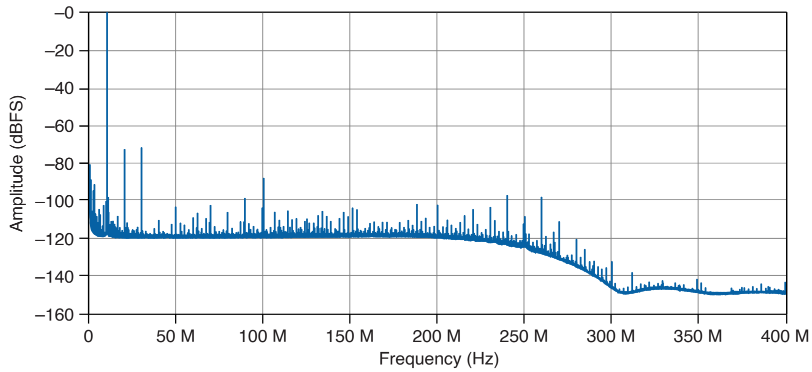


Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured



Noise[13]

50 Ω RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.045	0.018
0.5 V	0.040	0.018
1 V	0.035	0.017
2.5 V	0.030	0.017
5 V	0.030	0.014

Figure 1. 50 Ω Channel 0 Average Noise Density, 1 V_{pk-pk}Range, Measured

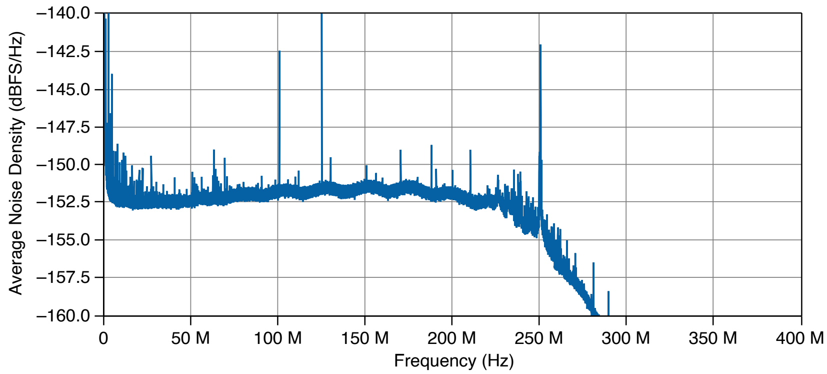
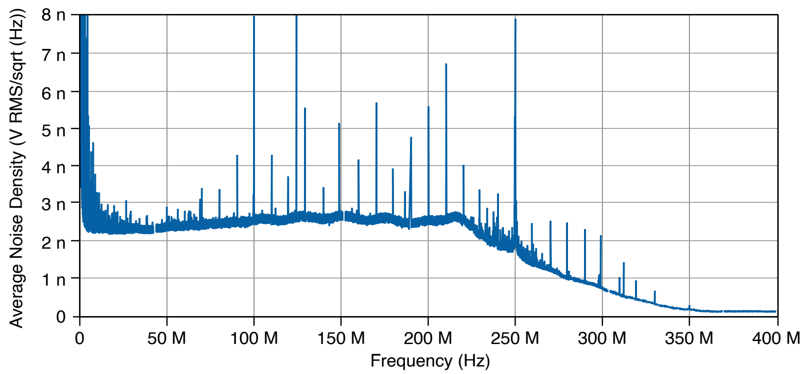


Figure 1. 50 Ω Channel 0 Average Noise Density, 0.25 V_{pk-pk} Range, Measured



1 MΩ RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.110	0.070
0.5 V	0.060	0.050
1 V	0.050	0.030
2.5 V	0.100	0.055
5 V	0.060	0.045
10 V	0.050	0.030
25 V	0.080	0.050

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
50 V	0.060	0.040
100 V	0.050	0.030

Horizontal

Sample Clock

Sources		
Internal	Onboard clock (internal VCTCXO)	
External	CLK IN (front panel SMB connector)	
	PXIe-DSTAR_A (backplane connector)	

Sample rate range, real-time[14]	15.259 kS/s to 1 GS/s
Timebase frequency	1.0 GHz

Timebase accuracy	
Phase-locked to onboard clock	±5 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy

Sample clock jitter[15]	500 fs RMS

Phase-Locked Loop (PLL) Reference Clock

Sources

Internal	Onboard clock (internal VCTCXO) PXI_CLK10 (backplane connector)
External (10 MHz)	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)

Duty cycle tolerance	45% to 55%, typical

External Sample Clock

Source	CLK IN (front panel SMB connector)
Impedance	50 Ω
Coupling	AC
Frequency	1.0 GHz
Input voltage range, when configured as a sample clock	632 $mV_{pk\text{-}pk}$ to 5 $V_{pk\text{-}pk}$ (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a sample clock	6 $V_{pk\text{-}pk}$
Duty cycle tolerance	45% to 55%, typical

External Reference Clock In

Sources	CLK IN (front panel SMB connector)

	AUX 0 CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC
Frequency[16]	10 MHz
Input voltage range, when configured as a reference clock	623 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a reference clock	6 V_{pk-pk}

Reference Clock Out

Source	PXI_CLK10 (backplane connector)
Destination	AUX 0 CLK OUT (front panel MHDMR connector)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±12 mA

Trigger

Supported triggers	Reference (stop) trigger Reference (arm) trigger

	Start trigger Advance trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 CH 1 SMB PFI 0 AUX 0 PFI <0..7> PXI_Trig <0..6> Software
Trigger delay	from 0 ns to 2.25×10^{15} ns ($(2^{51} - 1) \times$ **Sample Clock Period** ns)
Dead time	496 ns
Hold off	From dead time to 1.84×10^{19} ns ($(2^{64} - 1) \times$ **Sample Clock Period** ns)

Analog Trigger

Sources	CH 0 CH 1
Time resolution	
Interpolator enabled	**Sample Clock Period** / 1024 = 0.977 ps
Interpolator disabled	Sample clock period (1 ns)
Trigger filters	
Low Frequency (LF) Reject	100 kHz
High Frequency (HF) Reject	100 kHz
Trigger accuracy[17]	0.5% of FS
Trigger jitter[17]	15 ps RMS
Minimum threshold duration[18]	Sample clock period

Digital Trigger

Sources	PFI 0 (front panel SMB connector) AUX 0 PFI <0..7> (front panel MHDMR connector) PXI_Trig <0..6> (backplane connector)
Time resolution	8 ns

Programmable Function Interface

Connectors	AUX 0 PFI <0..7> (front panel MHDMR connector) PFI 0 (front panel SMB connector)
Direction	Bidirectional per channel

As an input (trigger)

Destination	Start trigger (acquisition arm) Reference (stop) trigger Arm reference trigger Advance trigger
Input impedance	49.9 kΩ
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	3.3 V
Maximum input overload	0 to 3.3 V (5 V tolerant)
Maximum frequency	50 MHz
Minimum pulse width	10 ns

As an output (event)

Sources	Ready for Start

	Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe compensation[19]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Maximum frequency	50 MHz
Minimum pulse width	10 ns

AUX 0 Connector Specifications

Connector	MHDMR
Voltage output	3.3 V ±10%
Maximum current drive on +3.3 V	200 mA

Output impedance on +3.3 V	<1 Ω

Waveform Specifications

Onboard memory size[20]	512 MB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (**Record Length** - 1)
Number of posttrigger samples	Zero up to **Record Length**
Maximum number of records in onboard memory[21]	1,398,101 for 512 MB

Channels	Bytes per Sample	Max Records per Channel	Record Length	Allocated Onboard Memory per Record
1	2	1,398,101	1	384
1	2	223,696	1,000	2,400
1	2	26,379	10,000	20,352
1	2	1	268,435,265	536,870,912
2	2	1,398,101	1	384
2	2	121,574	1,000	4,416
2	2	13,283	10,000	33,216
2	2	1	134,217,633	536,870,912

Table 10. Examples of Allocated Onboard Memory Per Record (512 MB Onboard Memory)

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at ni.com/manuals.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.
- Corrects the frequency response for all ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Interleaving spurs
- Intermodule synchronization errors

Refer to the **NI High-Speed Digitizers Help** for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[22]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE18.7.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5163. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can use InstrumentStudio to monitor, control, and record measurements from the PXIe-5163.

InstrumentStudio is an application that allows you to perform interactive measurements on several different NI device types in a single application.

Interactive control of the PXIe-5163 was first available via InstrumentStudio in NI-SCOPE18.7. InstrumentStudio is included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5163. MAX is included on the driver media.

Synchronization

Channel-to-channel skew, between the channels of a PXIe-5163	
50 Ω	<100 ps
1 MΩ	<150 ps

Note The channels of a PXIe-5163 are automatically synchronized when they are in the same NI-SCOPE session.

Synchronization with the NI-TClk API [23]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5163 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5163 modules using NI-TClk [24]	
NI-TClk synchronization without manual adjustment [25]	
Skew, peak-to-peak [26]	300 ps, typical
NI-TClk synchronization with manual adjustment [25]	
Skew, average	≤10 ps
Sample Clock delay/adjustment resolution	3.5 ps

Power Requirements

Current draw	
+3.3 V DC	1.97 A
+12 V DC	1.63 A
Power draw	
+3.3 V DC	6.5 W
+12 V DC	19.5 W
Total	26 W

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 module 21.26 cm × 12.88 cm × 2.0 cm (8.37 in. × 5.07 in. × 0.787 in.)
Weight	460 g (16.2 oz)

Bus Interface

Form factor	PXI Express (x8 Gen 2)
Slot compatibility	PXI Express or hybrid

Environmental Characteristics

Temperature	
Operating	0 °C to 50 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	4,600 m (570 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

[1] For more information about cooling, refer to the **Maintain Forced-Air Cooling Note to Users** available at ni.com/manuals.

[2] For input ranges between 2.5 V_{pk-pk} and 100 V_{pk-pk}, two offset ranges are possible. The driver software automatically picks the offset range that provides the highest resolution and accuracy.

[3] Derate above 500 kHz at 20 dB/dec until 5 MHz, then derate at 10 dB/dec.

[4] Within ±5 °C of self-calibration temperature.

[5] Applies after averaging data for 8.5 ms.

[6] Used to calculate errors when onboard temperature changes more than ±3 °C from the self-calibration temperature.

[7] Normalized to 50 kHz.

[8] For 1 MΩ mode, verified using a 50 Ω source and 50 Ω feed-through terminator.

[9] Verified using a 50 Ω source.

[10] 50% FS input pulse.

[11] -1 dBFS input signal corrected to FS. 1 kHz resolution bandwidth.

[12] 1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics.

[13] Verified with 50 Ω terminator connected directly to BNC input.

[14] Divide by **n** decimation from 1.0 GS/s used for all rates less than 1.0 GS/s. For more information about the sample clock and decimation, refer to the **NI High-Speed Digitizers Help**.

[15] Integrated from 100 Hz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

[16] The PLL reference clock must be accurate to ±25 ppm.

[17] Analog triggers. For input frequencies less than 150 MHz.

[18] Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

[19] 1 kHz, 50% duty cycle square wave, SMB PFI 0 only.

[20] Onboard memory is shared among all enabled channels.

[21] You can exceed these numbers if you fetch records while acquiring data. For more information, refer to the **NI High-Speed Digitizers Help**.

[22] Warm-up begins after the chassis and controller or PC is powered and NI-SCOPE is loaded and recognizes the PXIe-5163.

[23] NI-TClk installs with NI-SCOPE.

[24] Specifications are valid under the following conditions:

- All modules installed in the same PXI Express chassis
- NI-TClk used to align the sample clocks of each module
- Modules synchronized without using an external sample clock
- All parameters set to identical values for each module
- Self-calibration completed

[25] Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.

[26] **Skew** is the misalignment between module timing across slots of a chassis and is caused by clock and analog path delay differences.