# PCIe-5774 Specifications

2022-07-11

# Contents

# PCIe-5774 Specifications

## Definitions

**Warranted** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

**Characteristics** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

## Digital I/O

| | |
|---|---|
| Connector | Molex™ Nano-Pitch I/O™ |
| 5.0 V Power | ±5%, 50 mA maximum, nominal |

| Signal | Type | Direction |
|---|---|---|
| MGT Tx± <0..3>[1] | Xilinx UltraScale GTH | Output |
| MGT Rx± <0..3>[1] | Xilinx UltraScale GTH | Input |
| DIO <0..7> | Single-ended | Bidirectional |
| 5.0 V | DC | Output |
| GND | Ground | — |

Table 1. Digital I/O Signal Characteristics

## Digital I/O Single-Ended Channels

| | |
|---|---|
| Number of channels | 8 |
| Signal type | Single-ended |
| Voltage families | 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V |
| Input impedance | 100 kΩ, nominal |
| Output impedance | 50 Ω, nominal |
| Direction control | Per channel |
| Minimum required direction change latency | 200 ns |
| Maximum output toggle rate | 60 MHz with 100 µA load, nominal |

| Voltage Family (V) | $V_{IL}$ (V) | $V_{IH}$ (V) | $V_{OL}$ (100 µA Load) (V) | $V_{OH}$ (100 µA Load) (V) | Maximum DC Drive Strength (mA) |
|---|---|---|---|---|---|
| 3.3 | 0.8 | 2.0 | 0.2 | 3.0 | 24 |
| 2.5 | 0.7 | 1.6 | 0.2 | 2.2 | 18 |
| 1.8 | 0.62 | 1.29 | 0.2 | 1.5 | 16 |
| 1.5 | 0.51 | 1.07 | 0.2 | 1.2 | 12 |
| 1.2 | 0.42 | 0.87 | 0.2 | 0.9 | 6 |

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2]

## Digital I/O High-Speed Serial MGT[3]

**Note** MGTs are available on devices with KU060 FPGAs only.

| | |
|---|---|
| Data rate | 500 Mbps to 16.375 Gbps, nominal |
| Number of Tx channels | 4 |
| Number of Rx channels | 4 |
| I/O AC coupling capacitor | 100 nF |

## MGT TX± Channels[4]

| | |
|---|---|
| Minimum differential output voltage[5] | 170 mV pk-pk into 100 Ω, nominal |
| I/O coupling | AC-coupled, includes 100 nF capacitor |

## MGT RX± Channels

| | |
|---|---|
| **Differential input voltage range** | |
| ≤ 6.6 Gb/s | 150 mV pk-pk to 2000 mV pk-pk, nominal |
| > 6.6 Gb/s | 150 mV pk-pk to 1250 mV pk-pk, nominal |
| Differential input resistance | 100 Ω, nominal |
| I/O coupling | DC-coupled, requires external capacitor |

## Reconfigurable FPGA

PCIe-5774 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PCIe-5774 FPGA options.

| | KU035 | KU060 |
|---|---|---|
| LUTs | 203,128 | 331,680 |
| DSP48 slices<br>(25 × 18 multiplier) | 1,700 | 2,760 |
| Embedded Block RAM | 19.0 Mb | 38.0 Mb |
| Data Clock Domain | 200 MHz, 16 samples per cycle per channel (dual channel mode),<br>32 samples per cycle (single channel mode) | |
| Timebase reference sources | Onboard 100 MHz oscillator | |
| Data transfers | DMA, interrupts, programmed I/O | DMA, interrupts, programmed I/O, multi-gigabit transceivers |
| Number of DMA channels | 60 | |

Table 3. Reconfigurable FPGA Options

**Note** The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

## Onboard DRAM

| | |
|---|---|
| Memory size | 4 GB (2 banks of 2 GB) |
| DRAM clock rate | 1064 MHz |
| Physical bus width | 32 bit |
| LabVIEW FPGA DRAM clock rate | 267 MHz |
| LabVIEW FPGA DRAM bus width | 256 bit per bank |
| Maximum theoretical data rate | 17 GB/s (8.5 GB/s per bank) |

## Analog Input

# General Characteristics

| | |
|---|---|
| Number of channels | 2, single-ended, simultaneously sampled |
| Connector type | SMA |
| Input impedance | 50 Ω, nominal |
| Input coupling | DC |
| **Sample Clock** | |
| Internal Sample Clock[6] | 3.2 GHz |
| External Sample Clock[6] | 3.2 GHz |
| **Sample Rate** | |
| Dual channel mode | 3.2 GS/s per channel |
| Single channel mode | 6.4 GS/s |
| Analog-to-digital converter (ADC) | ADC12DJ3200, 12-bit resolution |

# Typical Specifications

| | |
|---|---|
| Full-scale input ranges | 200 mV pk-pk<br>1 V pk-pk |
| **Gain accuracy** | |

| | |
|---|---|
| 200 mV range | ±1.47% |
| 1 V range | ±1.44% |

**DC offset**

| | |
|---|---|
| 200 mV range | ±0.628 mV |
| 1 V range | ±1.269 mV |

| | |
|---|---|
| Vertical offset range | ±0.5 full-scale, nominal |

**Bandwidth (-3 dB)**[7]

| | |
|---|---|
| -01 variant | 200 mV range: 3.00 GHz |
| | 1 V range: 2.85 GHz |
| -02 variant | 200 mV range: 1.63 GHz |
| | 1 V range: 1.62 GHz |

| | Input Frequency | | | |
|---|---|---|---|---|
| | 99.9 MHz | 399 MHz | 999 MHz | 1.999 GHz |
| SNR[8] (dBFS) | 54.7 | 54.4 | 53.9 | 52.8 |
| SINAD[8] (dBFS) | 54.4 | 53.8 | 53.3 | 52.4 |
| SFDR (dBc) | -65.2 | -61.1 | -60.3 | -63.2 |
| ENOB[9] (bits) | 8.7 | 8.6 | 8.5 | 8.4 |

Table 4. Single-Tone Spectral Performance, Dual Channel Mode, 1 V range, -01 Variant

| | Input Frequency | | | |
|---|---|---|---|---|
| | 99.9 MHz | 399 MHz | 999 MHz | 1.999 GHz |
| SNR[8] (dBFS) | 54.0 | 53.9 | 52.8 | 50.1 |

| | Input Frequency | | | |
|---|---|---|---|---|
| | 99.9 MHz | 399 MHz | 999 MHz | 1.999 GHz |
| SINAD[8] (dBFS) | 53.9 | 53.4 | 52.2 | 50.0 |
| SFDR (dBc) | -61.3 | -60.9 | -58.4 | -52.3 |
| ENOB[9] (bits) | 8.7 | 8.6 | 8.4 | 8.0 |

Table 5. Single-Tone Spectral Performance, Single Channel Mode, 1 V range, -01 Variant[10]

| | Input Frequency | | | |
|---|---|---|---|---|
| | 99.9 MHz | 399 MHz | 999 MHz | 1.999 GHz |
| SNR[8] (dBFS) | 52.0 | 52.0 | 51.7 | 50.9 |
| SINAD[8] (dBFS) | 51.9 | 51.8 | 51.4 | 50.7 |
| SFDR (dBc) | -65.1 | -61.7 | -62 | -64.4 |
| ENOB[9] (bits) | 8.3 | 8.3 | 8.2 | 8.1 |

Table 6. Single-Tone Spectral Performance, Dual Channel Mode, 200 mV range, -01 Variant

| | Input Frequency | | | |
|---|---|---|---|---|
| | 99.9 MHz | 399 MHz | 999 MHz | 1.999 GHz |
| SNR[8] (dBFS) | 51.0 | 51.0 | 50.4 | 48.9 |
| SINAD[8] (dBFS) | 51.0 | 50.8 | 50.2 | 48.9 |
| SFDR (dBc) | -57.8 | -58.8 | -58.4 | -53.3 |
| ENOB[9] (bits) | 8.2 | 8.1 | 8.0 | 7.8 |

Table 7. Single-Tone Spectral Performance, Single Channel Mode, 200 mV range, -01 Variant[10]

| Mode | $\frac{nV}{\sqrt{Hz}}$ | $\frac{dBm}{Hz}$ | $\frac{dBFS}{Hz}$ |
|---|---|---|---|
| Dual channel | 15.3 | -143.3 | -147.3 |
| Single channel | 10.2 | -146.8 | -150.8 |

Table 8. Noise Spectral Density, 1 V Range, -01 Variant[11]

| Mode | $\frac{nV}{\sqrt{Hz}}$ | $\frac{dBm}{Hz}$ | $\frac{dBFS}{Hz}$ |
|---|---|---|---|
| Dual channel | 4.3 | -154.3 | -144.3 |

| Mode | $\frac{nV}{\sqrt{Hz}}$ | $\frac{dBm}{Hz}$ | $\frac{dBFS}{Hz}$ |
|---|---|---|---|
| Single channel | 3.1 | -157.1 | -147.1 |

Table 9. Noise Spectral Density, 200 mV Range, -01 Variant[11]

**Note** Noise spectral density is verified using a 50 Ω terminator connected to AI0. Noise Spectral density may be degraded using channel AI1.

Figure 1. Single Tone Spectrum (Dual Channel Mode, 99MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured

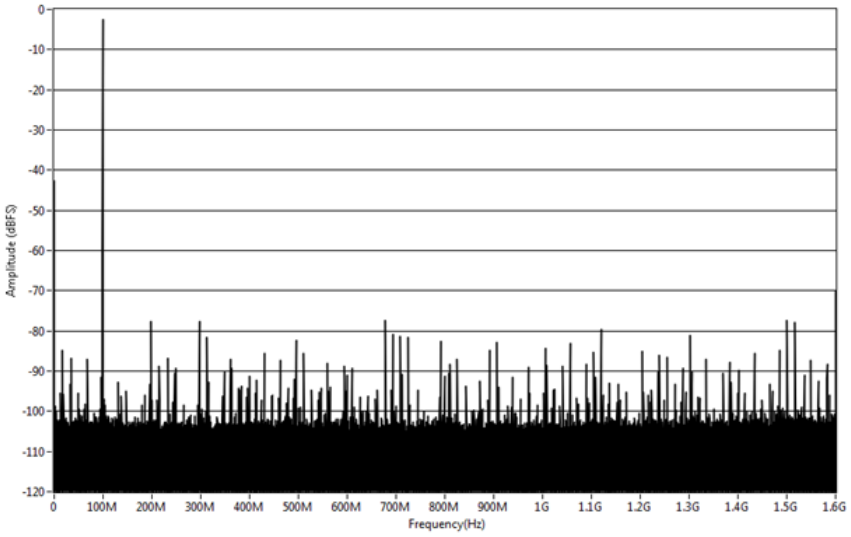


Figure 2. Single Tone Spectrum (Dual Channel Mode, 999 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured

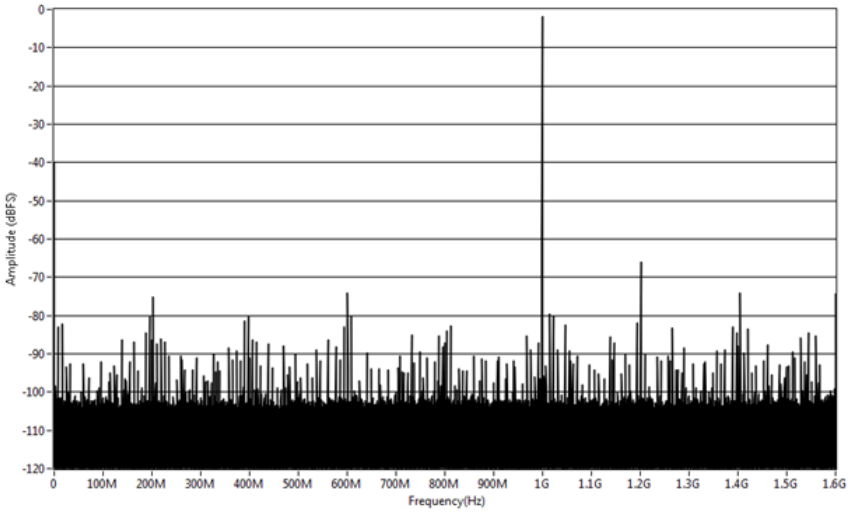



Figure 3. Single Tone Spectrum (Single Channel Mode, 99 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured

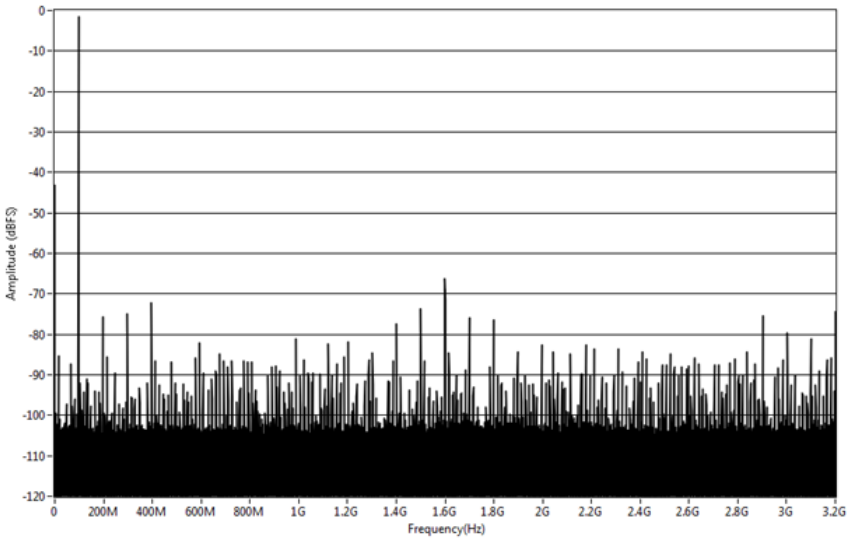
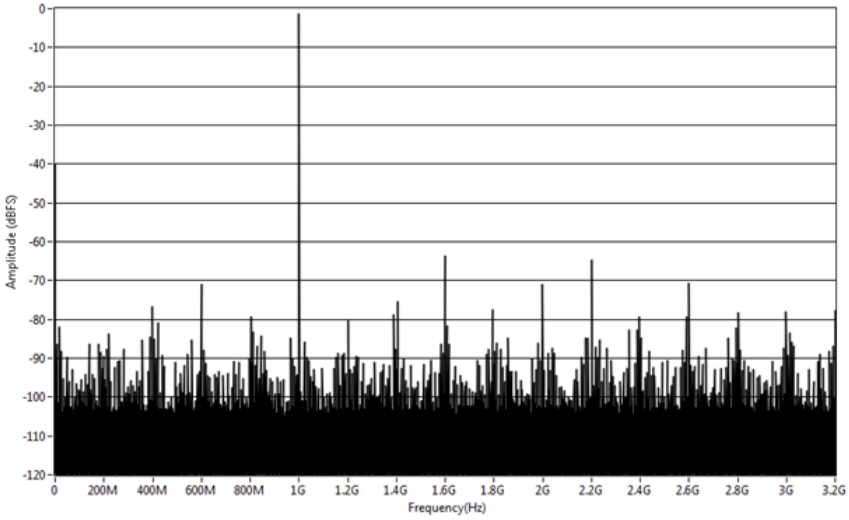


Figure 4. Single Tone Spectrum (Single Channel Mode, 999 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured




| Channel-to-channel crosstalk, measured | |
|---|---|
| 99.9 MHz | -94.1 dB |
| 399 MHz | -85.6 dB |
| 999 MHz | -82.5 dB |
| 1.59 GHz | -75.6 dB |
| 1.99 GHz | -72.2 dB |

Figure 5. Analog Input Frequency Response (1 V Range, -01 Variant), Measured

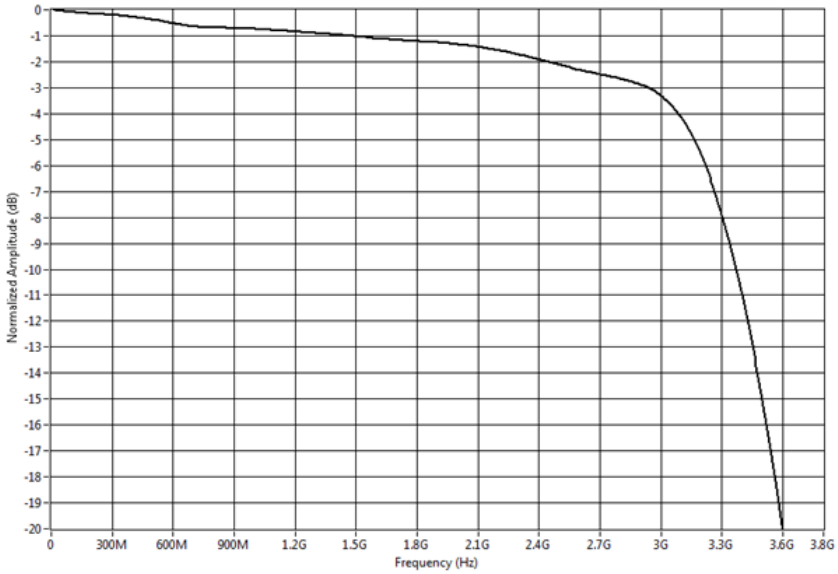



Figure 6. Analog Input Frequency Response (200 mV Range, -01 Variant), Measured

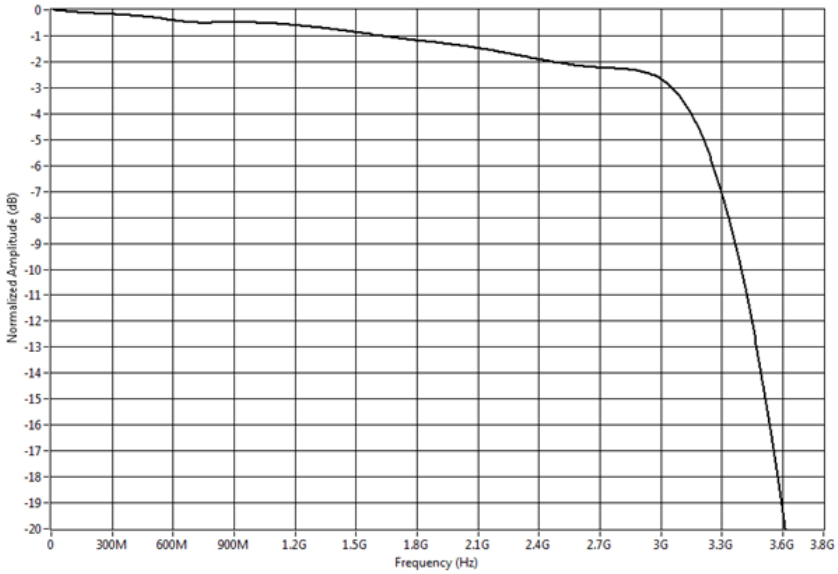


Figure 7. Analog Input Frequency Response (1 V Range, -02 Variant), Measured

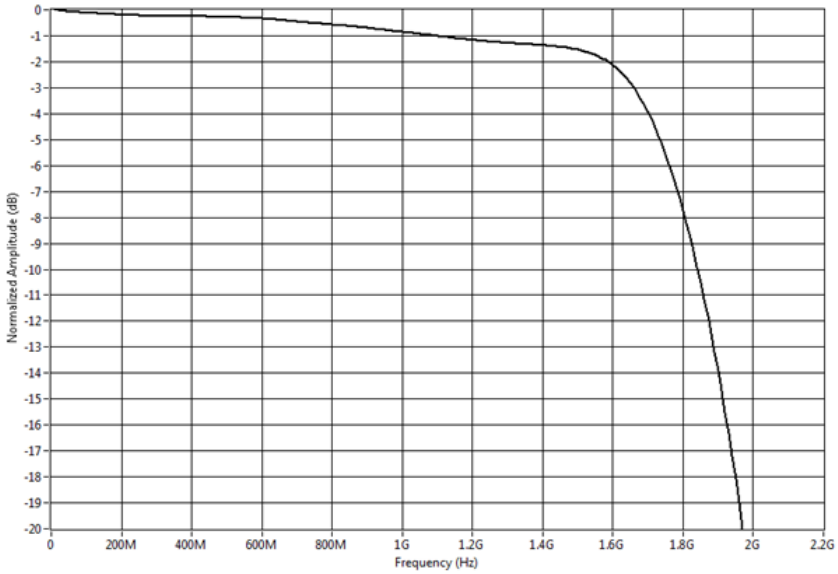



Figure 8. Analog Input Frequency Response (200 mV Range, -02 Variant), Measured

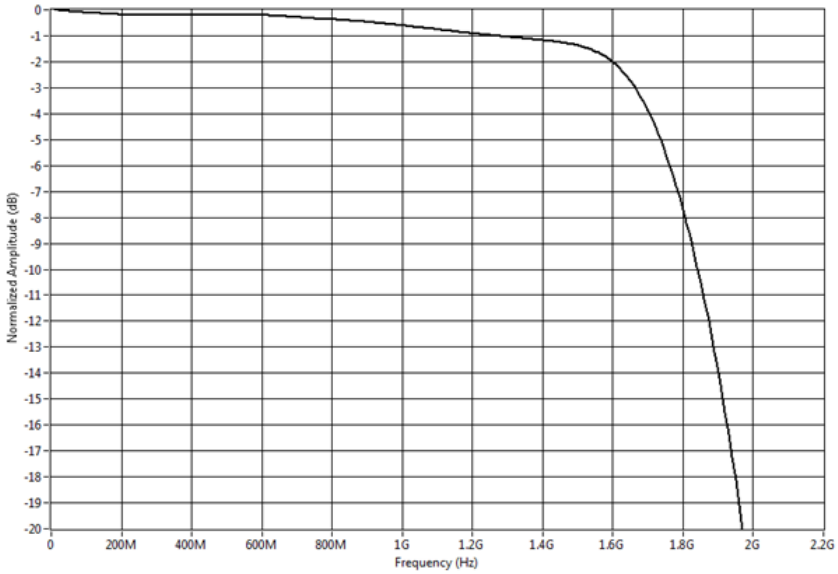


Figure 9. Input Return Loss (1 V Range), Measured

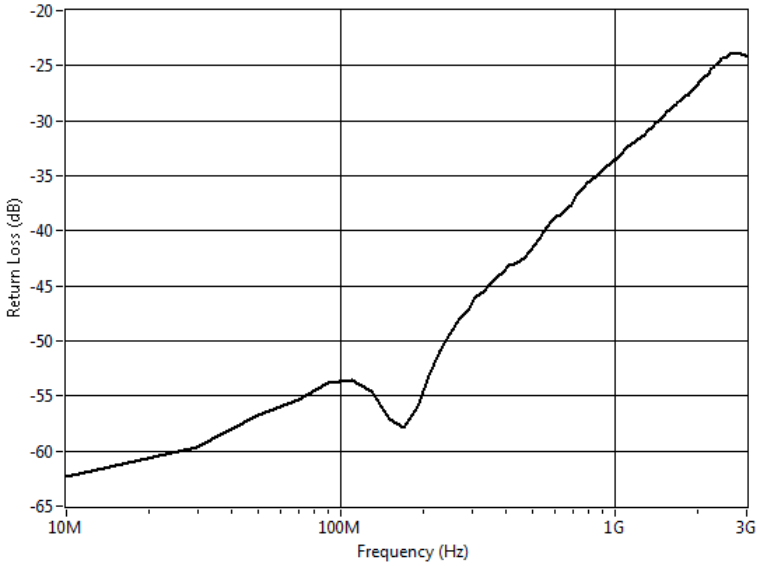
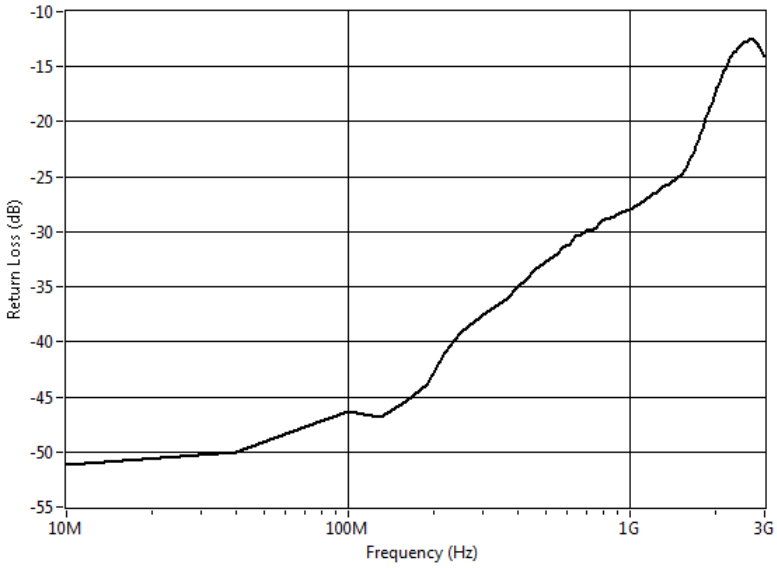



Figure 10. Input Return Loss (200 mV Range), Measured




## REF/CLK IN

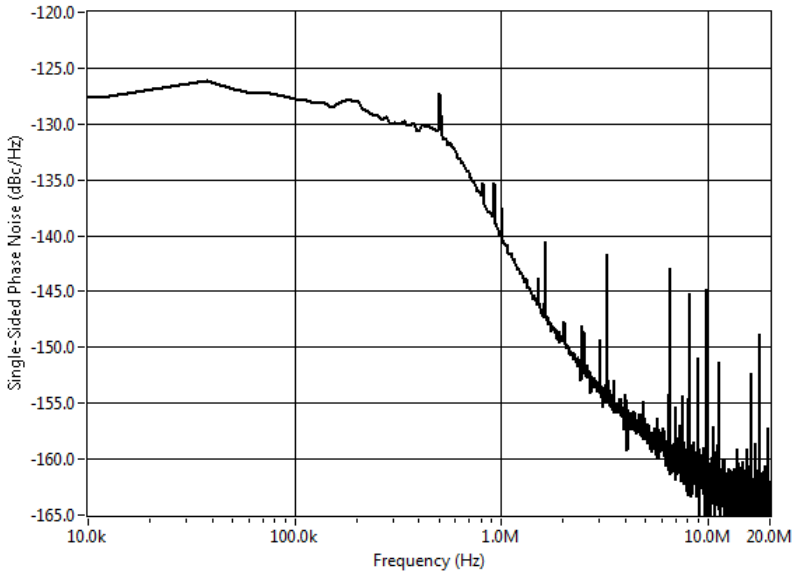
| | |
|---|---|
| Connector type | SMA |
| Input impedance | 50 Ω |

| | |
|---|---|
| Input coupling | AC |
| Input voltage range | 0.35 V pk-pk to 3.5 V pk-pk |
| Absolute maximum voltage | ±12 V DC, 5 V pk-pk AC |
| Duty cycle | 45% to 55% |
| Onboard reference timebase stability | ±0.5 ppm |
| Sample Clock jitter[12] | 85 fs RMS, measured |

| Clock Configuration | External Clock Frequency | Description |
|---|---|---|
| Internal Reference Clock[13] | - | The internal Sample Clock locks to an onboard voltage-controlled temperature compensated crystal oscillator (VCTCXO). |
| Internal Baseboard Reference Clock | 10 MHz | The internal Sample Clock locks to the 10 MHz Reference Clock, which is provided through the FPGA baseboard. |
| External Reference Clock (REF/CLK IN) | 10 MHz [14] | The internal Sample Clock locks to an external Reference Clock, which is provided through the REF/CLK IN front panel connector. |
| External Sample Clock (REF/CLK IN) | 3.2 GHz | An external Sample Clock can be provided through the REF/CLK IN front panel connector. |

Table 10. Clock Configuration Options

Figure 11. Phase Noise with 800 MHz Input Tone, Measured




## Analog IN Trigger

| | |
|---|---|
| Connector type | SMA |
| Input impedance | 50 Ω, nominal |
| Input coupling | DC |
| Input voltage range | ±5 V |
| Comparator threshold resolution | 12 bits |
| Minimum pulse width | 5 ns |
| Absolute maximum voltage | ±6 V |

## Digital OUT Trigger

| | |
|---|---|
| Connector type | SMA |
| Input impedance | 50 Ω, nominal |
| Input coupling | DC |
| Logic type | 3.3 V CMOS |
| Maximum current drive | 24 mA |
| Update rate resolution | 5 ns |
| Jitter | 3.2 ps rms, measured |

## Bus Interface

| | |
|---|---|
| Card edge form factor | PCI Express Gen-3 x8 |
| Slot compatibility | x8, and x16 PCI Express slots |

## Maximum Power Requirements

**Note** Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

| | |
|---|---|
| +3.3 V | 4.5 A |
| +12 V | 5 A |

| | |
|---|---|
| Maximum total power | 75 W |

## Physical

| | |
|---|---|
| Dimensions (including I/O bracket, not including connectors) | 12.6 cm × 26.3 cm × 4 cm (5.0 in. × 10.4 in. × 1.6 in.) |
| Weight | 990 g (35 oz) |
| PCI Express mechanical form factor | Standard height, three-quarter length, double slot |
| Integrated air mover (fan) | Yes |
| Maximum rear panel exhaust airflow | 84 $m^3$/h (50 CFM) (without any chassis impedance) |

## Environment

| | |
|---|---|
| Maximum altitude | 2,000 m (800 mbar) (at 25 °C ambient temperature) |
| Pollution Degree | 2 |

Indoor use only.

# Operating Environment

| | |
|---|---|
| Operating temperature, local[15] | 0 °C to 45 °C |
| Operating humidity | 10% to 90% RH, noncondensing |

## Storage Environment

| | |
|---|---|
| Ambient temperature range | -20 °C to 70 °C |
| Relative humidity range | 5% to 95% RH, noncondensing |

[1] Multi-gigabit transceiver (MGT) signals are available on devices with KU060 FPGAs only.

[2] Voltage levels are guaranteed by design through the digital buffer specifications.

[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

[4] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

[5] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

[6] In single channel mode the ADC cores are interleaved for an aggregate sample rate of 6.4 GS/s.

[7] Normalized to 10 MHz.

[8] Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

[9] Calculated from SINAD and corrected to full scale.

[10] Measured using channel AI0. Spectral performance may be degraded using channel AI1.

[11] Excludes fixed interleaving spurs.

[12] Integrated from 3.2 kHz to 20 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

[13] Default clock configuration.

[14] The external Reference Clock must be accurate to ±25 ppm.

[15] For PCI Express adapter cards with integrated air movers, NI defines the local operational ambient environment to be at the fan inlet. For cards without integrated air movers, NI defines the local operational ambient environment to be 25 mm (1 in.) upstream of the leading edge of the card.