



PMX700EN

60 V, N-channel Trench MOSFET

16 June 2022

Preliminary data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0603-3 (SOT8013) Surface-Mounted Device (SMD) using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Leadless ultra small package 0.63mm x 0.33 mm x 0.25 mm
- Trench MOSFET technology
- Low profile (0.25 mm)

3. Applications

- Battery switch
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

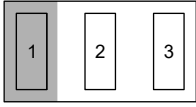
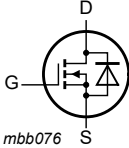
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	0.3	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 0.4\text{ A}; T_j = 25\text{ °C}$	-	680	800	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN0603-3 (SOT8013)</p>	 <p>mbb076</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMX700EN	DFN0603-3	DFN0603-3; plastic, ultra small and leadless full encapsulated package; 3 terminals; 0.225 mm pitch; 0.63 mm x 0.33 mm x 0.25 mm body	SOT8013

7. Marking

Table 4. Marking codes

Type number	Marking code
PMX700EN	D

8. Limiting values

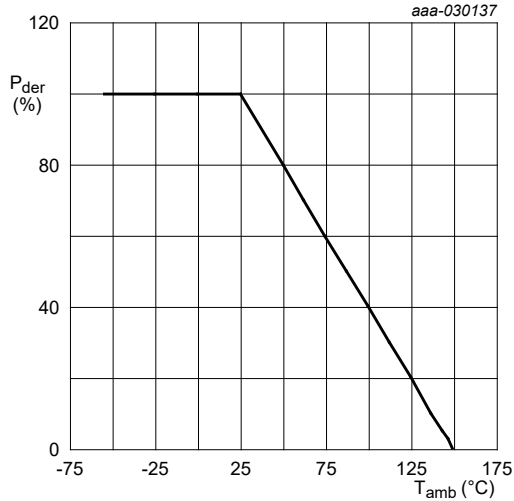
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	0.3	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	0.2	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	1.3	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	300	mW
			[1]	-	500	mW
		$T_{sp} = 25\text{ °C}$		-	4.7	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	0.3	A

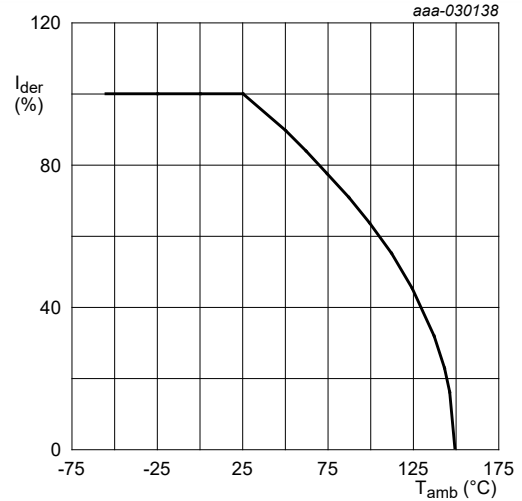
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

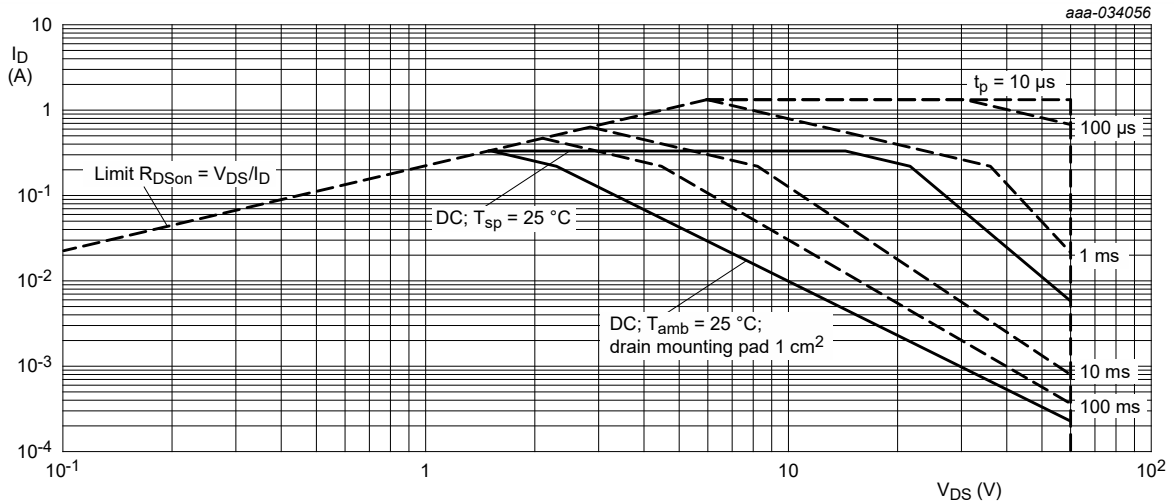


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	360	415	K/W
			[2]	-	215	250	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	23	26.5	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

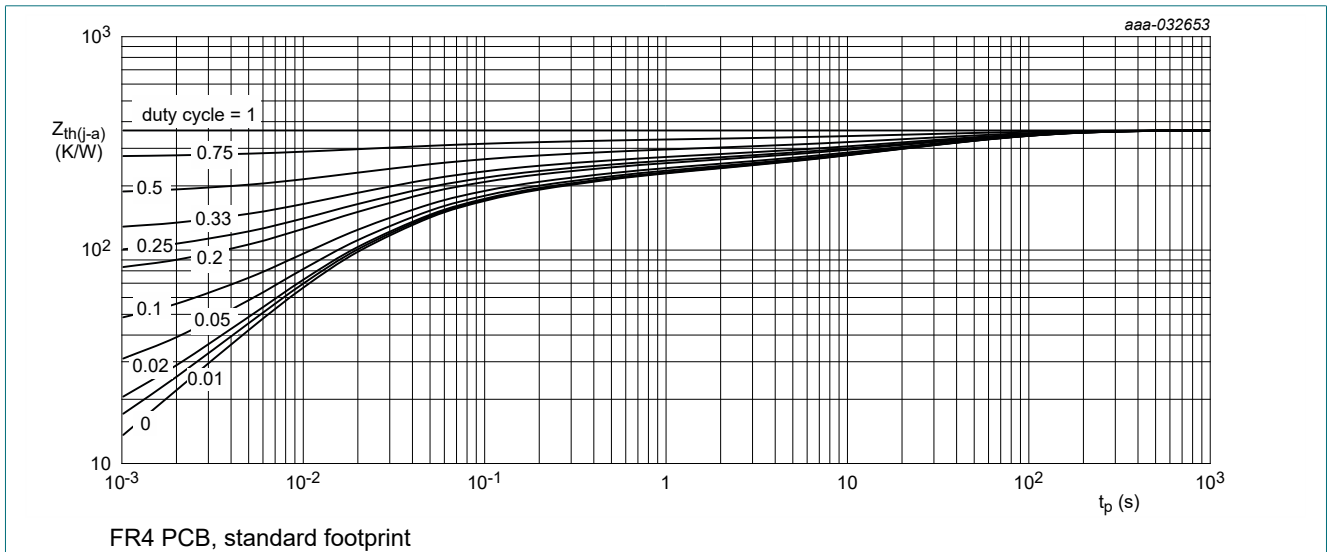


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

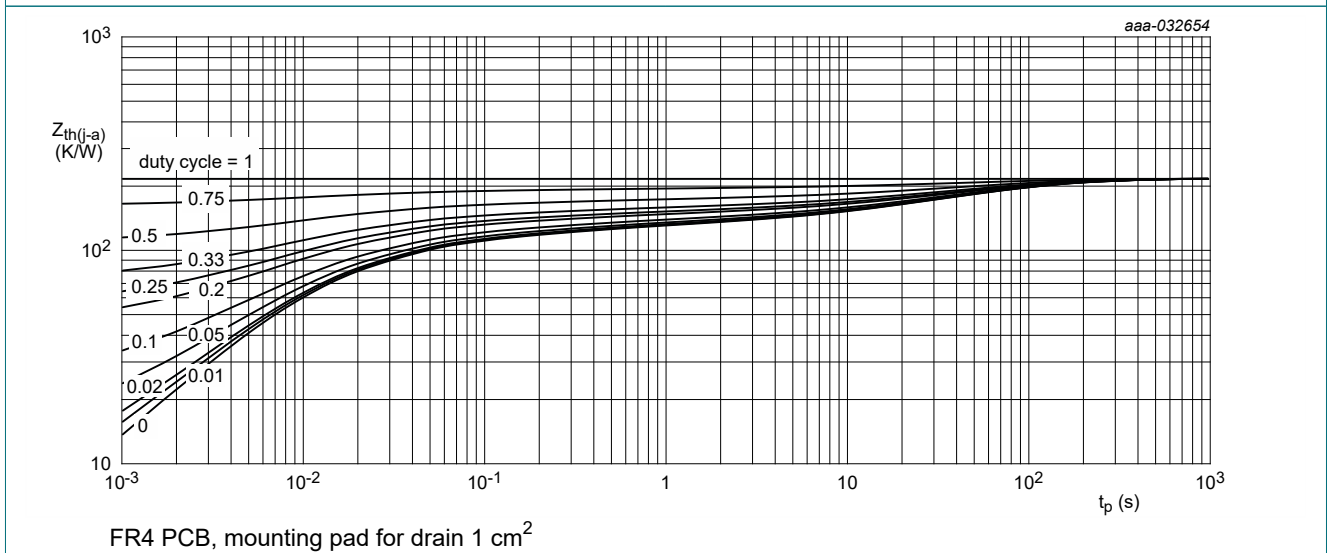


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	1	1.8	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = 20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 0.4 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	680	800	m Ω
		$V_{GS} = 10 \text{ V}$; $I_D = 0.4 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	1300	1600	m Ω
		$V_{GS} = 4.5 \text{ V}$; $I_D = 0.3 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	760	1000	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}$; $I_D = 0.4 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.1	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	40	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 \text{ V}$; $I_D = 0.4 \text{ A}$; $V_{GS} = 10 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.7	1.1	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	39	-	pF
C_{oss}	output capacitance		-	3	-	pF
C_{rss}	reverse transfer capacitance		-	2	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 \text{ V}$; $I_D = 0.4 \text{ A}$; $V_{GS} = 10 \text{ V}$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	1	-
t_r	rise time	-		1	-	ns
$t_{d(off)}$	turn-off delay time	-		7	-	ns
t_f	fall time	-		4	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 0.33 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V

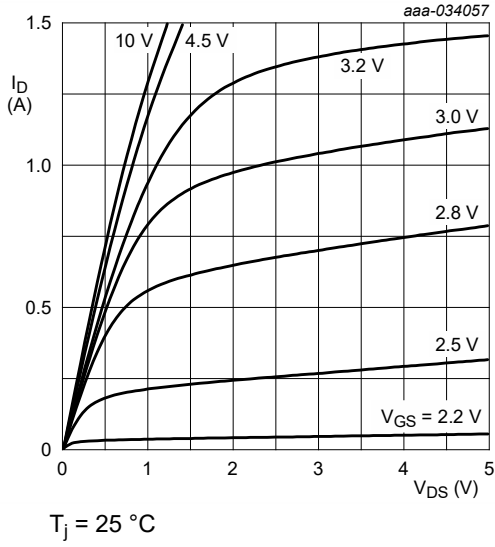


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

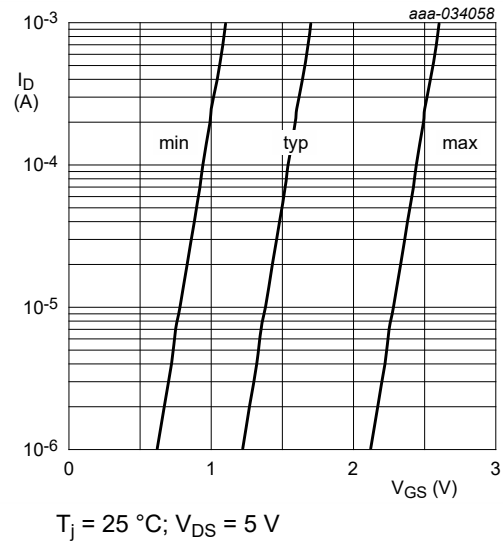


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

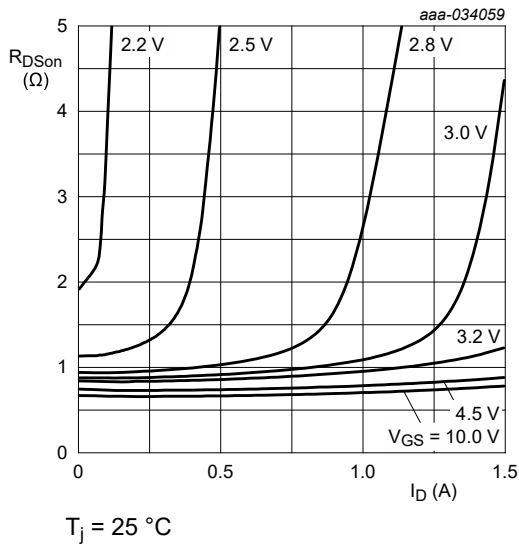


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

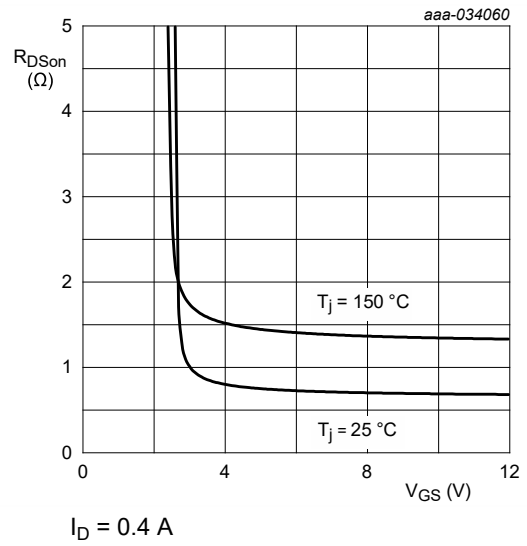


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

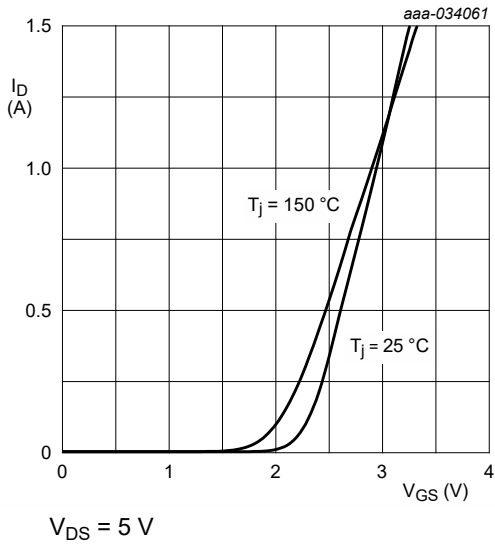


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

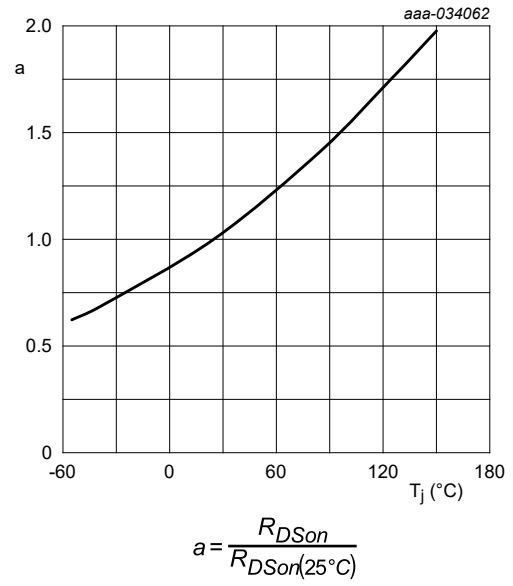


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

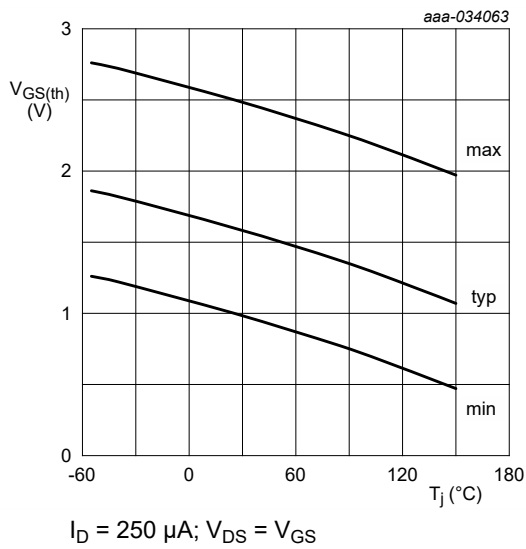


Fig. 12. Gate-source threshold voltage as a function of junction temperature

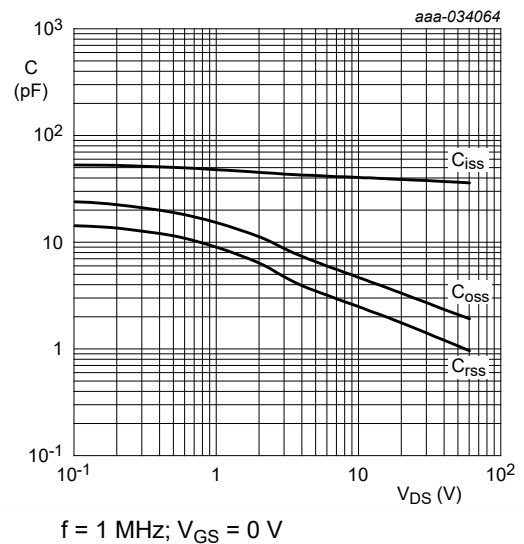
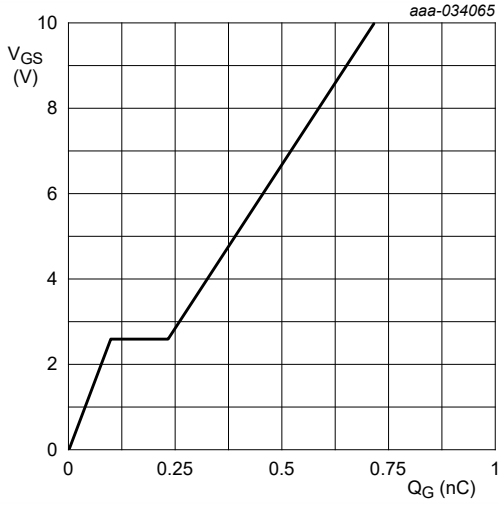


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 30 \text{ V}; I_D = 0.4 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

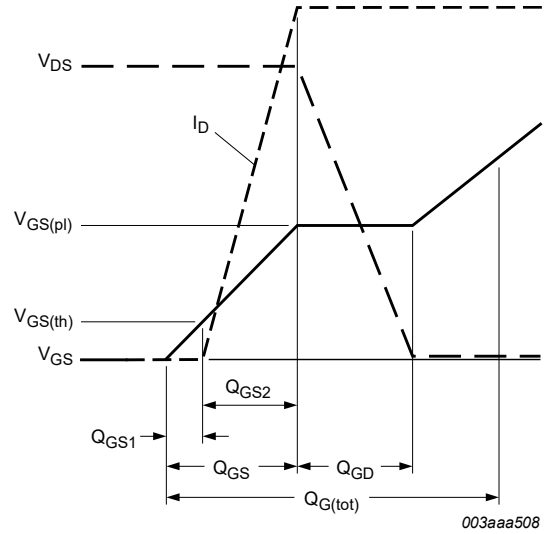
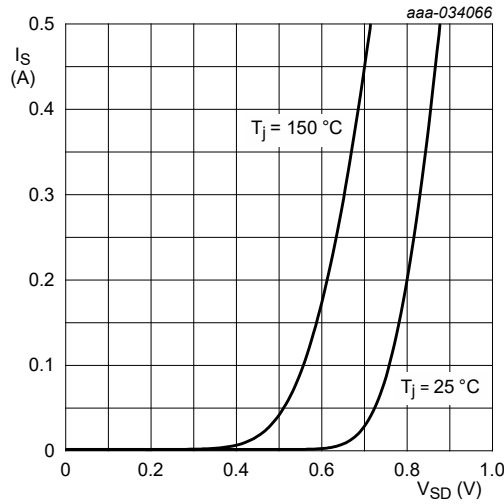


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

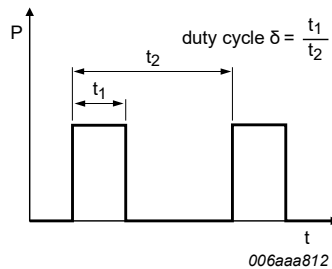
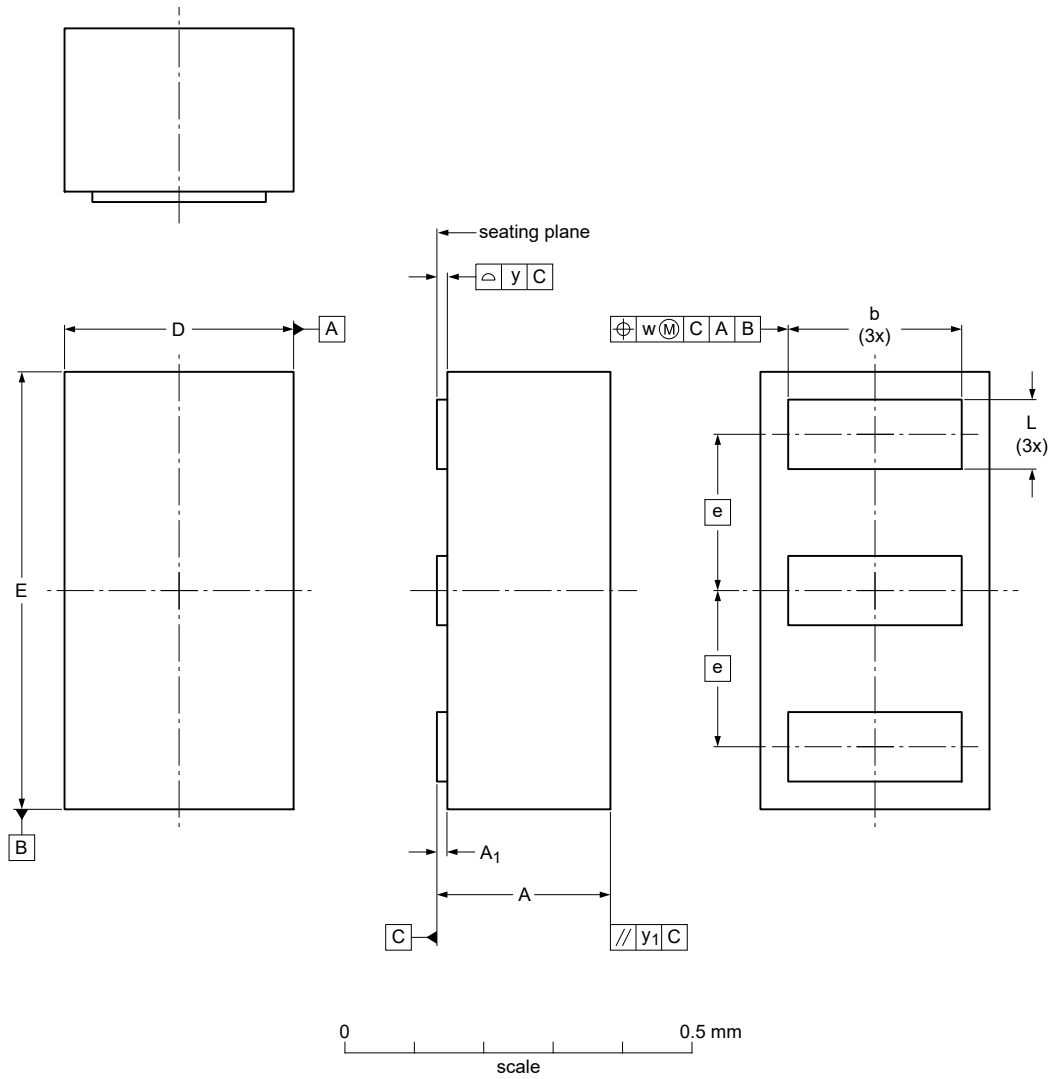


Fig. 17. Duty cycle definition

12. Package outline

DFN0603-3; plastic, ultra small and leadless full encapsulated package;
3 terminals; 0.225 mm pitch; 0.63 mm x 0.33 mm x 0.25 mm body

SOT8013



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	b	D	E	e	L	w	y	y ₁
mm	max 0.275	0.03	0.27	0.350	0.650		0.12			
	nom 0.225		0.23	0.305	0.605	0.225		0.04	0.03	0.05
	min						0.08			

Note

1. The marking bar indicates Pin 1. For electrical symmetrical devices the marking bar is omitted.

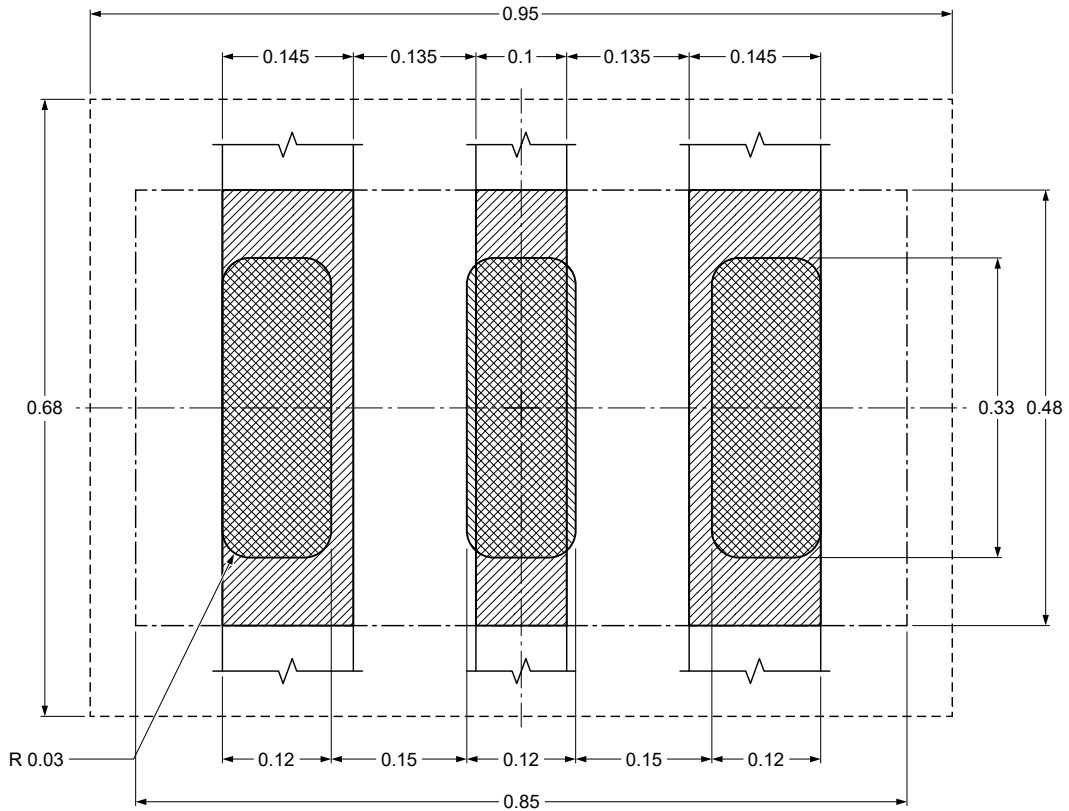
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Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8013		---				19-08-06 19-08-29





Fig. 18. Package outline DFN0603-3 (SOT8013)

13. Soldering

Footprint information for reflow soldering of ultra small and leadless encapsulated package; 3 terminals SOT8013



recommended stencil thickness: 0.08 mm

-  occupied area
 -  solder land (Cu extends under solder resist)
 -  solder resist
 -  stencil opening
- Dimensions in mm

Issue date ~~19-10-29~~
20-02-26

sot8013_fr

Fig. 19. Reflow soldering footprint for DFN0603-3 (SOT8013)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMX700EN v.1	20220616	Preliminary data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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