UM11666

SC18IS606-EVB evaluation board

Rev. 1.0 — 28 September 2021 **User manual**

Document information

Information	Content
Keywords	SC18IS606, I^2C to SPI, SC18IS602, SPI Controller, SPI master, I^2C bridge, SPI bridge
Abstract	SC18IS606 is designed to serve as an interface between a standard I^2C-bus of a microcontroller and an SPI bus. This allows the microcontroller to communicate directly with SPI devices through its I^2C-bus. SC18IS606 operates as an I^2C target and an SPI master.

Revision history

Rev	Date	Description
v.1.0	20210928	Initial version

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1 Introduction

SC18IS606 is designed to operate as an I^2C target and an SPI master. SC18IS606 controls all the SPI bus specific sequences, protocol, and timing. SC18IS606 has its own internal oscillator, and it supports three SPI chip select outputs that may be configured as GPIO when not used as SPI chip selects.

This document is intended to help the users to quickly setup, configure and operate the SC18IS606-EVB evaluation board in the users' hardware platform.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for SC18IS606-EVB evaluation board is at http://www.nxp.com/SC18IS606-EVB. The information page provides overview information, documentation, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the SC18IS606-EVB evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the SC18IS606-EVB evaluation board requires the kit contents.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- Quick Start Guide

4 Getting to know the hardware

The SC18IS606-EVB evaluation board is designed to be connected to an external I^2C controller via a 6-pin male (JP2) header. The SC18IS606-EVB evaluation board has an on-board SPI slave serial EEPROM, which can be directly accessed by the external I^2C controller via SC18IS606. The external I^2C controller can write, read, and program the serial EEPROM without requiring an SPI slave to be connected to the board.

The 3V3 power for the SC18IS606-EVB evaluation board should be supplied via this I^2C interface header as well.

The SC18IS606-EVB evaluation board also has an SPI interface header (JP1) to allow other SPI slave devices to be connected to the evaluation board. These SPI slave devices can be accessed directly by the I^2C controller via the SC18IS606 I^2C to SPI bridge.

4.1 Headers and jumpers

Please refer to Figure 1 to find the location of connectors and jumpers on the SC18IS606-EVB evaluation board.

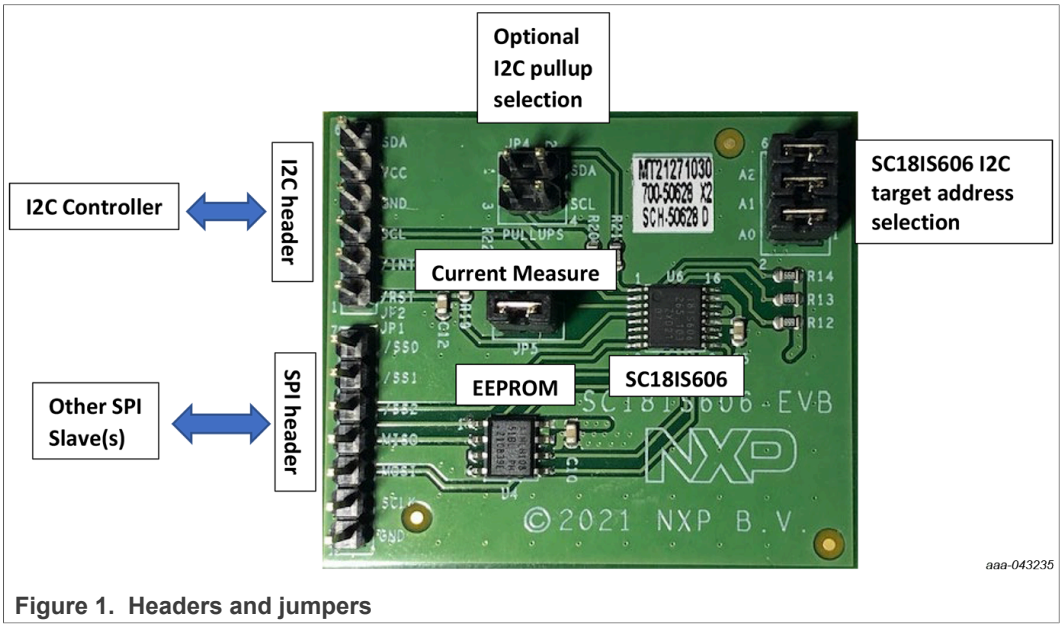

Figure 1. Headers and jumpers

4.2 Jumper settings

Table 1. Jumper settings

Header	Jumper on	Comment
JP3	1-2, 3-4, 5-6	I^2C target address 0x50
JP4	1-2, 3-4	Pull out jumpers if pull ups on I^2C controller
JP5	1-2	Pull out and insert current meter if SC18IS606 current is to be measured

Table 2. JP1 - SPI header

JP1 – SPI header	Function
1	Ground
2	SPICLK
3	MOSI
4	MISO
5	-CS2
6	-CS1
7	-CS0

Table 3. JP2 - I²C

JP2 – I²C Header	Function
1	-Reset
2	-INT (interrupt)
3	SCL
4	Ground
5	VCC
6	SDA

Table 4. JP3 – SC18IS606 I²C target address

JP3 – SC18IS606 I²C target address	1 -2	3 -4	5 -6
0x50	ON	ON	ON
0x51	OFF	ON	ON
0x52	ON	OFF	ON
0x53	OFF	OFF	ON
0x54	ON	ON	OFF
0x55	OFF	ON	OFF
0x56	ON	OFF	OFF
0x57	OFF	OFF	OFF

4.3 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the SC18IS606-EVB evaluation board are available at http://www.nxp.com/SC18IS606-EVB.

4.4 Sample control sequences from I²C controller

4.4.1 GPIO as input

```
Write 0x50 0xF6 0x07 // program chip select pins as GPIO
Write 0x50 0xF7 0xAA // configure GPIOs as inputs
Write 0x50 0xF5      // read inputs into buffer
Read 0x51            // read input pins state from buffer
```

4.4.2 GPIO as output

```
Write 0x50 0xF6 0x01 // program SS0 as GPIO
Write 0x50 0xF7 0x55 // GPIO pins as push-pull
Write 0x50 0xF4 0x00 // Set SS0 to '0'
Write 0x50 0xF4 0x01 // Set SS0 to '1'
```

4.4.3 SPI mode and clock configuration

```
Write 0x50 0xF0 0x02 // Set SPI mode 0, MSB first, SPI clock to 115KHz
Write 0x50 0xF0 0x05 // Set SPI mode 1, MSB first, SPI clock to 461KHz
```

4.4.4 Device ID read

```
Write 0x50 0xFE // Read device ID into buffer
Read 0x51 0x10  // read 16 bytes from buffer, return data 0x53
                // 0x43 0x31 0x38 0x49 0x53 ….. 0x30 0x2E 0x31 0x00
```

4.4.5 On-board EEPROM write and read

```
Write 0x50 0xF0 0x0C // SPI mode 3, SPI clock to 1.875MHz
Write 0xF1           // clear interrupt
Write 0x02 0x06      // send command 0x06 (write enable latch) to EEPROM with SS1 as -CS
Write 0x02 0x02 0x00 0x00 0x30 0x01 0x03 0x05 0x07 0x09 0x0B
                     // write data (0x01 0x03 … 0x0b) to EEPROM
Write 0x02 0x03 0x00 0x00 0x30 0x00 0x00 0x00 0x00 0x00 0x00
                     // Read data back from EEPROM into buffer
Read 0x51 0x0A       // Read 10 bytes from buffer. The first four bytes should be discarded
```

5 Errata list

Table 5. Errata list

Date	Errata Description	Demo Impact	Solution
-	None	None	None

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