LogicTile Express™ 20MG

For the Versatile Express™ Family

The Versatile Express family development boards provide an excellent environment for prototyping the next generation of system-on-chip designs. Through a range of plug-in options, hardware and software applications can be developed and debugged.
The LogicTile Express (LTE) 20MG is a development board especially designed for evaluation and prototyping of large user peripherals. An ideal companion FPGA board to work with a CoreTile Express product.
It offers:

- ~20 Million ASIC gates for user prototyping
- FPGA expansion by stacking a second LTE 20MG
- IO expansion via the top connectors
- Early device driver & software development

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The FPGA used is the largest Xilinx™ Virtex™ 7 device (XC7V2000T-1FLG1925CES9937). The T part offers gigabit transceivers (MGTs) in addition to the internal logic for prototyping.

A DDR3 SODIMM enables local dynamic memory, supporting up to 8GBs of 64bit DRAM, 4GB SODIMM supplied.

Features

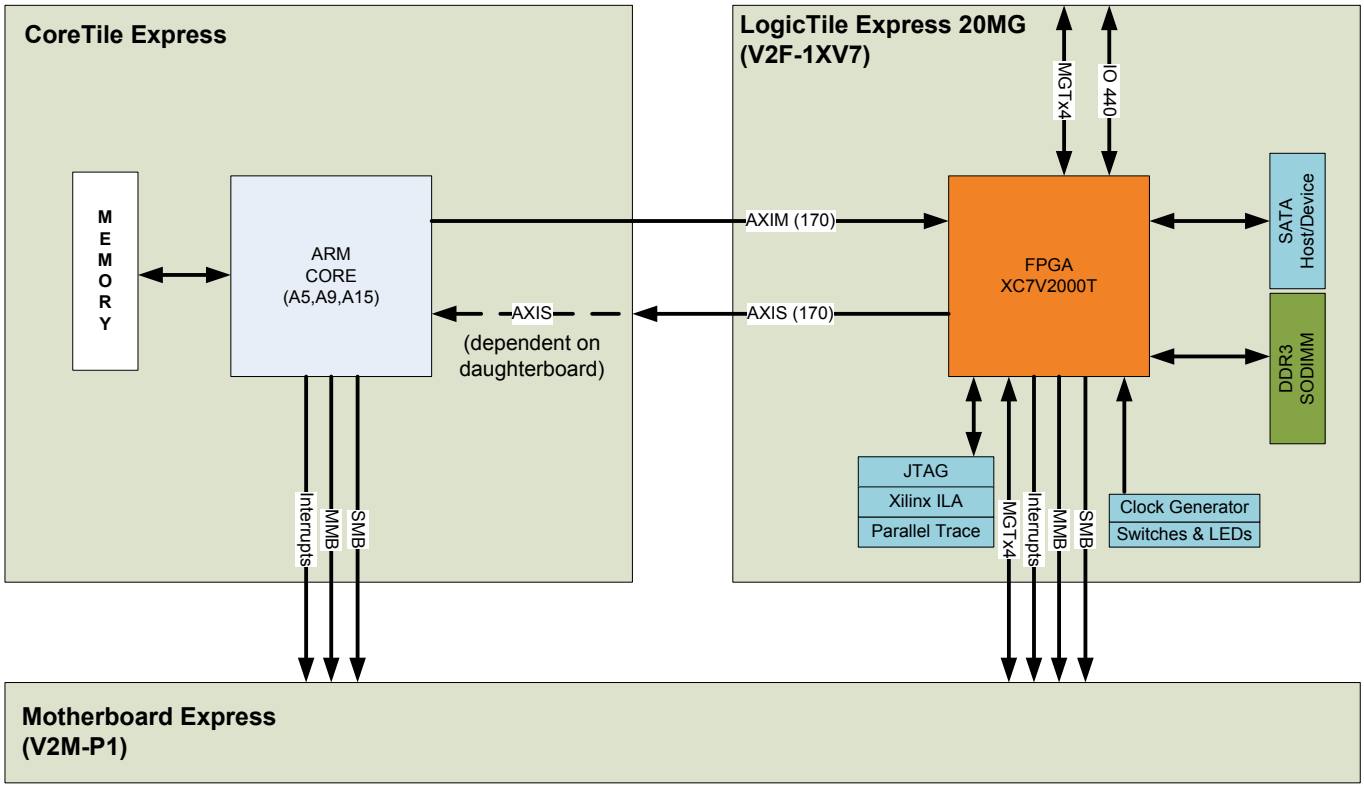
- FPGA (XC7V2000T)
  - 20 Million ASIC gates equivalent
  - PCIe 4lane endpoint support*
  - SATA Host and Device*
- Expansion
  - External AXI Master port
  - External AXI Slave port
  - 24bit RGB video out to motherboard
  - I^2S and SPDIF out to motherboard
  - Static memory bus to motherboard
  - DDR3 SODIMM (8GB max supported)
  - Interrupts to/from motherboard
  - Local PLL clock, 6 outputs to FPGA
- Debug
  - ARM JTAG
  - ARM 16bit parallel trace
  - Xilinx ILA for ChipScope/Identify
- User expansion upwards
  - 440 signals from XC7V2000T
  - 12 MGT channels from XC7V2000T
    - 4 up, 4 down, 4 to SATA connectors
- Simplified configuration
  - Fast programming < 1minute
  - Fast re-configuration < 10seconds

Deliverables

- Daughterboard
- ISE™ example design files
- Versatile Express support DVD
- Example AXI design
  - NIC301 example matrix
  - AXI mux/demux logic
- SelfTest Software
  - To prove AXI design
  - Allows user to modify for their design

*see Xilinx Virtex7 datasheet for details

LogicTile Express 20MG Architecture



The upper connectors allow the user to develop their own breakout board for connection to Si e.g. modems or to connectors to other systems or interfaces. It is possible to add an additional LTE 20MG on top for additional FPGA prototyping space.

A collection of different debug interfaces allows the use of ARM processor debug testing and proving of CoreSight. The Xilinx ILA connector allows the user to debug the FPGA design in real-time using ChipScope (part of the Xilinx ISE tool chain).

Additional support for PCIe and SATA is implemented using the Xilinx gigabit transceivers (MGTs) integrated in the FPGA using Xilinx or other 3rd party IP blocks. The PCIe interface uses the integrated Phy and PIPE interface and can utilise the built-in EndPoint. Four lanes of MGT also go to the upper connectors for additional expansion/prototyping support.

The support for multiplexed AXI interfaces on the FPGA allows prototyping of AXI components to be connected to an ARM processor (via CoreTile Express daughterboard) for functional testing at speed and device deriver/software development.

PART NUMBER: V2F-1XV7-0313A