MP2651

I²C-Controlled, 1-Cell to 4-Cell Buck-Boost Charger with Reverse Source Mode

DESCRIPTION

The MP2651 is a buck-boost charger IC designed for battery packs with 1 cell to 4 cells in series. The device can accept a wide 4V to 22V input voltage (V_{IN}) range to charge the battery. The buck-boost topology allows the battery voltage to be above or below V_{IN}.

When the input is present, the MP2651 operates in charge mode. It measures the battery voltage and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Other features include charge termination and auto-recharge.

The MP2651 also integrates the input current (I_{IN}) limit and V_{IN} limit to avoid overloading the input power source. This is compliant with the USB and PD specifications.

The MP2651 can also supply a wide voltage range (3V to 21V) at the input when source mode is enabled. The device also has an output current (I_{OUT}) limit with high resolution in source mode.

The I²C/SMBus interface can configure the charge and discharge parameters, including the I_{IN} limit, V_{IN} limit, charge current, battery-full regulation voltage, output voltage (V_{OUT}), and I_{OUT} in source mode. The MP2651 can also use the registers to provide information on statuses and faults.

To guarantee safe operation, the device limits the die temperature to a configurable threshold. Other safety features include input over-voltage protection (OVP), battery OVP, CFLR OVP, thermal shutdown, and a configurable timer to prevent prolonged charging of a dead battery.

The MP2651 is available in a TQFN-30 (4mmx5mm) package.

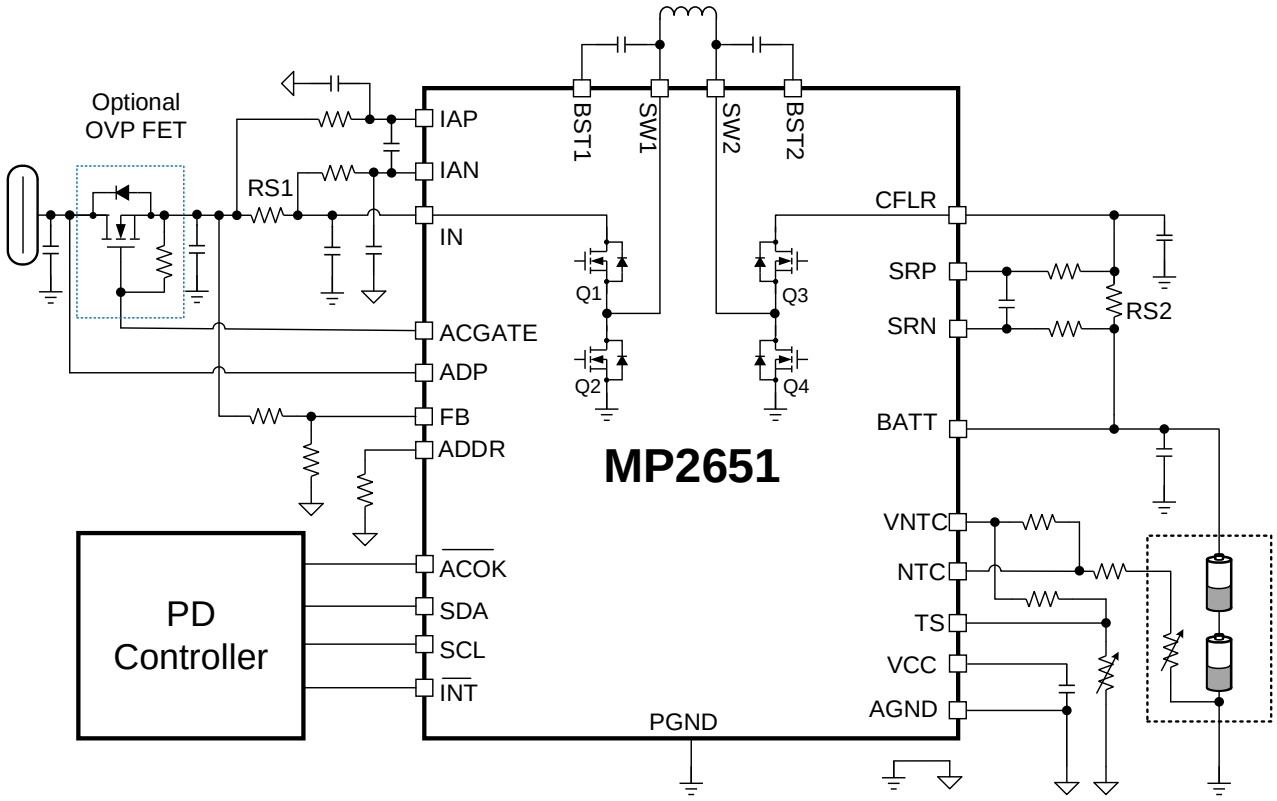
FEATURES

- Buck-Boost Charger for 1-Cell to 4-Cell Series Battery Packs
- 4V to 22V Operation Input Voltage (V_{IN})
- Up to 26V Sustainable Voltage, or 28V with External MOSFET
- Smooth Transitions Between Buck and Buck-Boost Modes
- Configurable Maximum Input Current (I_{IN}) Limit and Minimum V_{IN} Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 4.67V/Cell with 0.5% Accuracy
- Output Compatible with USB PD 3.0 Source Mode
- Configurable 3V to 21V Output Voltage (V_{OUT}) with 20mV/Step
- Up to 6A Output Current with 50mA/Step
- 500kHz to 1.2MHz Configurable f_{SW}
- I²C or SMBus Host Control Interface to Support Flexible Parameter Setting
- Input Power Source Status Indicator
- Integrated 10-Bit ADC for Monitoring in Both Charge Mode and Source Mode
- Analog Output Pin Monitors Charge Current
- Input and Battery OVP
- Output SCP in Source Mode
- Battery Missing Detection
- NTC Pin Floating Detection
- Integrated N-Channel MOSFET Driver for Input Power Pass Through or OVP
- Configurable JEITA for Battery Temperature Protection
- Thermal Regulation and Thermal Shutdown
- Available in a TQFN-30 (4mmx5mm) Package

APPLICATIONS

- Power Banks
- Wireless Speakers
- Drones
- Mobile Printers
- USB PD Multi-Cell Applications

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2651GVT-xxxx**	TQFN-30 (4mmx5mm)	*See Below*	1
EVKT-MP2651	Evaluation kit	*See Below*	-

* For Tape & Reel, add suffix -Z (e.g. MP2651GVT-xxxx-Z).

** "xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I^2C register map. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

MPSYWW
MP2651
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2651: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2651

EVKT-MP2651 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2651-VT-00A	MP2651 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

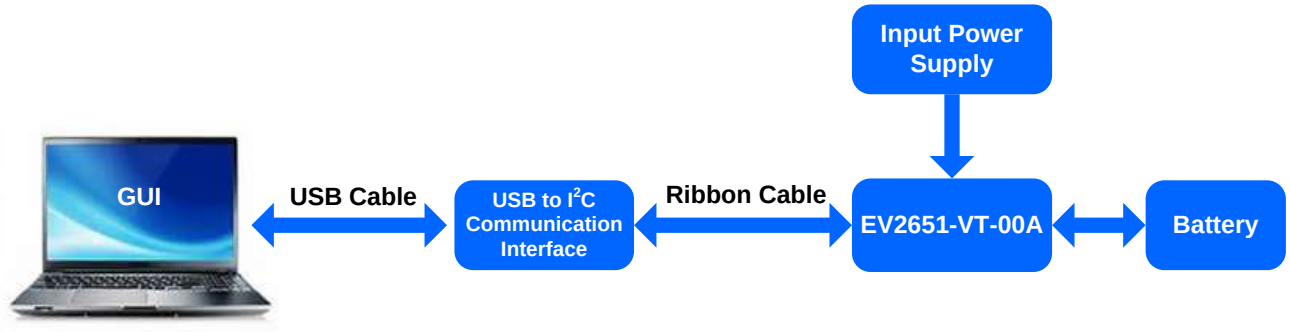
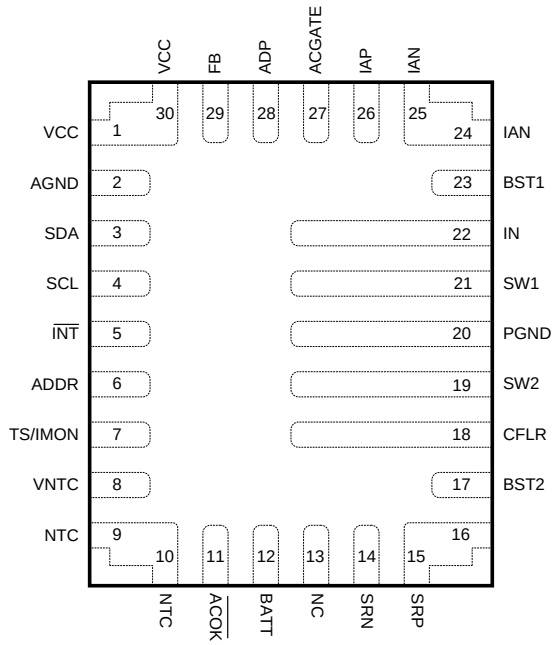


Figure 1: EVKT-MP2651 Evaluation Kit Set-Up

PACKAGE REFERENCE

TOP VIEW



TQFN-30 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 30	VCC	**VCC LDO output.** Connect a 4.7µF ceramic capacitor from the VCC pin to AGND. VCC can provide a 3.6V output for the internal circuit and open-drain pin pull-up.
2	AGND	**Analog ground.** All parameter settings refer to this ground.
3	SDA	**I²C/SMBus data.** Connect SDA to the logic rail through a 10kΩ resistor.
4	SCL	**I²C/SMBus clock.** Connect SCL to the logic rail through a 10kΩ resistor.
5	$\overline{\text{INT}}$	**Interrupt request output.** This is an open-drain structure that must be pulled up to VCC with an external 10kΩ resistor.
6	ADDR	**Address setting.** Connect a resistor to AGND to set the IC address.
7	TS/IMON	**Temperature sense/current monitor.** This pin can be set to be a temperature-sense pin (TS) or a current monitor pin (IMON). If this pin is configured to be the IMON pin, it monitors the charge current.
8	VNTC	**Battery temperature-sense bias.** This pin is used for the voltage bias of the NTC comparator's resistor divider.
9, 10	NTC	**Negative temperature coefficient (NTC) thermistor pin.** The NTC pin is the battery temperature sense's input.
11	$\overline{\text{ACOK}}$	**Input power good (PG) indication.** This pin has an open-drain output that indicates if the adapter is present. This pin must be externally pulled up to a voltage source.
12	BATT	**Battery pin.** BATT is the battery's positive terminal. Connect a 22µF ceramic capacitor from BATT to PGND, placed as close as possible to the IC. Connect the battery as close as possible to this pin to reduce IR drop.
13	NC	**No connection.** Float this pin.
14	SRN	**Battery current-sense resistor negative terminal.**
15, 16	SRP	**Battery current-sense resistor positive terminal.**
17	BST2	**Bootstrap.** Connect a 100nF bootstrap capacitor between the BST2 and SW2 pins to form a floating supply across the power MOSFET driver to drive the power MOSFET's gate above the supply voltage.
18	CFLR	**DC/DC power stage output.** Connect two 22µF ceramic filter capacitors from CFLR to PGND, placed as close as possible to the IC.
19	SW2	**Switching node.** SW2 is the middle point of the boost phase's half-bridge.
20	PGND	**Power ground.**
21	SW1	**Switching node.** SW1 is the middle point of the buck phase's half-bridge.
22	IN	**Input pin.** IN is the power input of the IC.
23	BST1	**Bootstrap.** Connect a 100nF bootstrap capacitor between BST1 and SW1 pin to form a floating supply across the power MOSFET driver to drive the power MOSFET's gate above the supply voltage.
24, 25	IAN	**Input current-sense negative terminal.**
26	IAP	**Input current-sense positive terminal.**
27	ACGATE	**Input N-channel MOSFET gate driver.** ACGATE drives the external pass-through N-channel MOSFET. It is recommended to connect a 1MΩ resistor between ACGATE and the N-channel MOSFET's source port.
28	ADP	**Adapter voltage sense.** If ADP over-voltage lockout (OVLO) is triggered, the external OVP MOSFET (if used) and power stage turn off. The ADP pin also provides the IC's internal bias voltage.
29	FB	**Feedback pin.** FB is the output voltage (V_{OUT}) feedback pin in source mode. If V_{OUT} at the IN pin is configured via the register in source mode, this pin is not functional. Leave this pin floating or connect it to AGND via a 10kΩ resistor.

ABSOLUTE MAXIMUM RATINGS (1)

ADP, ACGATE to PGND (DC).....-0.3V to +28V
IAP, IAN, IN to PGND (DC).....-0.3V to +26V
IAP, IAN, IN to PGND (20ns).....-0.3V to +28V
IAP to IAN .....-3.6V to +3.6V
SW1, SW2 to PGND (DC) .....-0.3V to +24V
SW1, SW2 to PGND (20ns).....-2V to +28V
CFLR, BATT to PGND .....-0.3V to +24V
SRP, SRN to PGND .....-0.3V to +24V
SRP to SRN.....-3.6V to +3.6V
BST1 to SW1 ..... 0 to 5V
BST2 to SW2 ..... 0 to 5V
All other pins to AGND.....-0.3V to +5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charge device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 22V
Input current (I_{IN}).....Up to 6A
Charge current (I_{CC}) .....Up to 6A
Battery voltage (V_{BATT}) .....Up to 18.68V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-30 (4mmx5mm) ..... 38 ..... 8.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input voltage range	V_{IN}		4		22	V
ADP under-voltage lockout (UVLO) threshold	V_{ADP_UVLO}	V_{ADP} falling	2.4	2.6	2.8	V
ADP UVLO hysteresis		V_{ADP} rising		1		V
ADP over-voltage lockout (OVLO) threshold	V_{ADP_OVP}	V_{ADP} rising	23	23.9	24.7	V
ADP OVLO hysteresis		V_{ADP} falling		500		mV
ADP over-voltage protection (OVP) recover deglitch time		V_{ADP} falling		100		ms
Input UVLO recovery degltich time	t_{INUVLO_DGL}	V_{IN} rising		30		ms
Input under-voltage protection (UVP)	V_{IN_UVP}	V_{IN} falling, REG11h, bits[9:8] = 00	2.9	3.2	3.5	V
		V_{IN} falling, REG11h, bits[9:8] = 01	6	6.4	6.8	V
		V_{IN} falling, REG11h, bits[9:8] = 10	11.5	12	12.5	V
		V_{IN} falling, REG11h, bits[9:8] = 11	16.2	16.8	17.4	V
Input UVP threshold hysteresis		V_{IN} rising, REG11h, bits[9:8] = 01/10/11		328		mV
		V_{IN} rising, REG11h, bits[9:8] = 00		490		mV
Input UVP recovery deglitch time	t_{INUVP_DGL}	V_{IN} rising		30		ms
Input OVP threshold	V_{IN_OVP}	V_{IN} rising, REG11h, bits[7:6] = 00	6.9	7.25	7.6	V
		V_{IN} rising, REG11h, bits[7:6] = 01	10.8	11.25	11.7	V
		V_{IN} rising, REG11h, bits[7:6] = 10	17	17.65	18.25	V
		V_{IN} rising, REG11h, bits[7:6] = 11	22	22.45	23.15	V
Input OVP deglitch time	t_{INOVP_DGL}	V_{IN} rising, REG11h, bit[10] = 0		1		µs
		V_{IN} rising, REG11h, bit[10] = 1		15		ms
Input OVP hysteresis		V_{IN} falling		320		mV
Input OVP recover deglitch time		V_{IN} falling		30		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DC/DC Converter						
Input quiescent current	I_{IN_Q}	V_{IN} = 5V, buck-boost and the ACGATE driver are disabled		550	620	µA
		V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}, buck-boost is disabled, ACGATE is enabled		1	1.2	mA
VCC low-dropout regulator (LDO) output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 15mA		3.6		V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{VCC} = 3.3V		23		mA
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			10		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			8		mΩ
CFLR to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			8		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			20		mΩ
Switching frequency	f_{SW}	REG0Eh, bits[6:4] = 000	450	500	550	kHz
		REG0Eh, bits[6:4] = 001	540	600	660	kHz
		REG0Eh, bits[6:4] = 010	630	700	770	kHz
		REG0Eh, bits[6:4] = 100	675	750	825	kHz
		REG0Eh, bits[6:4] = 011	720	800	880	kHz
		REG0Eh, bits[6:4] = 101	810	900	990	kHz
		REG0Eh, bits[6:4] = 110	900	1000	1100	kHz
		REG0Eh, bits[6:4] = 111	1070	1200	1280	kHz
Battery Charger						
Battery charge voltage regulation range	V_{BATT_REG}	1-cell OTP code setting	3.4		4.67	V
		2-cell OTP code setting	6.8		9.34	V
		3-cell OTP code setting	10.2		14.01	V
		4-cell OTP code setting	13.6		18.68	V
Battery charge voltage regulation accuracy		T_A = 25°C, V_{BATT_REG} = 4.35V, 1-cell OTP setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 4.35V, 1-cell OTP setting	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 8.4V, 2-cell OTP setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 8.4V, 2-cell OTP setting	-0.7		+0.7	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery charge voltage regulation accuracy (continued)		T_A = 25°C, V_{BATT_REG} = 12.6V, 3-cell OTP setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 12.6V, 3-cell OTP setting	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 16.8V, 4-cell OTP setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 16.8V, 4-cell OTP setting	-0.7		+0.7	%
Fast charge current range	I_{CC}	RS2 = 10mΩ, REG10h, bit[7] = 0	0		6.35	A
Fast charge current accuracy	I_{CC_ACC}	I_{CC} = 6A, REG14h, bits[13:6] = 0111 1000	5.79	6	6.2	A
		I_{CC} = 3A, REG14h, bits[13:6] = 0011 1100	2.84	3	3.14	A
		I_{CC} = 2A, REG14h, bits[13:6] = 0010 1000	1.88	2	2.13	A
		I_{CC} = 500mA, REG14h, bits[13:6] = 0000 1010	0.4	0.5	0.6	A
Pre-charge to fast charge threshold	V_{BATT_PRE}	REG0Bh, bit[12] = 1	2.9	3	3.1	V/cell
		REG0Bh, bit[12] = 0	2.45	2.55	2.6	V/cell
Pre-charge to fast charge deglitch time				30		ms
Pre-charge to fast charge hysteresis		1 cell		85		mV
		2 cells		160		mV
		3 cells		240		mV
		4 cells		315		mV
Pre-charge current range	I_{PRE}	RS2 = 10mΩ, REG10h, bit[7] = 0	0		1.5	A
Pre-charge current accuracy		V_{BATT} = 5V, I_{PRE} = 300mA, REG0Fh, bits[7:4] = 0011	-20		+20	%
		V_{BATT} = 5V, I_{PRE} = 500mA, REG0Fh, bits[7:4] = 0101	-15		+15	%
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising		2		V/cell
Trickle charge to pre-charge hysteresis		V_{BATT} falling		200		mV/cell

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Trickle charge current range	I_{TC}	RS2 = 10mΩ, REG10h, bit[7] = 0	0		750	mA
Trickle charge current accuracy		2 cells, V_{BATT} = 5V, REG0Fh, bits[11:8] = 0010, I_{TC} = 100mA	50	100	160	mA
Auto-recharge battery voltage threshold		Below battery charge voltage, REG10h, bit[11] = 0		-120		mV/cell
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising	170	230	285	mV/cell
Battery OVP hysteresis		V_{BATT} falling		113		mV/cell
Battery OVP deglitch time				30		ms
TC and pre-charge timer			1.8	2	2.2	hours
Constant current (CC) and constant voltage (CV) charge timer		REG12h, bits[12:11] = 11	18	20	22	hours
Termination current accuracy	I_{TERM}	I_{TERM} = 100mA, REG0Fh, bits[3:0] = 0010	60	120	180	mA
		I_{TERM} = 200mA, REG0Fh, bits[3:0] = 0100	160	220	290	mA
		I_{TERM} = 400mA, REG0Fh, bits[3:0] = 1000	360	420	490	mA
Charge termination deglitch time	t_{TERM_DGL}			1		s
Pin Leakage Current						
SRP, SRN leakage current	$I_{LKG\_SRP\_SRN}$		-0.5		+0.5	µA
IAP, IAN leakage current	$I_{LKG\_IAP\_IAN}$		-0.5		+0.5	µA
Input Current (I_{IN}) Limit and Input Voltage (V_{IN}) Limit						
I_{IN} limit range	I_{IN_LIM}	RS1 = 10mΩ, REG10, bit[8] = 0	0		5.8	A
I_{IN} limit accuracy	$I_{IN\_LIM\_ACC}$	REG08h, bits[6:0] = 000 1010, I_{IN_LIM} = 0.5A	0.368	0.43	0.5	A
		REG08h, bits[6:0] = 001 0010, I_{IN_LIM} = 0.9A	0.768	0.82	0.9	A
		REG08h, bits[6:0] = 001 1110, I_{IN_LIM} = 1.5A	1.32	1.41	1.5	A
		REG08h, bits[6:0] = 011 1100, I_{IN_LIM} = 3A	2.76	2.87	2.98	A
		REG08h, bits[6:0] = 110 0100, I_{IN_LIM} = 5A	4.688	4.836	4.98	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum V_{IN} regulation	V_{IN_MIN}	REG06h, bits[7:0] = 0011 1001, V_{IN_MIN} = 4.56V	4.44	4.58	4.72	V
		REG06h, bits[7:0] = 1000 0010, V_{IN_MIN} = 10.4V	10.19	10.4	10.61	V
		REG06h, bits[7:0] = 1010 1010, V_{IN_MIN} = 13.6V	13.33	13.6	13.87	V
		REG06h, bits[7:0] = 1110 0111, V_{IN_MIN} = 18.48V	18.11	18.48	18.85	V
Thermal Regulation and Protection						
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)				20		°C
Thermal regulation threshold	T_{J_REG}	REG0Fh, bits[14:12] = 111		120		°C
Battery Temperature Monitoring						
NTC floating threshold	V_{NTC_FLT}	V_{NTC} rising as a percentage of V_{VNTC}		95		%
NTC floating threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		3		%
NTC cold temp threshold	V_{COLD}	V_{NTC} rising as a percentage of V_{VNTC}, REG0Dh, bits[1:0] = 01	73.5	74.5	75.5	%
NTC cold temp threshold hysteresis		V_{NTC} falling as percentage of V_{VNTC}		1.2		%
NTC cool temp threshold	V_{COOL}	V_{NTC} rising as a percentage of V_{VNTC}, REG0Dh, bits[3:2] = 10	64.2	65.2	66.2	%
NTC cool temp threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		1.2		%
NTC warm temp threshold	V_{WARM}	V_{NTC} falling as a percentage of V_{VNTC}, REG0Dh, bits[5:4] = 01	32.2	33.2	34.2	%
NTC warm temp threshold hysteresis		V_{NTC} rising as a percentage of V_{VNTC}		1.2		%
NTC hot temp threshold	V_{HOT}	V_{NTC} falling as a percentage of V_{NTC}, REG0Dh, bits[7:6] = 10	22.6	23.6	24.6	%
NTC hot temp threshold hysteresis		V_{NTC} rising as a percentage of V_{NTC}		1.2		%
TS hot threshold	V_{TS}	REG0Dh, bits[12:10] = 011, T_A = 100°C	12.5	13.5	14.5	%
VNTC voltage	V_{VNTC}		1.26	1.28	1.30	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Source Mode						
Output voltage in source mode	V_{IN_SRC}	I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 00 1111 1010	4.85	5	5.15	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 01 1100 0010	8.82	9	9.18	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 0101 1000	11.76	12	12.24	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 1110 1110	14.7	15	15.3	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 11 1110 1000	19.7	20	20.3	V
FB reference voltage for external setting	V_{FB}	REG09h, bits[9:0] = 11 1110 1000	1.194	1.206	1.218	V
		REG09h, bits[9:0] = 00 1111 1010	0.306	0.313	0.32	V
Output OVP in source mode	$V_{IN\_SRC\_OV}$	V_{BATT} = 7.4V, V_{IN} rising, percentage of discharge voltage setting, REG11h, bits[14:13] = 11		110		%
Output OVP hysteresis in source mode		V_{IN} falling		5		%
Output UVP in source mode	$V_{IN\_SRC\_UV}$	REG11h, bits[12:11] = 00		75		%
Output UVP hysteresis in source mode				5		%
Discharge output under-voltage (UV) deglitch time		V_{IN} falling		10		ms
Discharge output UV recovery deglitch time		V_{IN} rising		30		ms
Output current regulation in discharge mode	I_{IN_SRC}	REG0Ah, bits[6:0] = 001 1110, V_{BATT} = 7.4V	0.9			A
		REG0Ah, bits[6:0] = 010 1100, V_{BATT} = 7.4V	1.5			A
		REG0Ah, bits[6:0] = 100 1100, V_{BATT} = 7.4V	3			A
Battery UVLO threshold	V_{BATT_UVLO}	V_{BATT} falling	2.5	2.6	2.7	V/cell
Battery UVLO hysteresis		V_{BATT} rising		280		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery low voltage threshold	V_{BATT_LOW}	V_{BATT} falling, REG0Bh, bits[10:9] = 10	3.1	3.2	3.3	V/cell
Battery low voltage hysteresis		V_{BATT} rising		200		mV/cell
Battery low voltage deglitch time		V_{BATT} falling		30		ms
Battery quiescent current	I_{BATT_Q}	V_{IN} = 0V, V_{BATT} = 8.4V, source mode is disabled, ADC, watchdog timer and ACGATE driver are disabled		33	39.5	µA
		V_{IN} = 0V, V_{BATT} = 8.4V, source mode is disabled, ADC and ACGATE driver are disabled, Watchdog timer is enabled			0.655	mA
		V_{IN}= 0V, V_{BATT} = 8.4V, source mode is disabled, ADC and watchdog timer are enabled, ACGATE driver is disabled			3.2	mA
ACGATE Driver						
ACGATE	V_{ACGATE}	Above V_{ADP} when enabled		6		V
		Above V_{ADP} when disabled		0		V
Open-Drain Pin Characteristics (INT, ACOK)						
Logic-low voltage threshold	V_L	10mA sink current			0.4	V
Analog-to-Digital Converter (ADC)						
Sample rate				50		kHz
ADC reference				1.28		V
ADC resolution				10		Bits
SMBus Interface (6)						
Input high threshold level	V_{IH}	$V_{PULL\ UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 1mA			0.4	V
Input leakage current	I_{LEAK}		-0.2		+0.2	µA
SMBus Timing Characteristics (5)						
SMBus clock frequency	f_{SCL}		10		400	kHz
Bus free time		Between a stop and start condition	4.7			µs
Start condition hold time, after which the first clock pulse is generated			4			µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start condition set-up time			4.7			µs
Stop condition set-up time			4			µs
Data hold time			300			ns
Data set-up time			250			ns
Clock low timeout			25		35	ms
Clock low period			4.7			µs
Clock high period			4		50	µs
Clock/data falling time					300	ns
Clock/data rising time					1000	ns

Notes:

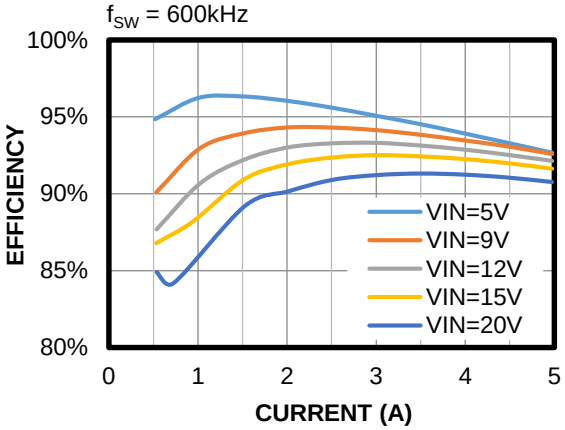
5) Guaranteed by design.
6) The SMBus should cover the I^2C specifications; the I^2C/SMBus lines are compatible with 1.8V/3.3V/5V logic.

TYPICAL CHARACTERISTICS

Inductor DCR = 10mΩ, unless otherwise noted.

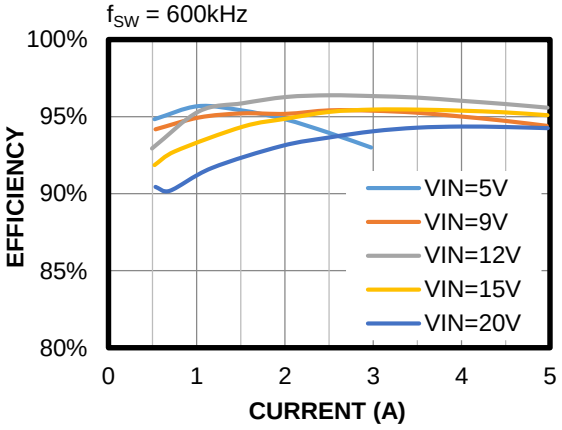
Efficiency vs. Charge Current

Charge mode with 1-cell battery, V_{BATT} = 4V, V_{IN} = 5V, 9V, 12V, 15V, or 20V, f_{SW} = 600kHz



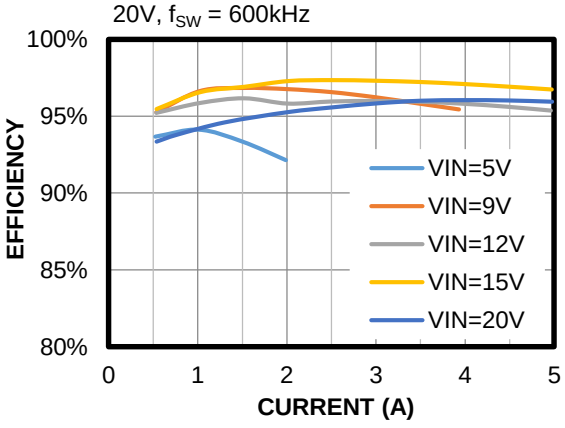
Efficiency vs. Charge Current

Charge mode with 2-cell battery, V_{BATT} = 8V, V_{IN} = 5V, 9V, 12V, 15V, or 20V, f_{SW} = 600kHz



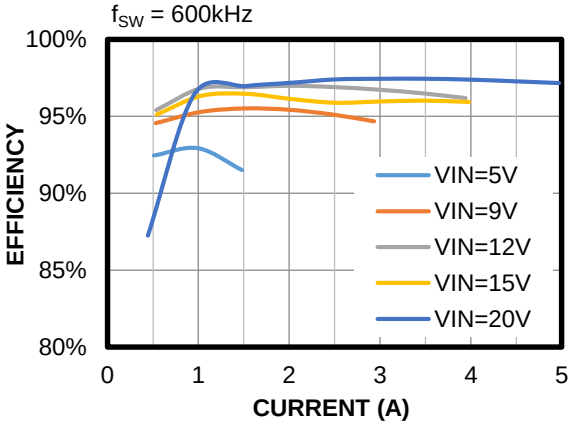
Efficiency vs. Charge Current

Charge mode with 3-cell battery, V_{BATT} = 12V, V_{IN} = 5V, 9V, 12V, 15V, or 20V, f_{SW} = 600kHz



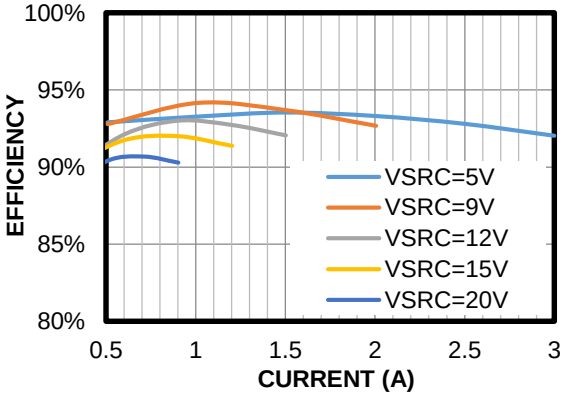
Efficiency vs. Charge Current

Charge mode with 4-cell battery, V_{BATT} = 16V, V_{IN} = 5V, 9V, 12V, or 20V, f_{SW} = 600kHz



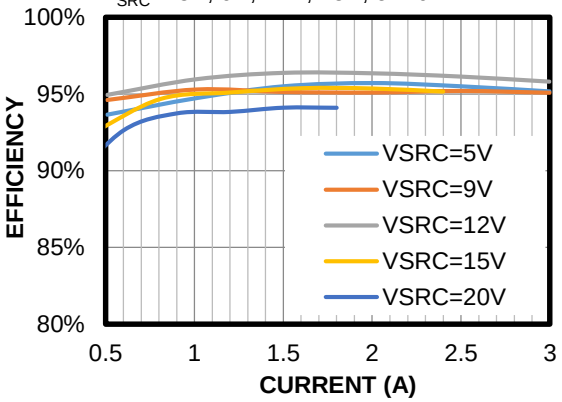
Efficiency vs. Source Current

Source mode with 1-cell battery, V_{BATT} = 4.2V, f_{SW} = 600kHz, V_{SRC} = 5V, 9V, 12V, 15V, or 20V



Efficiency vs. Source Current

Source mode with 2-cell battery, V_{BATT} = 8.4V, f_{SW} = 600kHz, V_{SRC} = 5V, 9V, 12V, 15V, or 20V

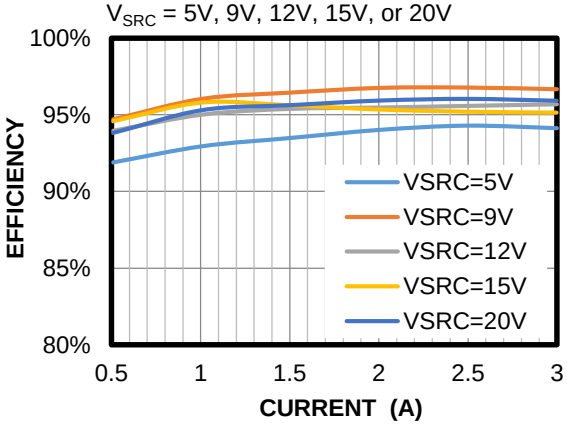


TYPICAL CHARACTERISTICS *(continued)*

Inductor DCR = 10mΩ, unless otherwise noted.

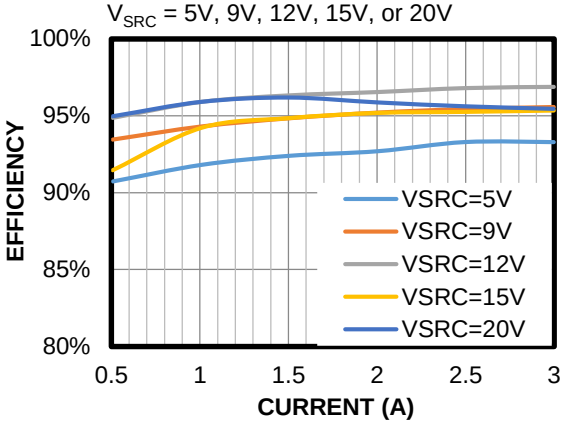
Efficiency vs. Source Current

Source mode with 3-cell battery,
V_{BATT} = 12.6V, f_{SW} = 600kHz,
V_{SRC} = 5V, 9V, 12V, 15V, or 20V



Efficiency vs. Source Current

Source mode with 4-cell battery,
V_{BATT} = 16.8V, f_{SW} = 600kHz,
V_{SRC} = 5V, 9V, 12V, 15V, or 20V

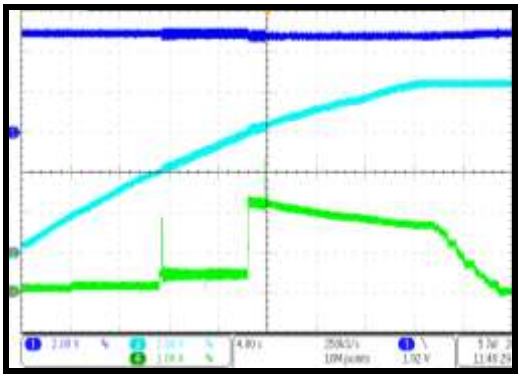


TYPICAL PERFORMANCE CHARACTERISTICS

The performance waveforms are tested on the evaluation board (see the Design Example section on page 57). C_{IN} = 5 x 10µF + 1µF, C_{CFLR} = 2 x 22µF + 1µF, C_{BATT} = 2 x 22µF, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

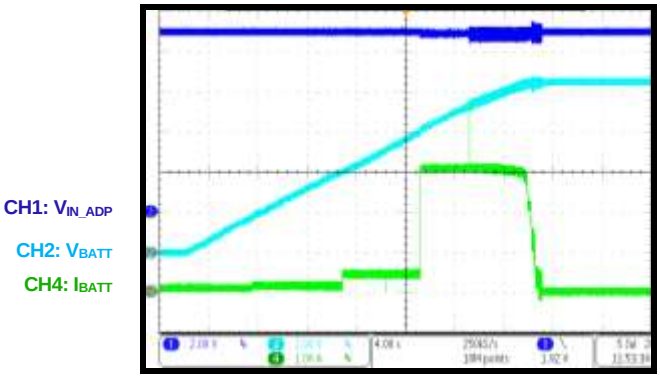
Charge Profile

V_{IN_ADP} = 5V, I_{IN_LIM} = 3A, I_{CC} = 3A,
V_{BATT_REG} = 8.4V, battery simulator: 10mV/step



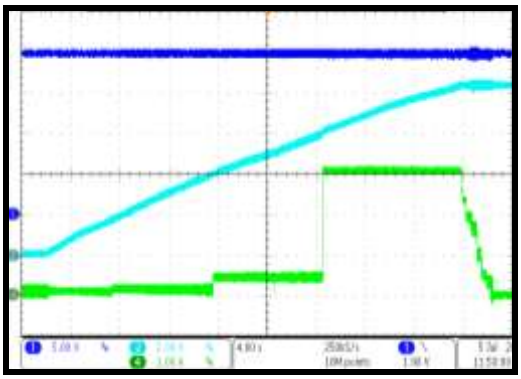
Charge Profile

V_{IN_ADP} = 9V, I_{IN_LIM} = 3A, I_{CC} = 3A,
V_{BATT_REG} = 8.4V, battery simulator: 10mV/step



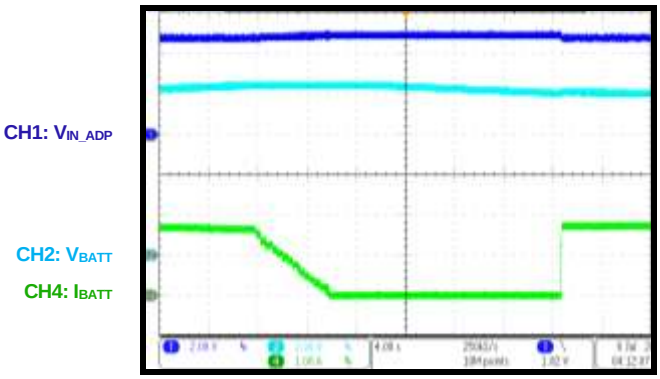
Charge Profile

V_{IN_ADP} = 20V, I_{IN_LIM} = 3A, I_{CC} = 3A,
V_{BATT_REG} = 8.4V, battery simulator: 10mV/step



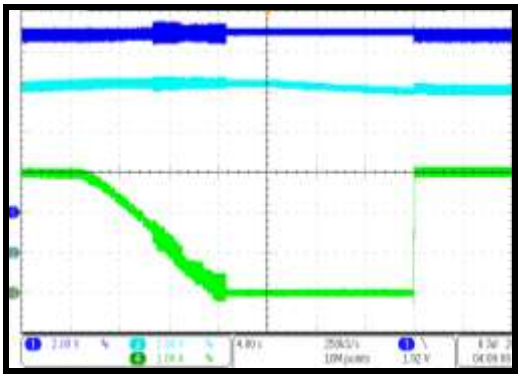
Auto-Recharge Profile

V_{IN_ADP} = 5V, I_{IN_LIM} = 3A, V_{BATT_REG} = 8.4V (2 cells), I_{CC} = 3A, battery simulator: 5mV/step



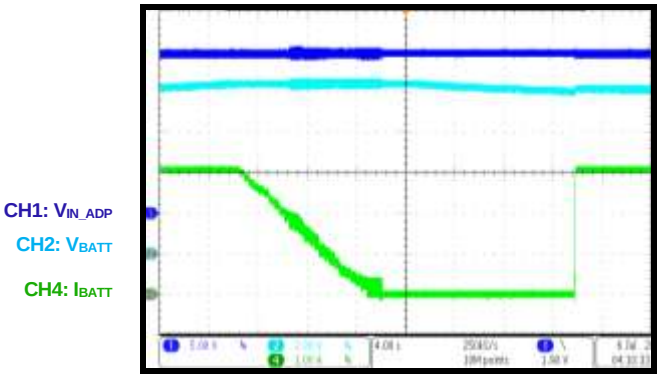
Auto-Recharge Profile

V_{IN_ADP} = 9V, I_{IN_LIM} = 3A, V_{BATT_REG} = 8.4V (2 cells), I_{CC} = 3A, battery simulator: 10mV/step



Auto-Recharge Profile

V_{IN_ADP} = 20V, I_{IN_LIM} = 3A, V_{BATT_REG} = 8.4V (2 cells), I_{CC} = 3A, battery simulator: 10mV/step

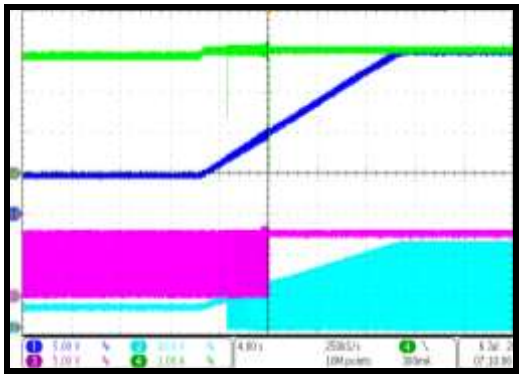


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

The performance waveforms are tested on the evaluation board (see the Design Example section on page 57). C_{IN} = 5 x 10µF + 1µF, C_{CFLR} = 2 x 22µF + 1µF, C_{BATT} = 2 x 22µF, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3000mA, 2-cell applications, V_{BATT_REG} = 8.4V, unless otherwise noted.

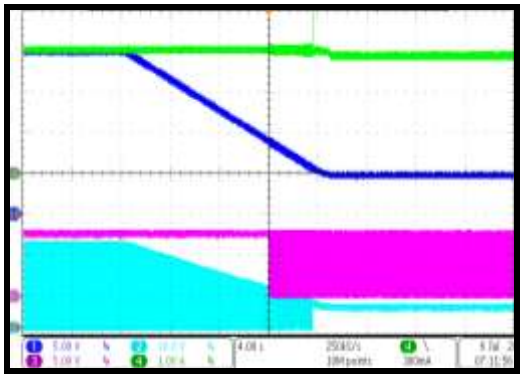
V_{IN_ADP} Steps from 5V to 20V

V_{BATT} = 7.4V (2 cells), I_{CC} = 3A, charge enabled



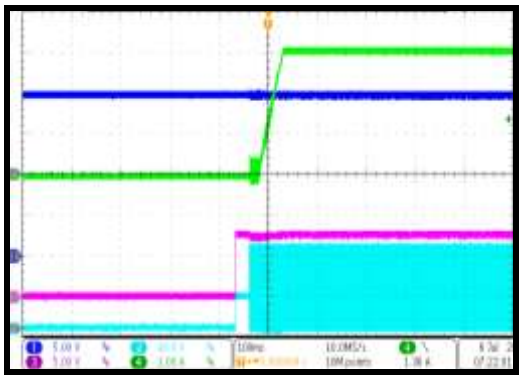
V_{IN_ADP} Steps from 20V to 5V

V_{BATT} = 7.4V (2 cells), I_{CC} = 3A, charge enabled



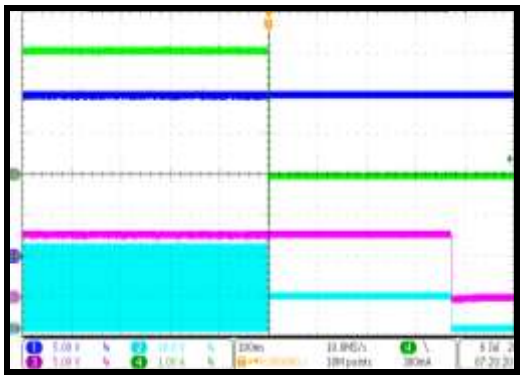
Charge Enabled

V_{IN_ADP} = 20V, V_{BATT} = 7.4V (2 cells), I_{CC} = 3A



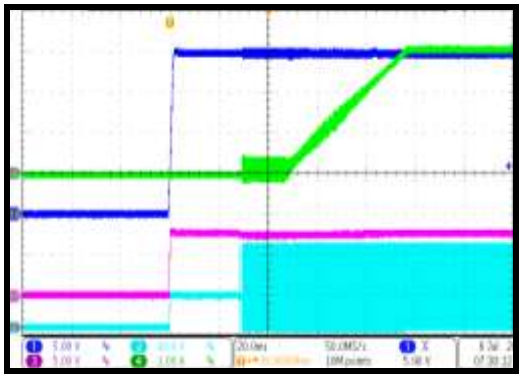
Charge Disabled

V_{IN_ADP} = 20V, V_{BATT} = 7.4V (2 cells), I_{CC} = 3A



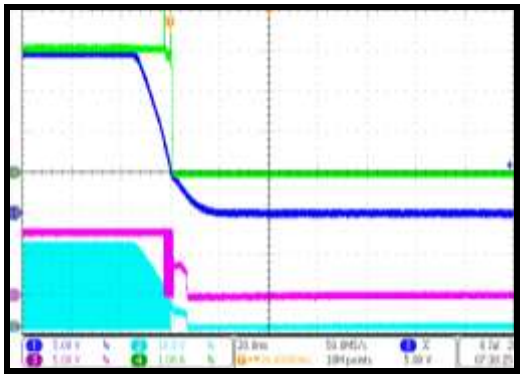
Input Start-Up

V_{IN_ADP} = 20V, V_{BATT} = 7.4V (2 cells), I_{CC} = 3A



Input Shutdown

V_{IN_ADP} = 20V, V_{BATT} = 7.4V (2 cells), I_{CC} = 3A

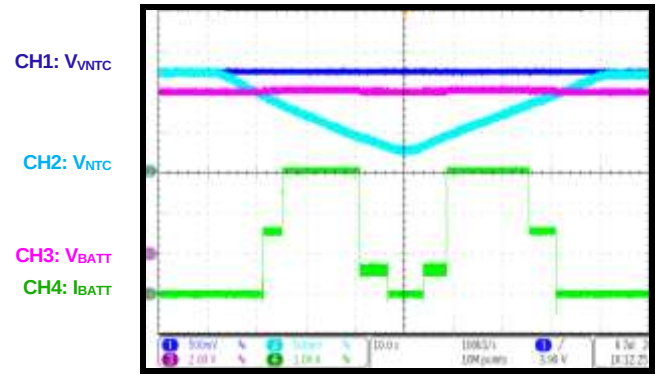


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

The performance waveforms are tested on the evaluation board (see the Design Example section on page 57). C_{IN} = 5 x 10µF + 1µF, C_{CFLR} = 2 x 22µF + 1µF, C_{BATT} = 2 x 22µF, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

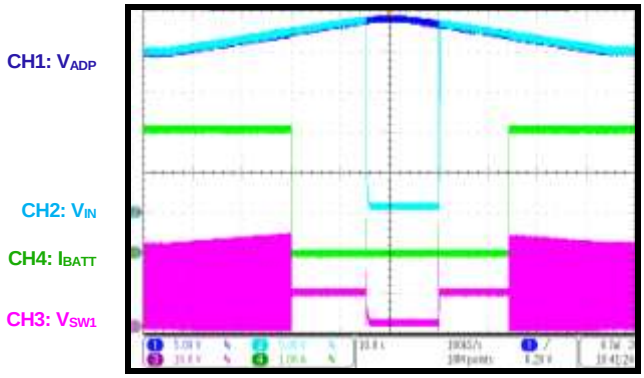
JEITA-Compatible NTC Protection

V_{IN_ADP} = 12V, V_{BATT} = 8V, V_{BATT_REG} falls 400mV in warm window, I_{CC} drops by 50% in cool window



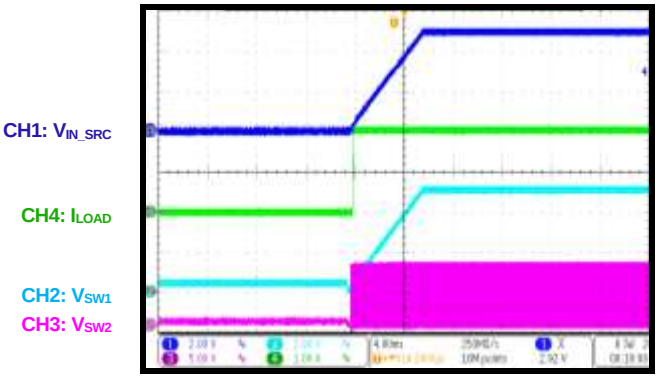
ADP and IN OVP

V_{BATT} = 8V, enable ACGATE driver with external N-channel pass through MOSFET, ramp V_{ADP} up and down



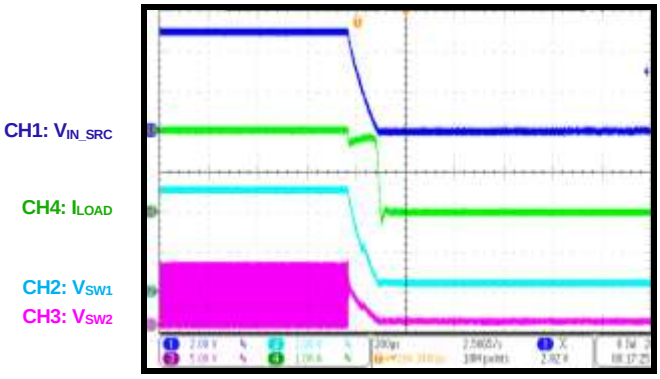
Source Mode Enabled

V_{BATT} = 7.4V (2 cells), $V_{IN\text{-}SRC}$ = 5V, I_{IN_SRC} = 2A (CC load)



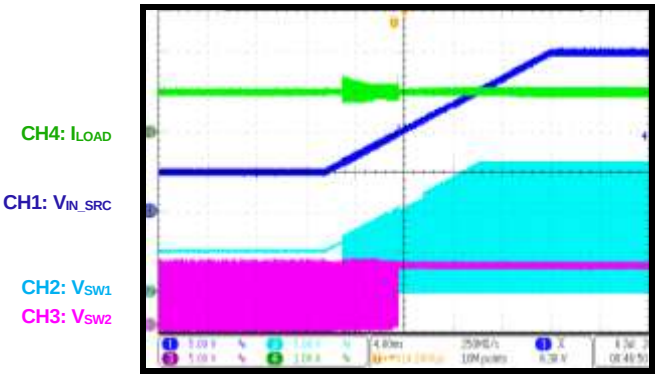
Shutdown through VIN

V_{BATT} = 7.4V (2 cells), $V_{IN\text{-}SRC}$ = 5V, I_{IN_SRC} = 2A (CC load)



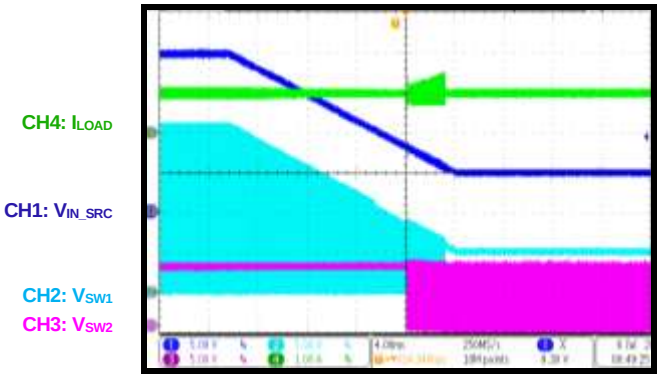
V_{IN_SRC} Steps from 5V to 20V

V_{BATT} = 7.4V (2 cells), $V_{IN\text{-}SRC}$ = 5V to 20V, I_{IN_SRC} = 1A (CC load)



V_{IN_SRC} Steps from 20V to 5V

V_{BATT} = 7.4V (2 cells), $V_{IN\text{-}SRC}$ = 20V to 5V, I_{IN_SRC} = 1A (CC load)

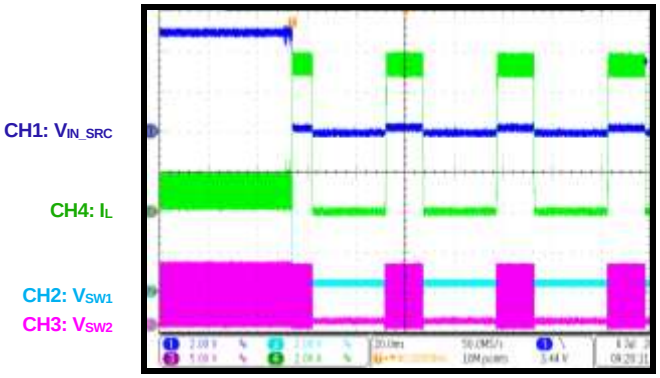


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

The performance waveforms are tested on the evaluation board (see the Design Example section on page 57). C_{IN} = 5 x 10µF + 1µF, C_{CFLR} = 2 x 22µF + 1µF, C_{BATT} = 2 x 22µF, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3000mA, 2-cell application, V_{BATT_REG} = 8.4V, unless otherwise noted.

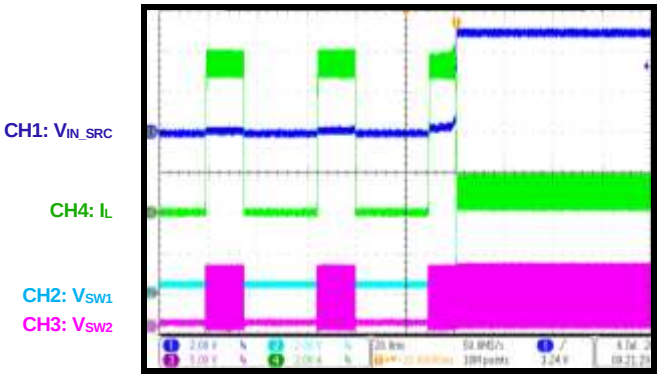
V_{IN_SRC} Short Protection

V_{BATT} = 7.4V (2 cells), V_{IN-SRC} = 5V,
I_{IN_SRC} = 1A (CC load)



V_{IN_SRC} Short Recovery

V_{BATT} = 7.4V (2 cells), V_{IN-SRC} = 5V,
I_{IN_SRC} = 1A (CC load)



FUNCTIONAL BLOCK DIAGRAM

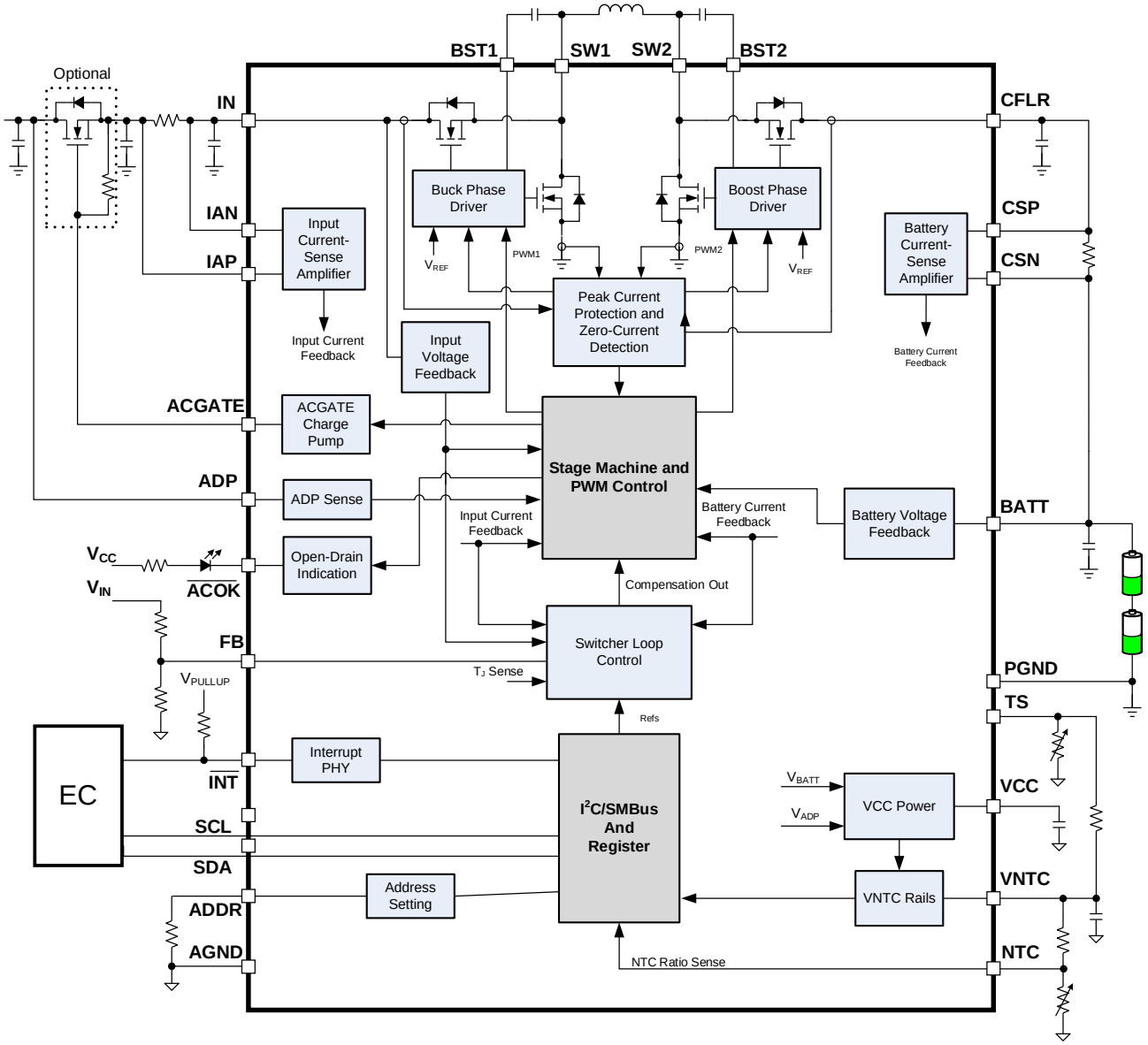


Figure 2: Functional Block Diagram

OPERATION

Introduction

The MP2651 is a highly integrated buck-boost charger IC with four switching FETs (Q1, Q2, Q3, and Q4) for battery packs with 1 to 4 cells in series. It also integrates one N-channel MOSFET driver for higher input over-voltage protection (VAP OVP).

The MP2651 also can operate in the reverse direction to power the input from the battery which is compliant to the USB PD source mode.

When input power is present, the MP2651 operates in charge mode. The buck-boost converter has three operating modes: boost mode when the input voltage (V_{IN}) is below the battery voltage (V_{BATT}), buck mode when V_{IN} exceeds the battery voltage, and buck-boost mode when V_{IN} is almost equal to the battery voltage. Figure 3 shows the power structure.

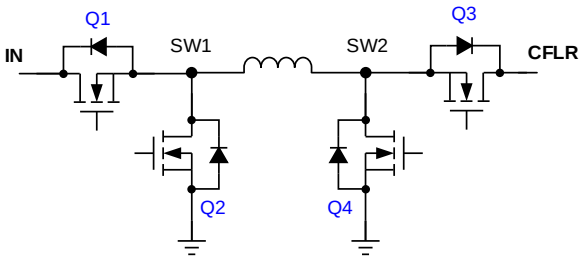


Figure 3: The MP2651 Power Structure

Table 1 shows the MOSFETs' operation modes while the device works in charge mode.

Table 1: MOSFET Operation in Charge Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	On
Q4	Switching	Switching	Off

Table 2 shows the MOSFETs' operation modes while the device works in source mode.

Table 2: MOSFET Operation in Source Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	On	Switching	Switching
Q4	Off	Switching	Switching

When the input is absent, the device operates in reverse to power the input from the battery via I²C/SMBus control. The MP2651 can provide a 3V to 21V output voltage (V_{OUT}), with 20mV/step at the input. The device also has an output current (I_{OUT}) limit with 50mA/step in this mode. This mode is called source mode in USB PD applications.

VCC LDO Output

The MP2651 integrates a low-dropout regulator (LDO) to power internal circuitry including the I²C block, FET driver, and bias current.

VCC is powered by V_{ADP} or V_{BATT}. When the ADP pin's voltage (V_{ADP}) exceeds V_{ADP_UVLO}, VCC is powered by V_{ADP}, regardless of whether the MP2651 is in charge mode or source mode. When the input is absent or V_{ADP} is below V_{ADP_UVLO}, VCC is powered by V_{BATT} while $V_{BATT} > V_{BATT\_UVLO}$.

The VCC can provide a 3.6V output to supply power to the internal circuit and open-drain pin's pull-up voltage. It is not recommended to power other circuits.

Input Power Status Indication

The MP2651 has both an $\overline{ACOK}$ pin and a register to indicate when the input power supply is in charge mode. The $\overline{ACOK}$ pin is an open-drain structure that is pulled to AGND when $V_{IN\_UVP} < V_{IN} < V_{IN\_OVP}$.

The PG_STAT register indicates when the power is good.

Input Over-Voltage Protection (OVP)

The MP2651 provides two input over-voltage protection (OVP) thresholds: V_{ADP_OVP} and V_{IN_OVP}.

The ADP pin senses the input voltage. If $V_{ADP} > V_{ADP\_OVP}$, the ACGATE pin pulls low to turn off M1 immediately; at the same time, buck-boost mode turns off (see Figure 4 on page 23). The MP2651 reports the ADP OVP fault in the fault register. There is a 100ms deglitch time to recover from ADP OVP.

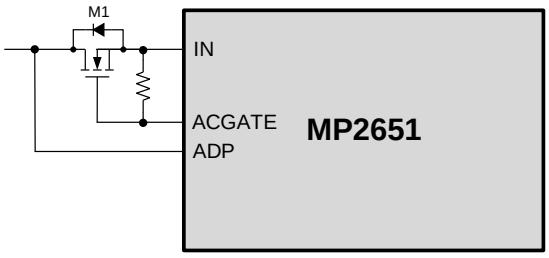


Figure 4: ACGATE Driver

When $V_{IN\_OVP} < V_{IN} < V_{ADP\_OVP}$, M1 still turns on, and the MP2651's switcher is disabled. Then a fault is reported in REG17h, bit[13].

Input Current Limit and Input Voltage Limit Regulation

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the MP2651 has both input current (I_{IN}) limit and V_{IN} limit regulation. If either the I_{IN} limit or V_{IN} limit is reached, the MP2651 regulates the duty cycles of Q1 and Q4 to limit the input power according to the setting.

Battery Charge Profile

In charge mode, the MP2651 regulates five control loops: V_{IN}, I_{IN}, charge current, battery-full regulation voltage, and device junction temperature.

The device provides four main charging phases: constant current trickle charge, constant pre-charge, constant current (CC) fast charge, and constant voltage (CV) charge (see Figure 5).

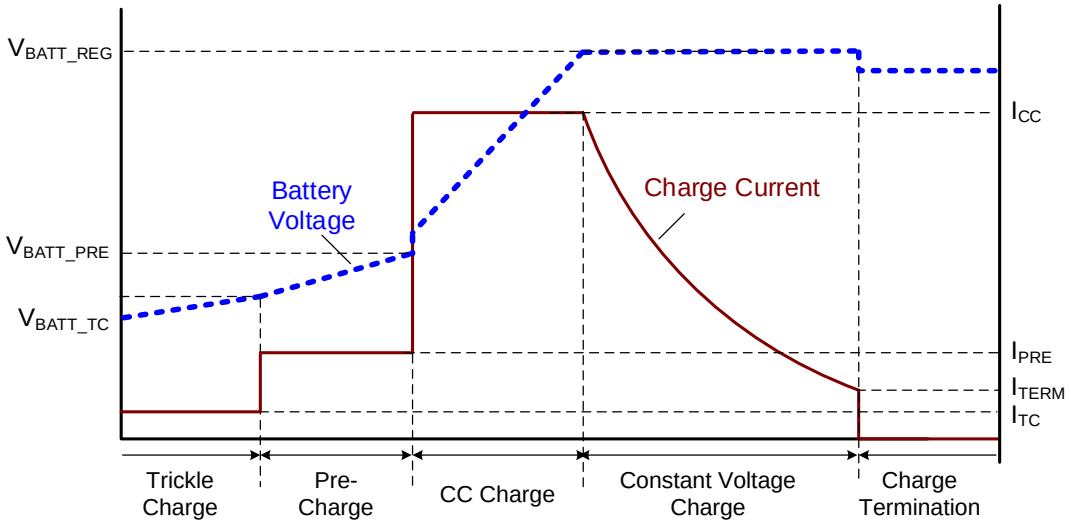


Figure 5: Charge Profile

Constant Current Trickle Charge (Phase 1)

When the input power qualifies as a good power supply, the IC checks the battery voltage to determine whether trickle charging is required. If the battery voltage is below V_{BATT_TC}, a configurable trickle-charge current is applied to the battery.

Constant Current Pre-Charge (Phase 2)

When V_{BATT} exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (about 2 hours) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted.

The pre-charge current can be configured via the I^2C register REG0Fh, bits[7:4], while V_{BATT_PRE} can be configured by REG0Bh, bit[12]. There are two options for this threshold: 2.5V/cell for LiFePO4 batteries, and 3V/cell for Li-ion batteries with other chemistries.

Constant Current Fast Charge (Phase 3)

When V_{BATT} exceeds V_{BATT_PRE} (set via REG0Bh, bit[12]), the IC enters the constant current charge (fast charge) phase.

The fast charge current can be configured via REG14h, bits[13:6].

Constant Voltage Charge (Phase 4)

When V_{BATT} reaches the level of the configurable battery-full voltage (V_{BATT_REG}, set via REG15h, bits[14:4]), the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the termination threshold (I_{TERM}) set via REG0Fh, bits[3:0], assuming that the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle stops and a corresponding timeout fault signal is asserted (see the Safety Timer section on page 25 for more details).

Automatic Recharge

When the battery is fully charged, charging is terminated and the battery may be discharged because of the system consumption or self-discharge. When V_{BATT} falls below the configurable recharge threshold, the IC automatically starts a new charging cycle, which means there is no manual requirement to restart a charging cycle if the input power is valid. The timer resets when the automatic recharge cycle begins.

A new charge cycle starts once all of the following conditions are valid:

- The input power is plugged back in
- Battery charging is enabled by the I^2C/SMBus
- There is no thermistor fault
- There is no safety timer fault
- There is no battery over-voltage (OV) fault

This means that re-plugging the input power or toggling the battery charging control bit (REG12h, bit[0]) can restart a charge cycle without any fault occurring. The new charge cycle can start with any phase, since the phase depends on V_{BATT}.

Battery Over-Voltage Protection (OVP)

The IC has battery OVP. If V_{BATT} exceeds the battery OV threshold (about 230mV above the battery regulation voltage per cell), charging is disabled. Battery OVP has a 30ms deglitch time. The switcher is turned off during battery OVP.

Junction Thermal Regulation

The thermal regulation loop always monitors the IC's internal junction temperature. If the junction temperature exceeds the temperature limit, the charge current drops to regulate the junction temperature. There are multiple thermal regulation thresholds ranging between 80°C and 120°C, so that the system design can meet the thermal requirements of different applications. The junction temperature's regulation threshold can be set via REG0Fh, bits[14:12].

Transitions Between Buck, Boost, and Buck-Boost Mode

The MP2651 always monitors V_{IN} and the CFLR voltage to automatically switch between different modes (see Figure 6).

When V_{IN} exceeds 90% of V_{BATT}, the MP2651 transitions from boost mode to buck-boost mode.

When V_{IN} drops below 75% of V_{BATT}, the MP2651 transitions from buck-boost mode to boost mode.

When V_{IN} drops below 120% of V_{BATT}, the MP2651 transitions from buck mode to buck-boost mode.

When V_{IN} exceeds 135% of V_{BATT}, the MP2651 transitions from buck-boost mode to buck mode.

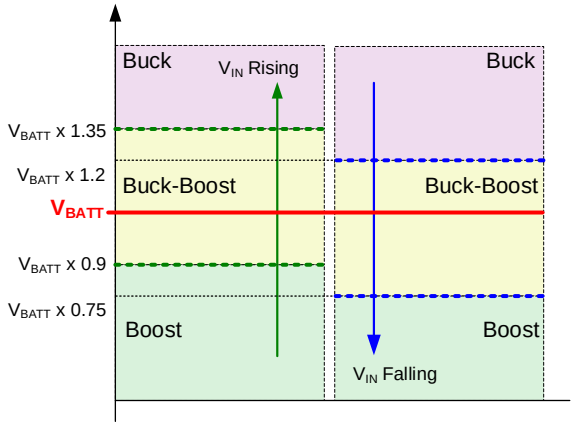


Figure 6: Mode Transition Threshold

Pulse-Skip Mode (PSM) Operation

The MP2651 utilizes pulse-skip mode (PSM) control to improve efficiency under light loads. In PSM, lighter loads mean the device skips more pulse width.

Cycle-by-Cycle MOSFET Current Limit

The MP2651 senses both the high-side and low-side MOSFET (HS-FET and LS-FET, respectively). During loop control, the device provides a valley current limit in buck mode and a peak current limit in boost mode for each cycle-by-cycle switching period. In buck mode, the next period does not start until the inductor current (I_L) drops to the valley current limit. Then I_L rises during the minimum on time to fold back the frequency after triggering the valley current limit.

ADC Conversion and Multiplexer

The MP2651 has a built-in, 10-bit SAR analog-to-digital converter (ADC) with 50kSPS. A 10-channel multiplexer measures the device's parameters (see Table 3).

Table 3: ADC Channels

Sink Mode	Source Mode
• V_{IN} • I_{IN} • V_{BATT} • Charge current • Battery temperature (NTC pin voltage ratio) • TS pin voltage ratio • Chip junction temperature	• Source voltage at the input • Source current at the input • V_{BATT} • Battery temperature • TS pin voltage ratio • Chip junction temperature

Safety Timer

The IC provides both the pre-charge and CC/CV charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is about 2 hours when V_{BATT} is below V_{BATT_PRE}.

The CC/CV charge safety timer starts when the battery enters the fast charge phase. The user can configure this time via REG12h, bits[12:11]. Above two safety timers can be disabled via REG12h, bit[13]. The safety timer does not operate in discharge mode.

The safety timer is reset at the beginning of a new charging cycle. The following actions restart the safety timer:

- Auto-recharge
- Charge enabled toggling
- Input power toggling
- Safety timer enable toggling
- Thermal shutdown recovery

The IC automatically suspends the timer if an NTC hot or cold fault occurs.

The IC automatically doubles the remaining time if any of the below conditions are met:

- I_{IN} limit loop kicks in
- V_{IN} limit loop kicks in
- Thermal regulation loop kicks in

Once the MP2651 no longer meets the conditions above, the timer returns to its standard remaining time. This function can be disabled via REG12h, bit[10].

Watchdog Timer

The MP2651 has a watchdog timer to monitor the I^2C interface. If the watchdog timer is enabled, the host must periodically reset the watchdog timer reset bit before the watchdog timer expires. If the watchdog timer expires, some of the registers are reset to their default values. See the Register Map on page 31 for more details.

The following actions reset the watchdog timer and force the device to recover from a watchdog timer fault:

- Write to watchdog timer reset bit
- Write to the charge current register (REG14h)
- Write to the battery regulation voltage register (REG15h)

The watchdog timer can be disabled via REG12h, bits[9:8].

Battery Temperature Monitoring via the Negative Temperature Coefficient (NTC) Thermistor

Thermistor is the generic name given to thermally sensitive resistors. A negative temperature coefficient (NTC) thermistor is generally called a thermistor. Depending on the manufacturing method and the structure, there are many shapes and characteristic for thermistors. Unless otherwise specified, thermistor resistance values are classified at a standard temperature of 25°C. The resistance of a temperature is solely a function of its absolute temperature.

Refer to the thermistor's datasheet to obtain the relevant parameters. Calculate the relationship between the resistance and absolute temperature of a thermistor with Equation (1):

$$R_1 = R_2 \times e^{\beta \cdot \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (1)$$

Where R_1 is the resistance at the absolute temperature T1, R_2 is the resistance at absolute temperature T2, and β is a constant that depends on the thermistor's material.

The MP2651 continuously monitors the battery's temperature by measuring the voltage at the NTC pin (V_{NTC}). This voltage is determined by the resistor divider since its ratio is produced by the NTC thermistor's resistance when the battery is under different ambient temperatures (see Figure 7).

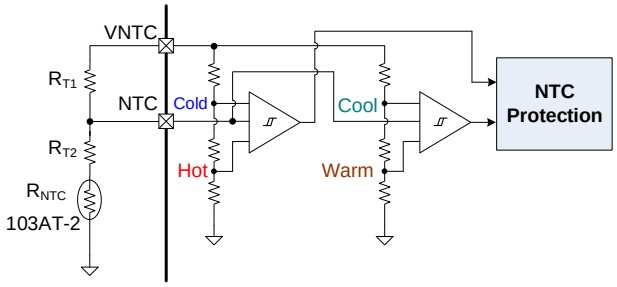


Figure 7: NTC Protection Circuit

The MP2651 internally sets a pre-determined upper and lower bound for V_{NTC} range. If V_{NTC} goes out of this range, the temperature is outside its safe operating limit. Then charging stops until the operating temperature returns into the safe range.

To satisfy the JEITA requirement, the MP2651 has four temperature thresholds: a cold battery threshold (0°C by default), cool battery threshold (10°C by default), warm battery threshold (45°C by default), and a hot battery threshold (60°C by default). For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}, respectively.

These thresholds can be configured via REG0Dh, bits[7:0]. When $V_{NTC} < V_{HOT}$ or $V_{NTC} > V_{COLD}$, charging is suspended and the timers are suspended. When $V_{HOT} < V_{NTC} < V_{WARM}$ or when $V_{COOL} < V_{NTC} < V_{COLD}$, the device responds based on what is set via REG0Ch, bits[14:4]. Figure 8 shows the JEITA control profile.

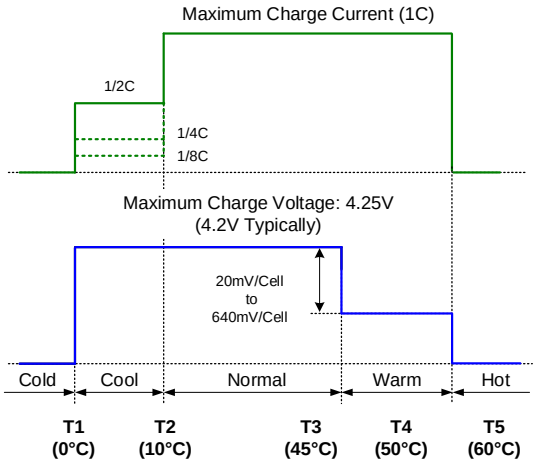


Figure 8: NTC Window

The MP2651 also monitors the battery temperature in discharge mode. NTC fault indication only occurs when the battery temperature is below the V_{COLD} threshold or above the V_{HOT} threshold.

NTC Floating Detection

If V_{NTC} exceeds 95% of 1.28V, an NTC float is detected, INT asserts, and the corresponding status register changes. The switcher turns off when NTC is floating.

Battery Missing Detection

The MP2651 counts how often charging terminates every 10s. If charge termination occurs more than three times in 10s, the MP2651 reports that the battery is missing via the status register and initiates an INT signal.

TS/IMON Pin Function

The MP2651 has a TS/IMON pin that is either used for temperature monitoring (TS) or current monitoring (IMON). When REG10h, bit[12] = 0, this pin is configured for temperature monitoring. When REG10h, bit[12] = 1, this pin is configured for charge current monitoring.

TS Function

When the TS function is enabled, the TS pin senses the input connector's temperature via REG0Dh, bits[12:10].

When the TS pin reaches V_{TS_HOT}, an INT signal asserts to indicate that a TS fault has occurred. In charge mode, the I_{IN} limit is reduced to 500mA with 50mA/Step every 62.5ms. When the IC recovers from a TS fault, the I_{IN} limit rises

to its set value with 50mA/step every 62.5ms.

By default, the triggered INT signal is masked by REG18h.

IMON Function

When the IMON function is used, the IMON pin represents the battery charge current with a gain of 0.1V/A.

Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the junction temperature reaches 150°C, the PWM converter shuts down. Normal operation does not resume until the junction temperature drops below 120°C.

Host Mode and Default Mode

The IC is a host-controlled device. After power-on reset (POR), the IC starts in the watchdog timer expiration state or in its default mode. All the registers are set to their default settings.

Any write to the IC forces it to host mode. All the device parameters can be configured by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG01h, bit[6] before the watchdog timer expires. If the watchdog timer expires, the IC goes back into default mode.

Impedance Compensation to Accelerate Charging

Throughout the entire charging cycle, the constant voltage charging stage takes a longer time. To accelerate the charging cycle, it is recommended for the device to stay in the constant current charging stage for as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the battery regulation voltage according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage provides additional safety measures. The real battery regulation voltage ($V_{BATT\_REG\_ACT}$) can be calculated with Equation (2):

$$V_{BATT\_REG\_ACT} = V_{BATT\_REG} + Min\ (V_{CLAMP},\ I_{CHG\_ACT}\ x\ R_{BATT}) \quad (2)$$

Where V_{BATT_REG} is the battery regulation voltage set via REG15h, bits[14:4], and I_{CHG_ACT} is the real-time charge current during operation.

Source Mode Operation

The MP2651 can operate in source mode to supply power to the IN pin using the battery. To ensure that the battery is not drained, the device does not enter this mode if the battery is below the configurable low battery threshold. Source mode operation can be enabled when REG12h, bit[3] = 1. When both charging and discharging are enabled, the discharge operation takes higher priority.

In source mode, the IC employs a fixed-frequency (500kHz to 1.2MHz, configurable) switching regulator. This regulator switches from PWM operation to PSM under light loads.

V_{OUT} is compliant with USB PD specifications. It can be set to 5V, 9V, 12V, 15V, or 20V, with 20mV/step, via the digital-to-analog-converter (DAC) in the register or the external FB pin.

The I_{OUT} limit can be configured via the I^2C/SMBus up to 5A, with 50mA/step. This is compliant with I^2C/SMBus specifications.

Discharge operation is enabled if both of the following conditions are met:

- $V_{BATT} > V_{BATT\_LOW}$
- REG12h, bit[3] = 1

To meet PD timing specifications, V_{OUT} should settle within 275ms.

In source mode, the switcher can work in buck mode, boost mode, or buck-boost mode, according to V_{BATT} and the discharge voltage.

Over-Voltage Protection (OVP) in Source Mode

The MP2651 features output OVP in source mode. The IC continuously monitors V_{IN} in source mode. If $V_{IN} > V_{IN\_SRC\_OV}$, the PWM is disabled and an OV fault asserts in the status and fault registers. The PWM recovers once V_{IN} drops below $V_{IN\_SRC\_OV}$ by a hysteresis (see the Electrical Characteristics section on page 12 for more details).

Short-Circuit Protection (SCP) in Source Mode

In addition to output OVP, the MP2561 features output short-circuit protection (SCP). When the load current reaches to the output current limit, V_{IN} begins to fall. If V_{IN} falls below $V_{IN\_SRC\_UV}$ for more than 10ms, a discharge fault asserts. Discharging is disabled for 30ms, then it restarts.

Battery Standby Mode

If only the battery is connected, the input source is absent, and the discharge function is disabled, the VCC LDO stays on. The device's maximum quiescent current (I_Q) is 35μA, which extends the batteries runtime.

Battery Under-Voltage Protection (UVP)

The MP2651 has two types of battery under-voltage protection (UVP). If $V_{BATT} < V_{BATT\_LOW}$ for 30ms in source mode, the MP2651 generates an INT signal to report that V_{BATT} is low, then source mode is stopped. The user can configure the source mode behavior via REG0Bh bit[11]. When REG0Bh bit[11] = 0, source mode restarts automatically when V_{BATT} exceeds 6.4V. When REG0Bh bit[11] = 1, source mode is latched, and the SRC-EN bit must be toggled to restart source mode.

SMBus and I²C Compatibility

The MP2651 has an SCL/SDA interface that is compatible with the SMBus/I²C interface. In addition, the MP2651's registers are 16 bits, which are compatible with both SMBus and I²C standards.

The system management bus (SMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

The MP2651 interface is an SMBus slave that supports both standard mode (100kHz) and fast mode (400kHz). The SMBus address is 0001 001x, where x is the read/write bit. The device receives control inputs from the master device, such as a microcontroller (MCU) or a digital signal processor.

Start and Stop Commands

All transactions begin with a start (S) command and are terminated by a stop (P) command. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 9).

Start and stop commands are always generated by the master. The bus is considered busy after a start command; it is considered free after a stop command.

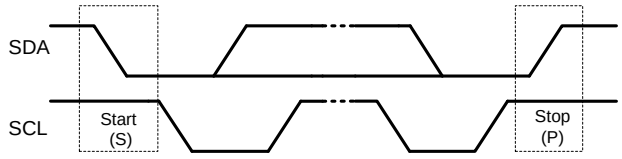


Figure 9: Start and Stop Commands

Data Validity

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 10).

When the bus is free, both lines are high. The SDA and SCL pins are open drains.

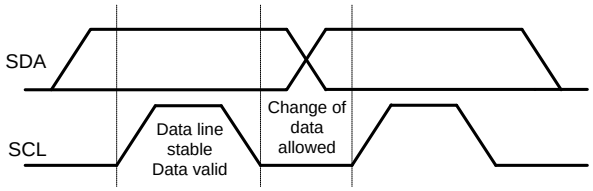


Figure 10: Data Validity

Interrupt to Host (INT)

The MP2651 has an alert mechanism that outputs an interrupt signal via the INT pin. If an interrupt is triggered, the device outputs a 256μs low-state INT pulse. The INT output is designed as open-drain structure that must be externally pulled up to a voltage source for operation. The INT signal can be masked via registers REG18h~19h.

Address Pin

To having multiple devices on the same I²C bus with the same address, the MP2651's address can be configured via the one-time programmable (OTP) memory.

To support multiple MP2651 devices on the same I²C/SMBUS lines, the device address can also be adjusted via the ADDR pin and the register.

The address is 7 bits long, followed by the 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 11 shows the address bit arrangement

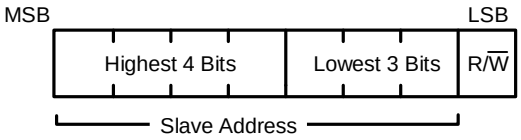


Figure 11: 7-Bit Address

The highest 4 bits of the address (REG05h, bits[6:3]) are configured via the OTP.

The lowest 3 bits of the address (REG05h, bits[2:0]) are configured using one of two methods. This is controlled by ADDR_CFG (REG05h, bit[7]). If REG05h, bit [7] =1, the lowest 3 bits are fixed to 001. If REG05h, bit [7] = 0, the ADDR pin configures the lowest 3 bits of the IC address. There is a 10μA current flowing out of the ADDR pin. Connect a resistor between the ADDR pin and AGND to set a different device address.

Table 4 shows the I²C/SMBus address for different ADDR resistor values. This address is 7 bits long, followed by the 8th data direction bit (R/W).

Table 4: Address Setting

R_{ADDR} (kΩ)	Slave Address
0Ω to 1kΩ	0001 000b
4.34kΩ to 5.87kΩ	0001 001b
9.35kΩ to 12.65kΩ	0001 010b
16.92kΩ to 22.89kΩ	0001 011b
Not recommended	0001 100b (reserved)
41.4kΩ to 56.01kΩ	0001 101b
59.33kΩ to 80.27kΩ	0001 110b
85kΩ to 115kΩ	0001 111b

SMBus Alert Response Address (ARA)

The SMBus alert response address (ARA) is a special address that can be used by the bus host.

If more than one slave-only device is connected on the bus, and all the INT lines are connected together, a slave-only device can signal to the host that it wants to talk through INT. The host processes the interrupt and simultaneously accesses all INT devices through the ARA. Only the device(s) that pull INT low acknowledge the ARA.

The host performs a modified receive byte operation. The 7-bit device address provided by the slave transmit device is placed in the 7 most significant bits of the byte. The 8th bit can be a 0 or 1.

The SMBus ARA is 0001 100b.

Byte Format

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first.

The acknowledgement takes place after every byte. The ACK bit allows the receiver to signal to the transmitter that the byte was successfully received, then another byte can be sent. All clock pulses, including the acknowledge pulse (9th clock pulse), are generated by the master (see Figure 12).

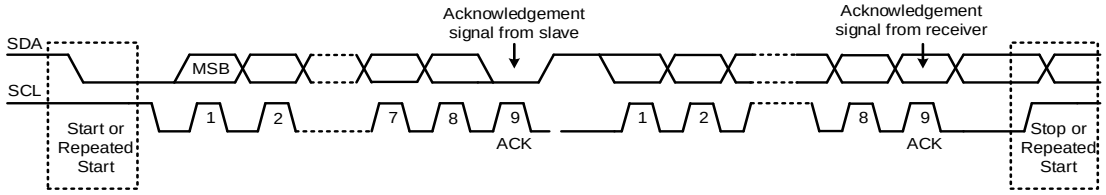


Figure 12: Acknowledge Bit

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. If the SDA line remains high during the 9th clock pulse, this is a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer or a repeated start command to start a transfer.

After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). If the register address is not defined, the charger IC sends back a NACK signal and returns to an idle state.

Figure 13, Figure 14, and Figure 15 show the complete data transfer.

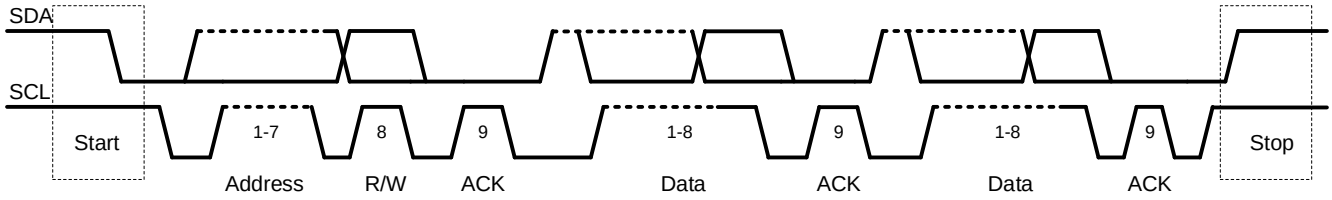


Figure 13: Byte Format

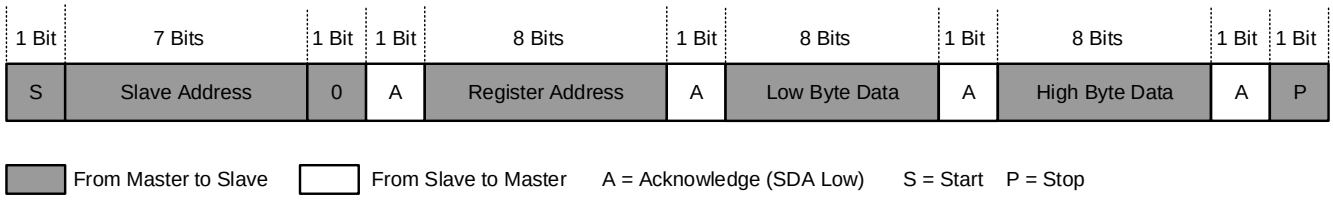


Figure 14: Singe-Word Write

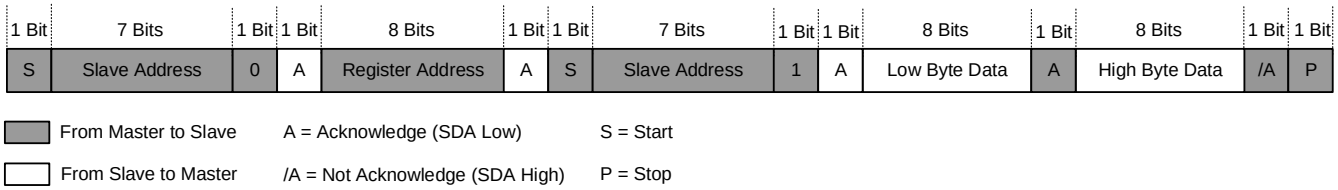


Figure 15: Single-Word Read

REGISTER MAP

Register Name	Register Address	OTP?	R/W	Description
REG05h	0x05	Yes	R/W	Device Address Setting
REG06h	0x06	Yes	R/W	Input Minimum Voltage Limit Setting
REG08h	0x08	Yes	R/W	Input Current Limit Setting
REG09h	0x09	No	R/W	Output Voltage Setting in Source Mode
REG0Ah	0x0A	No	R/W	Battery Impedance Compensation and Output Current Limit Setting in Source Mode
REG0Bh	0x0B	Yes	R/W	Battery Low Voltage Threshold and Battery Discharge Current Regulation in Source Mode
REG0Ch	0x0C	No	R/W	JEITA Action Setting
REG0Dh	0x0D	Yes	R/W	Temperature Protection Setting
REG0Eh	0x0E	Yes	R/W	Configuration Register 0
REG0Fh	0x0F	Yes	R/W	Configuration Register 1
REG10h	0x10	Yes	R/W	Configuration Register 2
REG11h	0x11	Yes	R/W	Configuration Register 3
REG12h	0x12	Yes	R/W	Configuration Register 4
REG14h	0x14	Yes	R/W	Charge Current Setting
REG15h	0x15	Yes	R/W	Battery Regulation Voltage Setting
REG16h	0x16	No	R	Status and Fault Register 0
REG17h	0x17	No	R	Status and Fault Register 1
REG18h	0x18	No	R/W	INT Mask Setting Register 0
REG19h	0x19	No	R/W	INT Mask Setting Register 1
REG22h	0x22	No	R	Internal DAC Output of the Input Current Limit Setting
REG23h	0x23	No	R	ADC Result of the Input Voltage
REG24h	0x24	No	R	ADC Result of the Input Current
REG25h	0x25	No	R	ADC Result of the Battery Voltage
REG27h	0x27	No	R	ADC Result of the Battery Current
REG28h	0x28	No	R	ADC Result of the NTC Voltage Ratio
REG29h	0x29	No	R	ADC Result of the TS Voltage Ratio
REG2Ah	0x2A	No	R	ADC Result of the Junction Temperature
REG2Bh	0x2B	No	R	ADC Result of the Battery Discharge Current
REG2Ch	0x2C	No	R	ADC Result of the Input Voltage in Discharge Mode
REG2Dh	0x2D	No	R	ADC Result of the Output Current in Discharge Mode

Notes:

7) The default device address is 08h due to the address pin connected to AGND. See the Address Pin section on page 28 to get the new device address if REG05h or the ADDR pin is modified.
8) OTP in this section means one-time programmable (OTP) memory.

REGISTER MAP

REG05h: Device Address Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comments
15:10	RESERVED	0	N/A	N/A	Reserved.	Reserved.
9	WD_SET	1	N	R/W	0: Disabled 1: Enabled	When this bit is set to 0, the watchdog timer is automatically disabled when V_{IN} is absent.
8	TLOW_EN	0	N	R	0: Disabled (I^2C) 1: Enabled (SMBus)	Default: 0 To be compliant with the SMBus, a 25ms timer is required to release SCL and SDA (reset the communication) if the timer expires. This bit can be configured via the OTP.
7	ADDR_CFG	0	N	R	0: The lower 3 bits of the IC address are determined by the ADDR pin 1: The lower 3 bits of the IC address are determined by the OTP	Default: 0 This bit determines how the device address is configured. This bit can be configured via the OTP.
6	ADDR[6]	0	N	R		Default: 0b0001 These bits determine the highest 4 bits of the device's address. These bits can be configurable via the OTP.
5	ADDR[5]	0	N	R		
4	ADDR[4]	0	N	R		
3	ADDR[3]	1	N	R		
2	ADDR[2]	0	N	R		If ADDR_CFG = 0, ADDR, bits[2:0] are set by the ADDR pin's resistor. If ADDR_CFG = 1, ADDR, bits[2:0] are fixed to 0b001.
1	ADDR[1]	0	N	R		
0	ADDR[0]	1	N	R		

REG06h: Input Minimum Voltage Limit Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:8	RESERVED	0	N/A	N/A	Reserved.	Reserved.
7	V_{IN_MIN}[6]	0	Y	R/W	10240mV.	Default: 4.56V Range: 0V to 20.4V These bits set the minimum V_{IN} limit. These bits can be configured via the OTP.
6	V_{IN_MIN}[6]	0	Y	R/W	5120mV.	
5	V_{IN_MIN}[5]	1	Y	R/W	2560mV.	
4	V_{IN_MIN}[4]	1	Y	R/W	1280mV.	
3	V_{IN_MIN}[3]	1	Y	R/W	640mV.	
2	V_{IN_MIN}[2]	0	Y	R/W	320mV.	
1	V_{IN_MIN}[1]	0	Y	R/W	160mV.	
0	V_{IN_MIN}[0]	1	Y	R/W	80mV.	

REG08h: Input Current Limit Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:7	RESERVED	0	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM}[6]	0	Y	R/W	3200mA.	Default: 500mA Range: 0A to 5A These bits set the I_{IN} limit. These bits can be configured via the OTP. Note that when RS1 changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] to keep the LSB unchanged.
5	I_{IN_LIM}[5]	0	Y	R/W	1600mA.	
4	I_{IN_LIM}[4]	0	Y	R/W	800mA.	
3	I_{IN_LIM}[3]	1	Y	R/W	400mA.	
2	I_{IN_LIM}[2]	0	Y	R/W	200mA.	
1	I_{IN_LIM}[1]	1	Y	R/W	100mA.	
0	I_{IN_LIM}[0]	0	Y	R/W	50mA.	

REG09h: Output Voltage Setting in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:12	RESERVED	0	N/A	R/W	Reserved.	Reserved.
11	$V_{IN\_SRC\_OS}$	0	N	R/W	0: 0V 1: 0.64V	Default: 0 When this bit is enabled, V_{IN_SRC} = DEC (bits[9:0]) + 0.64V
10	$V_{IN\_SRC\_CFG}$	0	N	R/W	0: Configured by the register bit 1: Configured by the FB pin	Default: 0 This bit determines the method of configuring V_{OUT} in source mode.
9	V_{IN_SRC}[9]	0	N	R/W	10240mV.	Default: 4.98V Range: 1V to 20.46V These bits set V_{OUT} in source mode.
8	V_{IN_SRC}[8]	0	N	R/W	5120mV.	
7	V_{IN_SRC}[7]	1	N	R/W	2560mV.	
6	V_{IN_SRC}[6]	1	N	R/W	1280mV.	
5	V_{IN_SRC}[5]	1	N	R/W	640mV.	
4	V_{IN_SRC}[4]	1	N	R/W	320mV.	
3	V_{IN_SRC}[3]	1	N	R/W	160mV.	
2	V_{IN_SRC}[2]	0	N	R/W	80mV.	
1	V_{IN_SRC}[1]	0	N	R/W	40mV.	
0	V_{IN_SRC}[0]	1	N	R/W	20mV.	

REG0Ah: Battery Impedance Compensation and Output Current Limit Setting in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	RESERVED	0	N/A	N/A	Reserved.	Reserved.
13	BATTR[2]	0	Y	R/W	200mΩ/cell.	Default: 0mΩ Range: 0mΩ to 350mΩ These bits input the predicted battery internal impedance and cable impedance.
12	BATTR[1]	0	Y	R/W	100mΩ/cell.	
11	BATTR[0]	0	Y	R/W	50mΩ/cell.	
10	V_{CLAMP}[2]	0	Y	R/W	240mV/cell.	Default: 0mV/cell Range: 0mV/cell to 420mV/cell These bits set the maximum compensation voltage, which should be added to original battery-full regulation voltage if the IR compensation function is used.
9	V_{CLAMP}[1]	0	Y	R/W	120mV/cell.	
8	V_{CLAMP}[0]	0	Y	R/W	60mV/cell.	
7	RESERVED	0	NA	NA	Reserved.	Reserved.
6	I_{IN_SRC}[6]	0	Y	R/W	3200mA.	Default: 2A Range: 0A to 5.5A These bits set the I_{OUT} limit in source mode. Note that when RS1 changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] to keep the LSB unchanged.
5	I_{IN_SRC}[5]	1	Y	R/W	1600mA.	
4	I_{IN_SRC}[4]	0	Y	R/W	800mA.	
3	I_{IN_SRC}[3]	1	Y	R/W	400mA.	
2	I_{IN_SRC}[2]	0	Y	R/W	200mA.	
1	I_{IN_SRC}[1]	0	Y	R/W	100mA.	
0	I_{IN_SRC}[0]	0	Y	R/W	50mA.	

REG0Bh: Battery Low Voltage Setting and Battery Discharge Current Regulation in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:14	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
13	V_{BATT_LOW}_EN	1	Y	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables the battery low-voltage protection. This bit can be configured via the OTP.
12	V_{BATT_PRE}	1	N	R/W	0: 2.5V/cell 1: 3V/cell	Default: 1 This bit sets the pre-charge to CC charge threshold.
11	BATTLOW_ ACT	0	Y	R/W	0: Only generate INT 1: Generate INT and latch off the DC/DC converter	Default: 0 This bit determines the behavior of battery low voltage protection when REG0Bh, bit[13] is set to 1. When V_{BATT} < V_{BATT_LOW} which is set via REG0Bh, bits[10:9]. INT is asserts and the DC/DC converter can also be latched off optionally. This bit can be configured via the OTP. Note that charging the battery or toggling the SRC_EN bit clears the DSCHG_FLT bit. Then the source can be enabled again. When source mode is disabled, the BATTLOW comparator does not operate.
10	V_{BATT_LOW}[1]	0	N	R/W	00: 3V/cell 01: 3.1V/cell 10: 3.2V/cell 11: 3.3V/cell	Default: 00 These bits set the low battery voltage threshold for battery low-voltage protection.
9	V_{BATT_LOW}[0]	0	N	R/W		
8	I_{BATT_DSCHG}EN	0	N	R/W	0: Disabled 1: Enabled	Default: 0 This bit enables battery discharge current regulation in source mode.
7	I_{BATT_DSCHG}[7]	1	N	R/W	6400mA.	Default: 6.4A Range: 0A to 12.75A These bits set the battery discharge current in source mode.
6	I_{BATT_DSCHG}[6]	0	N	R/W	3200mA.	
5	I_{BATT_DSCHG}[5]	0	N	R/W	1600mA.	
4	I_{BATT_DSCHG}[4]	0	N	R/W	800mA.	
3	I_{BATT_DSCHG}[3]	0	N	R/W	400mA.	
2	I_{BATT_DSCHG}[2]	0	N	R/W	200mA.	
1	I_{BATT_DSCHG}[1]	0	N	R/W	100mA.	
0	I_{BATT_DSCHG}[0]	0	N	R/W	50mA.	

REG0Ch: JEITA Action Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	WARM_ACT[1]	0	Y	R/W	00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}	These bits determine the device's behavior if NTC warm protection occurs.
13	WARM_ACT[0]	1	Y	R/W		
12	COOL_ACT[1]	1	Y	R/W	00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC} when NTC cool	These bits determine the device's behavior if NTC cool protection occurs.
11	COOL_ACT[0]	0	Y	R/W		
10	JEITA_VSET[4]	1	Y	R/W	320mV/cell.	Default: 320mV/cell Range: (0mv to 620mv)/cell with 20mv/cell per step These bits set the decrement value for the battery-full voltage if NTC cool or warm protection occurs. The battery-full voltage can be set via REG15h.
9	JEITA_VSET[3]	0	Y	R/W	160mV/cell.	
8	JEITA_VSET[2]	0	Y	R/W	80mV/cell.	
7	JEITA_VSET[1]	0	Y	R/W	40mV/cell.	
6	JEITA_VSET[0]	0	Y	R/W	20mV/cell.	
5	JEITA_ISET[1]	0	Y	R/W	00: 1/2 times 01: 1/4 times 10: 1/8 times 11: 1/16 times	Default: 01 These bits set the scaling value of the constant current (CC) charge current. The CC charge current can be set via REG14h.
4	JEITA_ISET[0]	1	Y	R/W		
3:0	RESERVED	0	N/A	N/A	Reserved.	Reserved.

REG0Dh: Temperature Protection Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	TS_EN	1	N	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables the external temperature-sense function.
14	RESERVED	0	N/A	N/A	Reserved.	Do not change this bit's value.
13	TS_ACT	1	Y	R/W	0: Only deliver INT when the TS threshold is reached 1: Deliver INT and take TS action	Default: 1 This bit determine the device's behavior if TS over-temperature protection (OTP) occurs. An INT asserts after TS OTP occurs, and an additional I_{IN} regulation can be taken optionally. This bit can be configured via the OTP.
12	V_{TS_HOT}[2]	1	N	R/W	000: 9% (100°C) 001: 10% (95°C) 010: 11.3% (90°C) 011: 12.7% (85°C) 100: 14.3% (80°C) 101: 16.1% (75°C) 110: 18.2% (70°C) 111: 20.6% (65°C)	Default: 100 These bits set the TS over-temperature (OT) threshold, which is a percentage of VNTC. Assume the thermistor is 103AT, with a 10kΩ pull-up resistor.
11	V_{TS_HOT}[1]	0	N	R/W		
10	V_{TS_HOT}[0]	0	N	R/W		
9	NTC_EN	1	N	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables NTC protection.
8	NTC_ACT	1	N	R/W	0: Only deliver INT when the NTC threshold is reached 1: Deliver INT and take JEITA action	Default: 1 This bit determines the device's behavior if NTC protection occurs. An INT asserts when NTC protection and additional actions can be taken optionally. It can be configured via the OTP.
7	V_{HOT}[1]	1	N	R/W	00: 29.1% (50°C) 01: 25.9% (55°C) 10: 23% (60°C) 11: 20.4% (65°C)	Default: 10 These bits set the NTC hot temperature threshold, which is as a percentage of V_{NTC}. Assume the thermistor is 103AT.
6	V_{HOT}[0]	0	N	R/W		
5	V_{WARM}[1]	0	N	R/W	00: 36.5% (40°C) 01: 32.6% (45°C) 10: 29.1% (50°C) 11: 25.9% (55°C)	Default: 01 These bits set the NTC warm temperature threshold, which is as a percentage of V_{NTC}. Assume the thermistor is 103AT.
4	V_{WARM}[0]	1	N	R/W		
3	V_{COOL}[1]	1	N	R/W	00: 74.2% (0°C) 01: 69.6% (5°C) 10: 64.8% (10°C) 11: 59.9% (15°C)	Default: 10 These bits set the NTC cool temperature threshold, which is as a percentage of V_{NTC}. Assume the thermistor is 103AT.
2	V_{COOL}[0]	0	N	R/W		
1	V_{COLD}[1]	0	N	R/W	00: 78.4% (-5°C) 01: 74.2% (0°C) 10: 69.6% (+5°C) 11: 64.8% (+10°C)	Default: 01 These bits set the NTC cold temperature threshold, which is as a percentage of V_{NTC}. Assume the thermistor is 103AT.
0	V_{COLD}[0]	1	N	R/W		

REG0Eh: Configuration Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:9	RESERVED	0	N/A	N/A	Reserved.	Reserved.
8	ADC_START	0	N	R/W	0: Disable ADC 1: Enable ADC	This bit enables the analog-to-digital converter (ADC) when it is set to one-shot conversion mode via REG0Eh, bit[7]. This bit returns to 0 after conversion is complete. When the DC/DC converter is enabled, this bit is set to 1 to enable the ADC. This bit is read-only when ADC_CONV = 1. The bit stays high during ADC conversion.
7	ADC_CONV	0	N	R/W	0: One-shot conversion 1: Continuous conversion	This bit determines the behavior of ADC conversion.
6	SW_FREQ[2]	0	Y	R/W	000: 500kHz 001: 600kHz 010: 700kHz 011: 800kHz 100: 750kHz 101: 900kHz 110: 1000kHz 111: 1200kHz	Default: 600kHz These bits set the buck-boost converter's switching frequency. These bits can be configured via the OTP.
5	SW_FREQ[1]	0	Y	R/W		
4	SW_FREQ[0]	1	Y	R/W		
3:0	RESERVED	0	NA	NA	Reserved.	Do not change the value of these bits.

REG0Fh: Configuration Register 1

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	TJ_REG EN	1	Y	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables junction temperature OT regulation. This bit can be configured via the OTP.
14	T_{J_REG}[2]	1	Y	R/W	000: 80°C 001: 90°C 010: 95°C 011: 100°C 100: 105°C 101: 110°C 110: 115°C 111: 120°C	Default: 111 These bits set the junction temperature regulation point.
13	T_{J_REG}[1]	1	Y	R/W		
12	T_{J_REG}[0]	1	Y	R/W		
11	I_{TC}[3]	0	Y	R/W	400mA.	Default: 100mA Range: 0mA to 750mA These bits set the trickle-charge current. These bits can be configured via the OTP.
10	I_{TC}[2]	0	Y	R/W	200mA.	
9	I_{TC}[1]	1	Y	R/W	100mA.	
8	I_{TC}[0]	0	Y	R/W	50mA.	
7	I_{PRE}[7]	0	Y	R/W	800mA.	Default: 400mA Range: 0mA to 1500mA These bits set the pre-charge current. These bits can be configured via the OTP.
6	I_{PRE}[6]	1	Y	R/W	400mA.	
5	I_{PRE}[5]	0	Y	R/W	200mA.	
4	I_{PRE}[4]	0	Y	R/W	100mA.	
3	I_{TERM}[3]	0	Y	R/W	400mA.	Default: 200mA Range: 0mA to 750mA These bits set the termination current. These bits can be configured via the OTP.
2	I_{TERM}[2]	1	Y	R/W	200mA.	
1	I_{TERM}[1]	0	Y	R/W	100mA.	
0	I_{TERM}[0]	0	Y	R/W	50mA.	

REG10h: Configuration Register 2

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	ACGATE_ CTRL	0	N	R/W	0: Not force ACGATE on 1: Force ACGATE on	Default: 0 This bit controls the ACGATE. It can force ACGATE to turn on external MOSFET when it is set to 1. The ACGATE state depends on the ADP voltage.
13	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.
12	TS/IMON	0	Y	R/W	0: TS/IMON pin acts as TS 1: TS/IMON pin acts as IMON	This bit configures the function of the TS/IMON. It is configured to TS function by default. This bit can be configured via the OTP.
11	VRECH	1	N	R/W	0: -100mV/cell 1: -200mV/cell	Default: 1 This bit sets the automatic recharge threshold, which is compared to battery-full voltage. This bit can be configured via the OTP.
10	BAT_NUM[1]	0	N	R/W	00: 1 cell 01: 2 cell 10: 3 cell 11: 4 cell	Default: 01 This bit sets the battery cells in series. This bit can be configured via the OTP.
9	BAT_NUM[0]	1	N	R/W		
8	IN_RSNS	0	N	R/W	0: 10mΩ 1: 5mΩ	This bit sets the I_{IN} sense gain. It should be set according to external sense resistor (RS1). It assumes a 10mΩ sense FET is used by default. This bit can be configured via the OTP.
7	IBATT_RSNS	0	N	R/W	0: 10mΩ 1: 5mΩ	This bit sets the battery current sense gain. It should be set according to external sense resistor (RS2). It assumes 10mΩ sense FET is used as default. This bit can be configured via the OTP.
6	ACGATE_EN	1	N	R/W	0: Disable the ACGAET driver (External ACFET will be off mandatorily) 1: Enable the ACGATE driver	Default: Enabled This bit is used to enable ACGATE driver.
5	RESERVED	0	N/A	N//A	Reserved.	Do not change the values of these bits.
4	RESERVED	0	N/A	N/A	Reserved.	
3	RESERVED	0	N/A	N/A	Reserved.	
2	RESERVED	0	N/A	N/A	Reserved.	
1	RESERVED	0	N/A	N/A	Reserved.	

0	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.

REG11h: Configuration Register 3

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	$V_{IN\_SRC\_OV}$[1]	1	N	R/W	00: 106% 01: 120% 10: 115% 11: 110%	Default: 11 These bits set the over-voltage (OV) threshold for the source V_{OUT}.
13	$V_{IN\_SRC\_OV}$[0]	1	N	R/W		
12	$V_{IN\_SRC\_UV}$[1]	0	N	R/W	00: 75% 01: 80% 10: 85% 11: 30%	Default: 00 These bits set the under-voltage (UV) threshold for the source V_{OUT}.
11	$V_{IN\_SRC\_UV}$[0]	0	N	R/W		
10	VIN_OVP_DGL	0	N	R/W	0: 1µs 1: 15ms	Default: 0 This bit sets the deglitch time for input over-voltage protection (OVP) in charge mode.
9	V_{IN_UVP}[1]	0	N	R/W	00: 3.2V 01: 6.4V 10: 12V 11: 16.8V	Default: 00 These bits set the input under-voltage protection (UVP) threshold. These bits can be configured via the OTP.
8	V_{IN_UVP}[0]	0	N	R/W		
7	V_{IN_OVP}[1]	1	N	R/W	00: 7.2V 01: 11.2V 10: 17.6V 11: 22.4V	Default: 11 These bits are used to set the input OVP threshold. These bits can be configured via the OTP.
6	V_{IN_OVP}[0]	1	N	R/W		
5	RESERVED	1	N/A	N/A	Reserved.	Do not change the value of this bit.
4	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.
3	BATTOVP_EN	1	N	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables battery OVP.
2	RESERVED	0	N/A	R/W	Reserved.	Do not change the value of this bit.
1	RESERVED	0	N/A	R/W	Reserved.	Do not change the value of this bit.
0	RESERVED	0	N/A	R/W	Reserved.	Do not change the value of this bit.

REG12h: Configuration Register 4

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.
14	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.
13	TMR_EN	1	Y	R/W	0: Disabled 1: Enabled	This bit enables the charging safety timer (both the trickle/pre-charge timer and CC/CV charge timer). It is set to 1 by default. This bit can be configured via the OTP.
12	CHG_TMR[1]	1	Y	R/W	00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours	Default: 11 These bits set the CC/CV timer.
11	CHG_TMR[0]	1	Y	R/W		
10	TMR2X_EN	1	Y	R/W	0: The safety timer is not doubled during input DPM or thermal regulation 1: The safety timer is doubled during input DMP and thermal regulation	Default: 1 This bit sets the safety timer during DPM and thermal regulation.
9	WTD_RST	0	Y	R/W	0: Normal 1: Reset	Default: 0 This bit resets the I^2C watchdog timer. It returns to 0 after it is reset.
8	WTD[1]	0	Y	R/W	00: Disable timer 01: 40s 10: 80s 11: 175s	Default: 00 This bit sets the I^2C watchdog timer. These bits can be configured via the OTP.
7	WTD[0]	0	Y	R/W		
6	DC/DC_EN	1	Y	R/W	0: Disabled 1: Enabled	Default: 1 This bit enables the DC/DC converter. This bit can be configured via the OTP.
5	RESERVED	0	N/A	N/A	Reserved.	Do not change the value of this bit.
4	TERM_EN	1	Y	R/W	0: Disabled 1: Enabled	This bit enables charge termination. It is set to 1 by default via the OTP.
3	SRC_EN	0	Y	R/W	0: Disable source mode 1: Enable source mode	Default: 0 This bit enables source mode configuration. SRC_EN can override the charge enable function.
2	REG_RST	0	Y	R/W	0: Keep current register setting 1: Reset to default register value and reset safety timer	Default: 0 This bit sets the register reset setting. It resets to 0 after the register is reset.
1	IINLIM_EN	1	Y	R/W	0: IIN_LIM disabled 1: IIN_LIM enabled	Default: 1 This bit enables the I_{IN} limit loop.

0	CHG_EN	1	Y	R/W	0: Charge disabled 1: Charge enabled	Default: 1 This bit configures the charge mode. SRC_EN overrides the CHG_EN enable function. It can be configured via the OTP.

REG14h: Charge Current Setting

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
15:14	RESERVED	0	NA	NA	Reserved.	Reserved.
13	I_{CC}[7]	0	Y	R/W	6400mA.	Default: 2A Range: 0A to 6A Offset: 0A These bits set the charge current. These bits can be configured via the OTP.
12	I_{CC}[6]	0	Y	R/W	3200mA.	
11	I_{CC}[5]	1	Y	R/W	1600mA.	
10	I_{CC}[4]	0	Y	R/W	800mA.	
9	I_{CC}[3]	1	Y	R/W	400mA.	
8	I_{CC}[2]	0	Y	R/W	200mA.	
7	I_{CC}[1]	0	Y	R/W	100mA.	
6	I_{CC}[0]	0	Y	R/W	50mA.	
5:0	RESERVED	0	N/A	N/A	Reserved.	Reserved.

REG15h: Battery Regulation Voltage Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	V_{BATT_REG}[10]	0	Y	R/W	10240mV.	Default: 8.4V (absolute voltage) Range: 3.4V/cell to 4.67V/cell for different cell counts These bits set the charge-full voltage. These bits can be configured via the OTP. The minimum charge-full voltage setting step is the cell number multiplied by 10mv:
13	V_{BATT_REG}[9]	1	Y	R/W	5120mV.	
12	V_{BATT_REG}[8]	1	Y	R/W	2560mV.	
11	V_{BATT_REG}[7]	0	Y	R/W	1280mV.	
10	V_{BATT_REG}[6]	1	Y	R/W	640mV.	
9	V_{BATT_REG}[5]	0	Y	R/W	320mV.	
8	V_{BATT_REG}[4]	0	Y	R/W	160mV.	
7	V_{BATT_REG}[3]	1	Y	R/W	80mV.	
6	V_{BATT_REG}[2]	0	Y	R/W	40mV.	
5	V_{BATT_REG}[1]	0	Y	R/W	20mV.	
4	V_{BATT_REG}[0]	0	Y	R/W	10mV.	
3:0	RESERVED	0	N/A	R/W	Reserved.	Reserved.

REG16h: Status and Fault Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	MD_STAT[1]	0	N	R	00: Shipping mode 01/11: Operation mode 10: Standby mode	These bits indicate the DC/DC converter's operation status. These bits assert INT when the state changes.
14	MD_STAT[0]	0	N	R		
13	PG_STAT	0	N	R	0: V_{IN} not PG 1: V_{IN} PG	Default: 0 This bit indicates the power good (PG) status. It asserts INT when this bit changes from 0 to 1.
12	SWITCH_STAT[1]	0	N	R	00: Idle 01: Buck 10: Buck-boost 11: Boost	Default: 00 These bits indicate the DC/DC converter's operation mode.
11	SWITCH_STAT[0]	0	N	R		
10	BATT_MISS_ STAT	0	N	R	0: Normal 1: Battery missing	Default: 0 This bit indicates whether the battery is missing.
9	RESERVED	0	N/A	N/A	Reserved.	Reserved.
8	CHG_STAT[2]	0	N	R	000: No charging 001: Trickle charge 010: Pre-charge 011: CC charge 100: CV charge 101: Charge termination	Default: 000 These bits indicate the charging status. These bits assert INT when the state changes.
7	CHG_STAT[1]	0	N	R		
6	CHG_STAT [0]	0	N	R		
5	VIN_MIN_STAT	0	N	R	0: Not in V_{IN} limit 1: In V_{IN} limit	Default: 0 This bit indicates whether the IC stays in the V_{IN} loop. It asserts INT when this bit changes from 0 to 1.
4	IIN_LIM_STAT	0	N	R	0: Not in I_{IN} limit 1: In I_{IN} limit	Default: 0 This bit indicates whether the IC stays in the I_{IN} loop. It asserts INT when this bit changes from 0 to 1.
3	RESERVED	0	N/A	N/A	Reserved	Reserved
2	RESERVED	0	N/A	N/A	Reserved.	Reserved
1	TS_FAULT	0	N	R	0: Normal 1: A TS fault has occurred	This bit indicates whether a TS-related fault occurs. It asserts INT when a fault occurs.
0	RESERVED	0	N/A	N/A	Reserved.	Reserved.

REG17h: Status and Fault Register 1

Bits	Name	Default	Reset by WTD	R/W	Description		Comment
15	VIN_ SRC_OV	0	N	R	0: Normal operation 1: OVP has occurred in source mode.		This bit indicates whether output over-voltage protection (OVP) occurs in source mode. It asserts INT if a fault occurs.
14	VIN_ SRC_UV	0	N	R	0: Normal operation 1: UVP has occurred source mode		This bit indicates whether output under-voltage protection (UVP) occurs in source mode. It asserts INT if a fault occurs.
13	VIN_OV	0	N	R	0: Normal operation 1: Input OVP has occurred in charge mode		This bit indicates whether output OVP occurs in charge mode. It asserts INT if a fault occurs.
12	VADP_OV	0	N	R	0: Normal operation 1: VADP OVP has occurred in charge mode		This bit indicates whether ADP OVP occurs in charge mode. It asserts INT if a fault occurs.
11	RESERVED	0	N/A	N/A	Reserved.		Reserved.
10	RESERVED	0	N/A	N/A	Reserved.		Reserved.
9	RESERVED	0	N/A	N/A	Reserved.		Reserved.
8	VBATT_OV	0	N	R	0: Normal operation 1: Battery OVP has occurred		This bit indicates whether battery OVP occurs in charge mode. It asserts INT if a fault occurs.
7	VBATT_ LOW	0	N	R	0: Normal 1: Discharging has stopped due to low battery voltage		This bit indicates whether there is a low battery voltage in source mode. It asserts INT if a fault occurs.
6	WTD_EXP	0	N	R	0: Normal operation 1: The watchdog timer has expired		This bit indicates whether the watchdog timer has expired.
5	CHG_ TMR_EXP	0	N	R	0: Normal operation 1: The charge Safety timer has expired		This bit indicates whether the charge safety timer has expired. It asserts INT if a fault occurs.
4	THERM_ SHDN	0	N	R	0: Normal operation 1: Thermal shutdown has occurred		This bit indicates whether thermal shutdown occurs. It asserts INT if a fault occurs.
3	RESERVED	0	NA	R/W	Reserved.		Reserved.
2	NTC_ FAULT[2]	0	N	R	Charge mode: 000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot 111: NTC float	Source mode: 000: Normal 001: NTC cold 100: NTC hot 111: NTC float	These bits indicate whether an NTC fault occurs in charge mode or source mode. These bits assert INT if a fault occurs.
1	NTC_ FAULT[1]	0	N	R			
0	NTC_ FAULT[0]	0	N	R			

REG18h: INT Mask Setting Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	RESERVED	0	N/A	N/A	Reserved.	Reserved.
13	VIN_SRC_ FAULT	0	Y	R/W	0: Masked 1: Not masked	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set.
12	VIN_OV_ FAULT	0	Y	R/W	0: Masked 1: Not masked	
11	PG_STAT	0	Y	R/W	0: Masked 1: Not masked	
10	BATT_OV_F AULT	0	Y	R/W	0: Masked 1: Not masked	
9	RESERVED	0	N/A	N/A	Reserved.	Reserved.
8	RESERVED	0	N/A	N/A	Reserved	Reserved
7	BATT_LOW_ FAULT	0	Y	R/W	0: Masked 1: Not masked	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set.
6	BATT_ MISS_STAT	0	Y	R/W	0: Masked 1: Not masked	
5	THERM_ SHDN	0	Y	R/W	0: Masked 1: Not masked	
4	TS_FAULT	0	Y	R/W	0: Masked 1: Not masked	
3	NTC_FAULT	0	Y	R/W	0: Masked 1: Not masked	
2	CHG_TMR_ FAULT	0	Y	R/W	0: Masked 1: Not masked	
1	MD_STAT	0	Y	R/W	0: Masked 1: Not masked	
0	CHG_STAT	0	Y	R/W	0: Masked 1: Not masked	

REG19h: INT Mask Setting Register 1

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:3	RESERVED	0	NA	NA	Reserved.	Reserved.
2	RESERVED	0	Y	R/W	Reserved.	Reserved.
1	VIN_MIN_ STAT	0	Y	R/W	0: Masked 1: Not masked	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set.
0	IIN_LIM_STAT	0	Y	R/W	0: Masked 1: Not masked	

REG22h: Internal DAC Output of the Input Current Limit

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:7	RESERVED	0	NA	NA	Reserved.	Reserved.
6	I_{IN_DPM}[6]	0	N	R	3200mA.	These bits only indicate the real I_{IN} limit value, which is read-only.
5	I_{IN_DPM}[5]	0	N	R	1600mA.	
4	I_{IN_DPM}[4]	0	N	R	800mA.	
3	I_{IN_DPM}[3]	0	N	R	400mA.	
2	I_{IN_DPM}[2]	0	N	R	200mA.	
1	I_{IN_DPM}[1]	0	N	R	100mA.	
0	I_{IN_DPM}[0]	0	N	R	50mA.	

REG23h: ADC Result of the Input Voltage

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{IN}[9]	N/A	N/A	R	10240mV.	These bits indicate the ADC V_{IN} conversion .
8	V_{IN}[8]	N/A	N/A	R	5120mV.	
7	V_{IN}[7]	N/A	N/A	R	2560mV.	
6	V_{IN}[6]	N/A	N/A	R	1280mV.	
5	V_{IN}[5]	N/A	N/A	R	640mV.	
4	V_{IN}[4]	N/A	N/A	R	320mV.	
3	V_{IN}[3]	N/A	N/A	R	160mV.	
2	V_{IN}[2]	N/A	N/A	R	80mV.	
1	V_{IN}[1]	N/A	N/A	R	40mV.	
0	V_{IN}[0]	N/A	N/A	R	20mV.	

REG24h: ADC Result of the Input Current

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{IN}[9]	N/A	N/A	R	3200mA.	These bits indicate the ADC I_{IN} conversion.
8	I_{IN}[8]	N/A	N/A	R	1600mA.	
7	I_{IN}[7]	N/A	N/A	R	800mA.	
6	I_{IN}[6]	N/A	N/A	R	400mA.	
5	I_{IN}[5]	N/A	N/A	R	200mA.	
4	I_{IN}[4]	N/A	N/A	R	100mA.	
3	I_{IN}[3]	N/A	N/A	R	50mA.	
2	I_{IN}[2]	N/A	N/A	R	25mA.	
1	I_{IN}[1]	N/A	N/A	R	12.5mA.	
0	I_{IN}[0]	N/A	N/A	R	6.25mA.	

REG25h: ADC Result of the Battery Voltage per Cell

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{BATT}[9]	N/A	N/A	R	2560mV/cell.	These bits indicate the ADC conversion of the battery voltage per cell. The real battery voltage should be the value read times the number of cells.
8	V_{BATT}[8]	N/A	N/A	R	1280mV/cell.	
7	V_{BATT}[7]	N/A	N/A	R	640mV/cell.	
6	V_{BATT}[6]	N/A	N/A	R	320mV/cell.	
5	V_{BATT}[5]	N/A	N/A	R	160mV/cell.	
4	V_{BATT}[4]	N/A	N/A	R	80mV/cell.	
3	V_{BATT}[3]	N/A	N/A	R	40mV/cell.	
2	V_{BATT}[2]	N/A	N/A	R	20mV/cell.	
1	V_{BATT}[1]	N/A	N/A	R	10mV/cell.	
0	V_{BATT}[0]	N/A	N/A	R	5mV/cell.	

REG27h: ADC Result of the Battery Charge Current

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{BATT}[9]	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of the charge current times the external 10mΩ sense resistor.
8	I_{BATT}[8]	N/A	N/A	R	3200mA.	
7	I_{BATT}[7]	N/A	N/A	R	1600mA.	
6	I_{BATT}[6]	N/A	N/A	R	800mA.	
5	I_{BATT}[5]	N/A	N/A	R	400mA.	
4	I_{BATT}[4]	N/A	N/A	R	200mA.	
3	I_{BATT}[3]	N/A	N/A	R	100mA.	
2	I_{BATT}[2]	N/A	N/A	R	50mA.	
1	I_{BATT}[1]	N/A	N/A	R	25mA.	
0	I_{BATT}[0]	N/A	N/A	R	12.5mA.	

REG28h: ADC Result of the NTC Sense Ratio

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	NTC[9]	N/A	N/A	R	512/1024.	These bits indicate the ADC conversion of the NTC voltage, as a percentage of V_{NTC}. The real battery temperature can be recalculated according to the external divider and thermistor datasheet.
8	NTC[8]	N/A	N/A	R	256/1024.	
7	NTC[7]	N/A	N/A	R	128/1024.	
6	NTC[6]	N/A	N/A	R	64/1024.	
5	NTC[5]	N/A	N/A	R	32/1024.	
4	NTC[4]	N/A	N/A	R	16/1024.	
3	NTC[3]	N/A	N/A	R	8/1024.	
2	NTC[2]	N/A	N/A	R	4/1024.	
1	NTC[1]	N/A	N/A	R	2/1024.	
0	NTC[0]	N/A	N/A	R	1/1024.	

REG29h: ADC Result of the TS Sense Ratio

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:8	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	TS[9]	N/A	N/A	R	512/1024.	These bits indicate the ADC conversion of TS voltage, as a percentage of V_{NTC}.
8	TS[8]	N/A	N/A	R	256/1024.	
7	TS[7]	N/A	N/A	R	128/1024.	
6	TS[6]	N/A	N/A	R	64/1024.	
5	TS[5]	N/A	N/A	R	32/1024.	
4	TS[4]	N/A	N/A	R	16/1024.	
3	TS[3]	N/A	N/A	R	8/1024.	
2	TS[2]	N/A	N/A	R	4/1024.	
1	TS[1]	N/A	N/A	R	2/1024.	
0	TS[0]	N/A	N/A	R	1/1024.	

REG2Ah: ADC Result of the Junction Temperature

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	TJ[9]	N/A	N/A	R	512.	These bits indicate the ADC conversion of the junction temperature, calculated with the following equation: $T_J = 314 - 0.5703 \times bits[9:0]$
8	TJ[8]	N/A	N/A	R	256.	
7	TJ[7]	N/A	N/A	R	128.	
6	TJ[6]	N/A	N/A	R	64.	
5	TJ[5]	N/A	N/A	R	32.	
4	TJ[4]	N/A	N/A	R	16.	
3	TJ[3]	N/A	N/A	R	8.	
2	TJ[2]	N/A	N/A	R	4.	
1	TJ[1]	N/A	N/A	R	2.	
0	TJ[0]	N/A	N/A	R	1.	

REG2Bh: ADC Result of the Battery Discharge Current

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:8	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{BATT_DIS}[9]	N/A	N/A	R	6400mA.	These bits indicate the ADC conversion of the battery discharge charge current.
8	I_{BATT_DIS}[8]	N/A	N/A	R	3200mA.	
7	I_{BATT_DIS}[7]	N/A	N/A	R	1600mA.	
6	I_{BATT_DIS}[6]	N/A	N/A	R	800mA.	
5	I_{BATT_DIS}[5]	N/A	N/A	R	400mA.	
4	I_{BATT_DIS}[4]	N/A	N/A	R	200mA.	
3	I_{BATT_DIS}[3]	N/A	N/A	R	100mA.	
2	I_{BATT_DIS}[2]	N/A	N/A	R	50mA.	
1	I_{BATT_DIS}[1]	N/A	N/A	R	25mA.	
0	I_{BATT_DIS}[0]	N/A	N/A	R	12.5mA.	

REG2Ch: ADC Result of the Input Voltage in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:10	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{IN_SRC}[9]	N/A	N/A	R	10240mV.	These bits indicate the ADC V_{OUT} conversion at the IN pin in source mode.
8	V_{IN_SRC}[8]	N/A	N/A	R	5120mV.	
7	V_{IN_SRC}[7]	N/A	N/A	R	2560mV.	
6	V_{IN_SRC}[6]	N/A	N/A	R	1280mV.	
5	V_{IN_SRC}[5]	N/A	N/A	R	640mV.	
4	V_{IN_SRC}[4]	N/A	N/A	R	320mV.	
3	V_{IN_SRC}[3]	N/A	N/A	R	160mV.	
2	V_{IN_SRC}[2]	N/A	N/A	R	80mV.	
1	V_{IN_SRC}[1]	N/A	N/A	R	40mV.	
0	V_{IN_SRC}[0]	N/A	N/A	R	20mV.	

REG2Dh: ADC Result of the Output Current in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15:8	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{IN_SRC}[9]	N/A	N/A	R	3200mA.	These bits indicate the ADC I_{OUT} conversion in source mode.
8	I_{IN_SRC}[8]	N/A	N/A	R	1600mA.	
7	I_{IN_SRC}[7]	N/A	N/A	R	800mA.	
6	I_{IN_SRC}[6]	N/A	N/A	R	400mA.	
5	I_{IN_SRC}[5]	N/A	N/A	R	200mA.	
4	I_{IN_SRC}[4]	N/A	N/A	R	100mA.	
3	I_{IN_SRC}[3]	N/A	N/A	R	50mA.	
2	I_{IN_SRC}[2]	N/A	N/A	R	25mA.	
1	I_{IN_SRC}[1]	N/A	N/A	R	12.5mA.	
0	I_{IN_SRC}[0]	N/A	N/A	R	6.25mA.	

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. I_{IN} is discontinuous in buck mode. The RMS ripple current (I_{CIN_RMS}) of the input capacitor can be calculated with Equation (3):

$$I_{CIN\_RMS} = I_{CHG} x \frac{\sqrt{V_{BATT} x (V_{IN} - V_{BATT})}}{V_{IN}} \quad (3)$$

The worst-case RMS ripple current occurs at a 50% duty cycle. Typically, V_{BATT} is between 6V and 9V for a 2-cell battery configuration, which means the worst-case condition occurs when the input is between 12V and 20V.

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended for the input decoupling capacitor. These capacitors should be placed as close as possible to the IN and PGND pins, and their voltage rating must exceed the normal V_{IN} level. A capacitor with a minimum 25V voltage rating is recommended for up to a 20V V_{IN}. It is recommended to use 1 x 1µF and 5 x 10µF capacitors for up to a 3A I_{IN} limit.

Ceramic capacitors show a DC bias effect that reduces the charger's effective capacitance. This effect may lead to a significant capacitance drop, especially at higher input voltages with small capacitor packages. Choose a higher voltage rating or nominal capacitance value to obtain the required value at the relevant operation point.

VCC Decoupling Capacitor

VCC is an internal LDO output. Place an external 4.7µF decoupling capacitor between VCC and AGND, and as close to these pins as possible.

Selecting the Inductor

The MP2651 can operate in buck mode or boost mode, which means that the inductor current is equal to either the charging current (I_{CHG}) or I_{IN}. The inductor's saturation current should exceed the larger value between I_{IN} and I_{CHG}, plus half the ripple current. The inductor current ripples for buck mode and boost mode are calculated with Equation (4) and Equation (5), respectively:

$$I_{RIPPLE\_BUCK} = \frac{V_{BATT} x (V_{IN} - V_{BATT})}{V_{IN} x f_{SW} x L} \quad (4)$$

$$I_{RIPPLE\_BOOST} = \frac{V_{IN} x (V_{BATT} - V_{IN})}{V_{BATT} x f_{SW} x L} \quad (5)$$

The inductor ripple current (I_{RIPPLE}) depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the switching frequency (f_{SW}), and the inductance (L).

The inductance (L) in buck mode can be estimated with Equation (6):

$$L = \frac{V_{BATT} x (V_{IN} - V_{BATT})}{I_{RIPPLE\_BUCK} x V_{IN} x f_{SW}} \quad (6)$$

The required inductance (L) in boost mode can be calculated with Equation (7):

$$L = \frac{V_{IN} x (V_{BATT} - V_{IN})}{V_{BATT} x f_{SW} x I_{RIPPLE\_BOOST}} \quad (7)$$

The MP2651 has a configurable switching frequency from 500kHz to 1.2MHz. Higher switching frequencies mean that smaller-value inductors can be used. The inductor saturation current should exceed I_{CHG} plus half of the ripple current.

The maximum input ripple current occurs when D = 0.5. For example, the battery charging voltage ranges between 6V and 9V for 2-cell battery packs. For a 15V adapter voltage, a 7.5V V_{BATT} gives the maximum inductor ripple current. Another example is a 3-cell battery with a V_{BATT} range between 9V and 13.2V. For a 20V adapter voltage, a 10V V_{BATT} gives the maximum inductor ripple current.

Generally, the inductor ripple is designed to be between 20% and 40% of the maximum charging current. For practical designs, there is a tradeoff between inductor size and efficiency.

Selecting the Output Capacitor

The output capacitor (C_{BATT}) should have a sufficient ripple current rating to absorb the output AC current.

In boost mode, I_{OUT} is discontinuous and dominates the output RMS ripple current. The output RMS ripple current (I_{CBATT_BOOST}) can be calculated with Equation (8):

$$I_{CBATT\_BOOST} = I_{CHG} x \frac{\sqrt{V_{IN} \times (V_{BATT} - V_{IN})}}{V_{IN}} \quad (8)$$

The worst-case output RMS ripple current occurs at the lowest VBUS input voltage. The CFLR voltage is approximately 8V for the 2-cell battery packs, so the worst-case scenario occurs when the voltage is 5V in source mode. Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended for the output decoupling capacitor. This capacitor should be placed as close as possible to the CFLR and PGND pins.

The capacitor's voltage rating must exceed the normal V_{BATT} level. A capacitor with a minimum 16V voltage rating is recommended for 2-cell battery packs.

Current Sense

The MP2651 has current loops to limit the current and to improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current. Figure 16 shows the recommended connection.

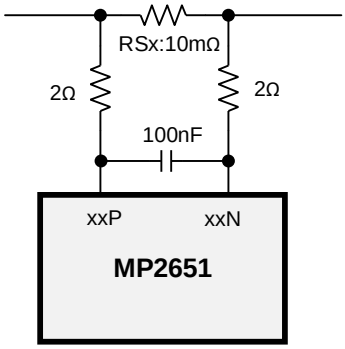


Figure 16: Input or Output Current-Sense Circuit

The I_{IN} loop limits the current drawn from the USB port or adapter, and I_{IN} is sensed through the IAP and IAN pins.

The battery current loop limits the charge current and discharge current. The battery current is sensed through the SRP and SRN pins.

Selecting the Resistor Divider for the NTC Thermistor Temperature

In real-world applications, an external NTC thermistor is placed close to the battery to sense the battery's temperature. The MP2651 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 7 on page 26). Every temperature corresponds to a voltage ratio. The MP2651 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature thresholds can be calculated with Equation (9) and Equation (10), respectively:

$$\frac{R_{T2} + R_{NTC\_HOT}}{R_{T1} + R_{T2} + R_{NTC\_HOT}} = \frac{V_{HOT}}{V_{VNTC}} \quad (9)$$

$$\frac{R_{T2} + R_{NTC\_COLD}}{R_{T1} + R_{T2} + R_{NTC\_COLD}} = \frac{V_{COLD}}{V_{VNTC}} \quad (10)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point.

By default, V_{HOT} / V_{VNTC} is 23.6%, while V_{COLD} / V_{VNTC} is 74.5%.

Assume that the expected hot and cold temperature thresholds are 60°C and 0°C, respectively. Using a 103AT thermistor as an example, the thermistor values are:

- R_{NTC_HOT} = 2.981kΩ
- R_{NTC_COLD} = 28.704kΩ

R_{T1} and R_{T2} can be calculated with Equation (9) or Equation (10). In this scenario, R_{T1} = 9.845kΩ, R_{T2} = 60Ω.

For simplification, a 10kΩ R_{T1} can be used, and R_{T2} can be replaced with a wire.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer PCB is recommended. For the best performance, refer to Figure 17 and follow the guidelines below:

1. Place the output capacitors as close to CFLR and PGND as possible. Place a small-sized, 1µF (e.g. 0603) capacitor closer than the other 22µF capacitors.
2. Tie the ground connections for the input and output capacitors to the IC ground with a short copper trace connection or PGND plane.
3. Place the input capacitors as close to IN and PGND as possible. Place a small-sized, 1µF (e.g. 0603) capacitor closer than the other 10µF capacitors.
4. Route the connection between CFLR/IN and its 1µF capacitor on the same layer with the IC. The connection to PGND must be on the same layer as the IC. Keep this routing loop as small as possible.
5. Connect AGND and PGND to each decoupling capacitor via a single-point connection.
6. Place the VCC decoupling capacitor and the bootstrap capacitors next to the IC, and keep the trace connections as short as possible.
7. Use a Kelvin connection for the current-sense resistor.
8. Route current-sense wires (IAP and IAN, then SRP and SRN) away from switching nodes, such as SW1 and SW2.

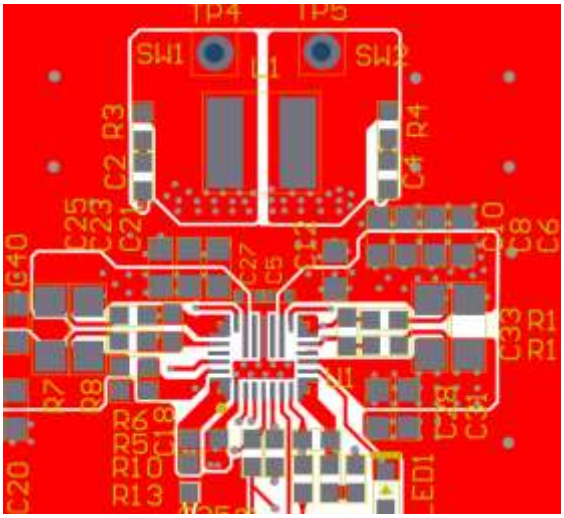


Figure 17: Recommended PCB Layout

Design Example

Table 5 shows a design example following the application guidelines for the specifications below.

Table 5: Design Example

V_{IN}	5V to 20V
V_{BATT_REG}	8.4V
f_{SW}	600kHz
I_{CC}	3A
V_{IN_SRC}	5V to 20V

Figure 18 on page 57 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 17. For more device applications, refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

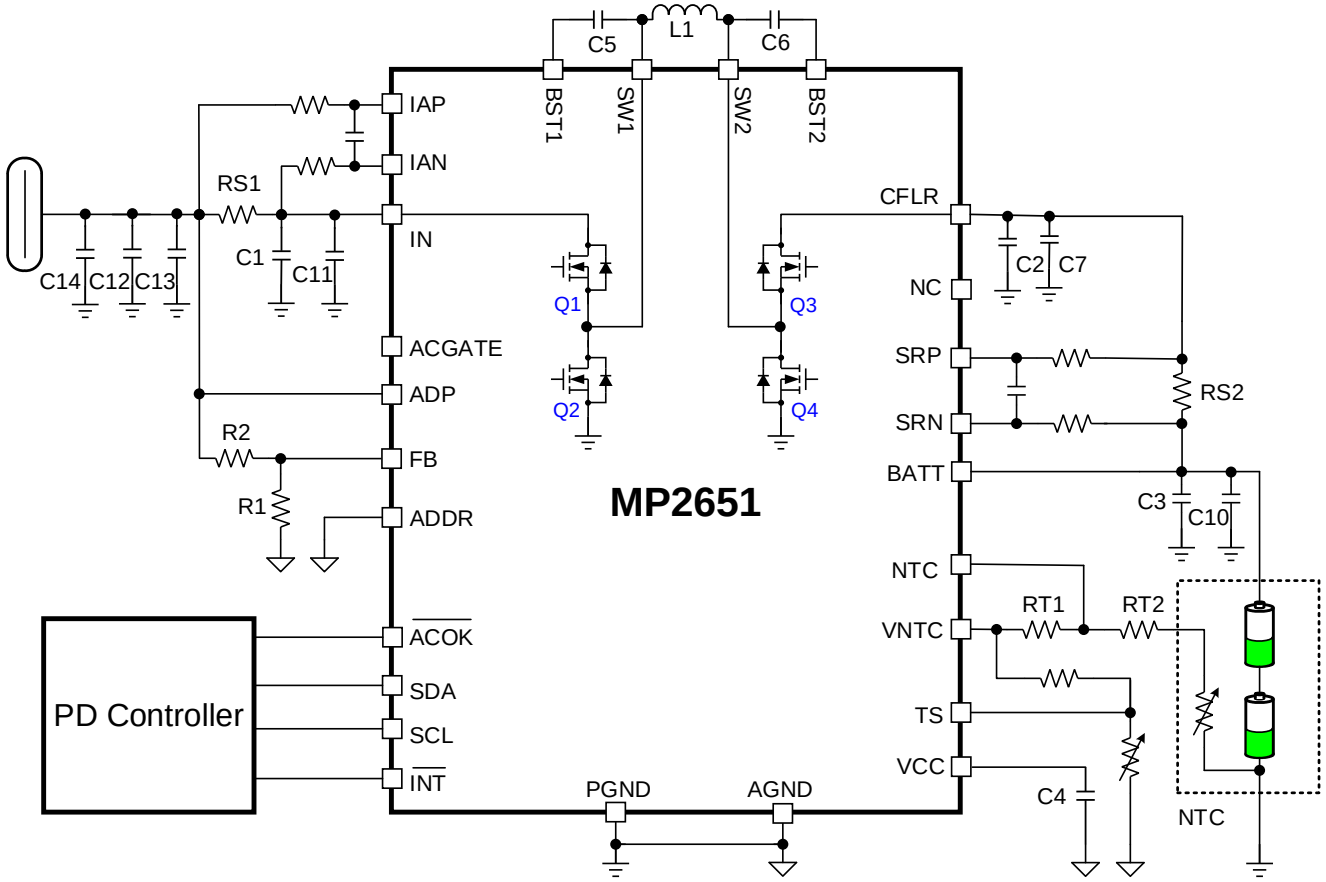


Figure 18: Typical Application Circuit without Input Block FETs

Table 6: Key BOM for Figure 18

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 25V, X7S	0805	Any
4	C2, C3,C7, C10	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} > 14A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any

TYPICAL APPLICATION CIRCUITS *(continued)*

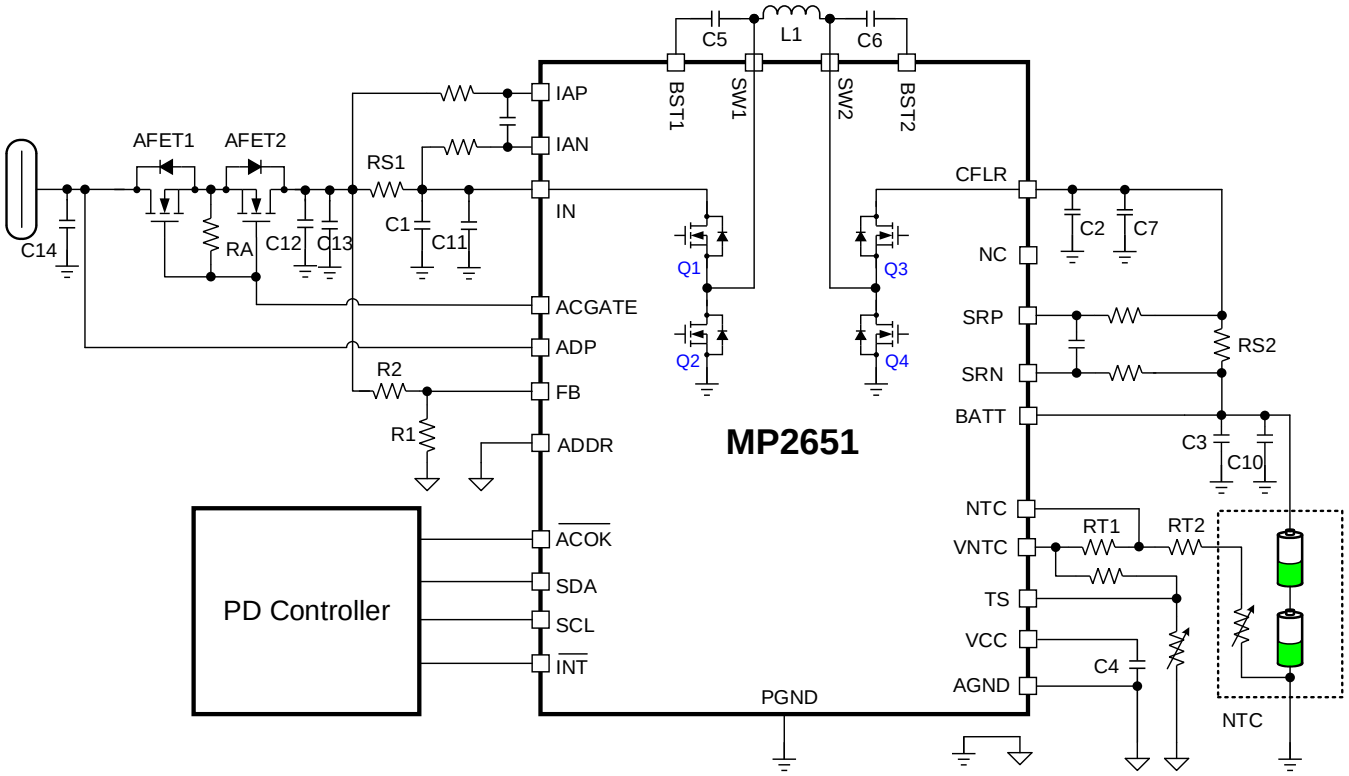


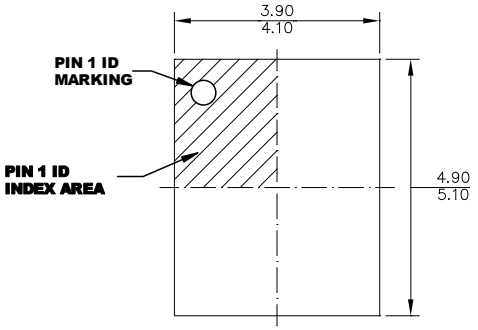
Figure 19: Typical Application Circuit with Input Block FETs

Table 7: Key BOM for Figure 19

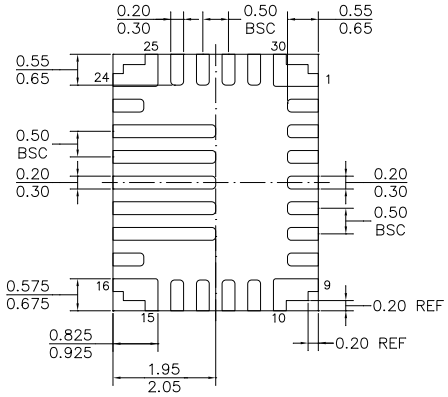
Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 25V, X7S	0805	Any
4	C2, C3, C7, C10	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} > 14A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
1	RA	5MΩ	Film resistor, 5%	0603	Any
2	AFET1, AFET2,	SISA14DN-T1-GE3	N-channel MOSFET, 30V, 5.1mΩ, 20A	Power PAK 1212-8	Vishay

PACKAGE INFORMATION

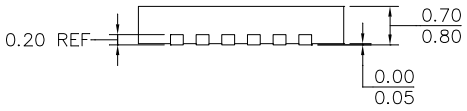
TQFN-30 (4mmx5mm)



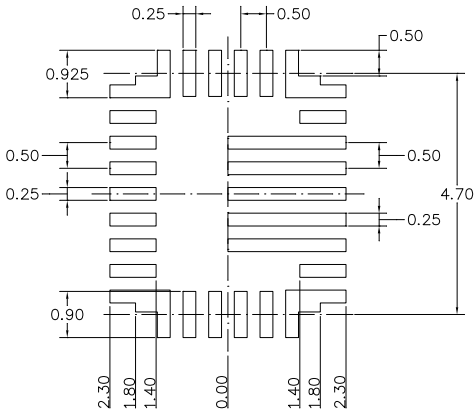
TOP VIEW



BOTTOM VIEW



SIDE VIEW

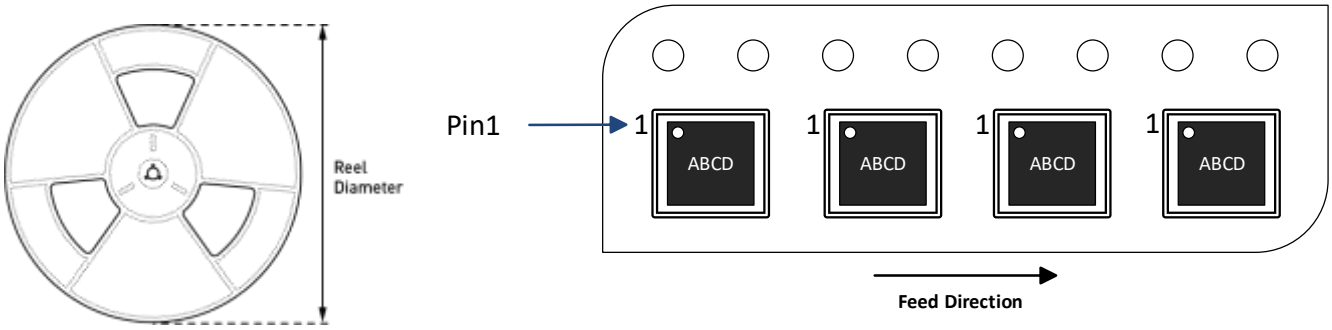


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2651GVT-xxxx-Z	TQFN-30 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/24/2022	Initial Release	-