NCV51511

Synchronous Buck with NCV51511 Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The Evaluation board is developed to evaluate performance of high side and low side gate driver and the target application is 300W non−isolation Synchonous Buck 48 V ±10% input voltage and 28 V regulated output voltage.

To supply bias voltage both synchronous buck and NCV51511, the NCV33163 control the auxiliary power output around 10 V. And the main synchronous buck controller generate high side and low side PWM input signal for NCV51511.The NCV51511 drive the high side and low side external MOSFET depend on the input PWM signal and V_{DD} level.

In this demonstration note introduces the features of the evaluation board, schematic, layout, and the test results. As the main focus of the evaluation board is to present NCV51511 performance.

NCV51511 Features

- Drives two N−Channel MOSFETs in High & Low Side
- Integrated Bootstrap Diode for High Side Gate Drive
- Bootstrap Supply Voltage Range up to 100 V
- 3 A Source, 6 A Sink Output Current Capability
- Drives 1 nF Load with Typical Rise/Fall Times of 6 ns/4 ns
- TTL Compatible Input Thresholds
- Wide Supply Voltage Range 8 V to 16 V (Absolute Maximum 18 V)
- Fast Propagation Delay Times (Typ. 30 ns)
- 2 ns Delay Matching (Typical)
- Under Voltage Lockout (UVLO) Protection for Drive Voltage
- Operating Junction Temperature Range of −40°C to 125°C

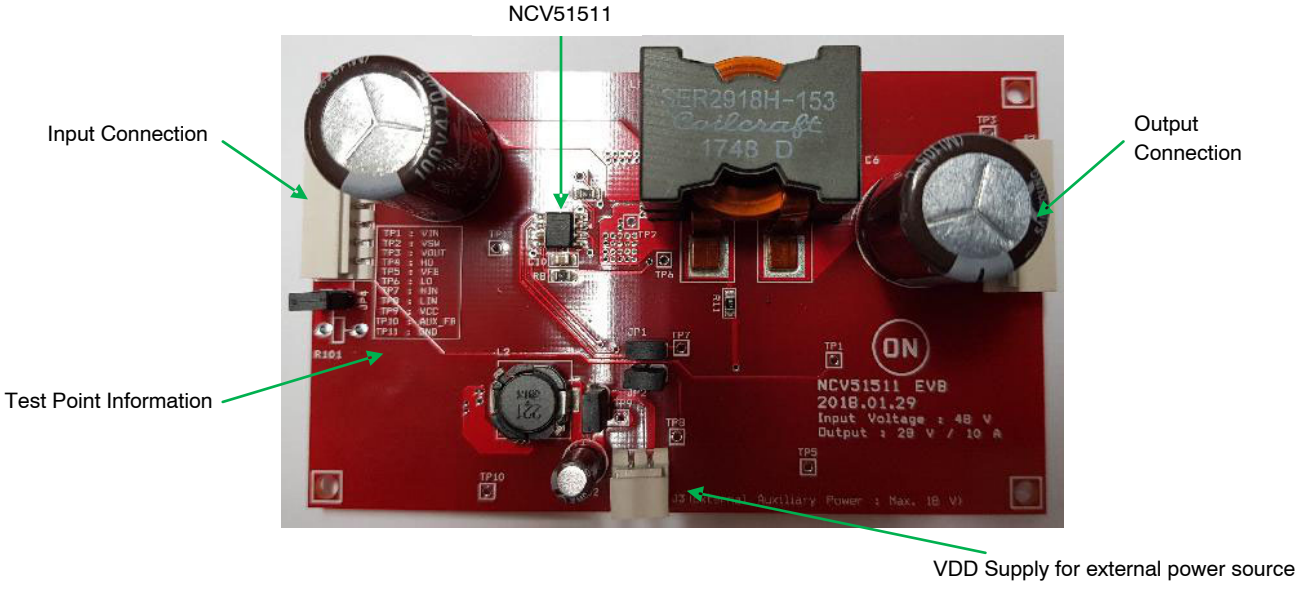

Figure 1. NCP51511 Evaluation Board

ABSOLUTE MAXIMUM RATINGS

Pin Name	Description	Maximum Voltage	Maximum Current
VIN	DC Input Voltage	60 V	5.0 A
VOUT	Regulated DC Output Voltage	28 V	11 A
VAUX	Auxiliary Power Input	18 V	0.5 A
GND	Ground	–	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NCV51511 EVALUATION BOARD USER TERMINALS

Pin Name	Description
VIN	Positive DC input voltage, 36 V to 60 V
GND	Common power negative / signal returen
VOUT	Regulated DC output voltage 28 V
VAUX	Regulated DC output for V_{DD} auxiliary power
JP1	High side Input signal connection to the gate driver HIN
JP2	Low side Input signal connection to the gate driver LIN
JP3	Auxiliary power connection for supply V_{DD} both Sync buck controller and driver IC Shorted : Sync buck and NCV51511 using auxiliary power output for VDD. Open : Sync buck and NCV51511 using external power directly from the J3 Connector.
JP4	Auxiliary power input connection

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 38 V < V_{IN} < 58 V, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Voltage	Positive DC input	37	48	60	V
Input Voltage UVLO		–	36	–	V
AUX output voltage		–	10.6	–	V
Output voltage	No Load Condition	–	28.8	–	V
	Full Load Condition	–	28.5	–	V
Overcurrent Threshold		–	–	13	A
Soft Start Time		–	20	–	ms
Switching Frequency		190	200	210	kHz
System Efficiency	50% Load @ 48 V	–	97.2	–	%
	100% Load @ 48 V	–	97.0	–	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NCV51511

The NCV51511 is high side and low side gate−drive IC designed for high−voltage, high−speed, driving MOSFETs operating up to 80 V.

The NCV51511 integrates a driver IC and a bootstrap diode. The driver IC features low delay time and matched PWM input propagation delays, which further enhance the performance of the part.

The high speed dual gate driver are designed to drive both the high−side and low−side of N−Channel MOSFETs in a half bridge or synchronous buck configuration. The floating high−side driver is capable of operating with supply voltages of up to 80 V. In the dual gate driver, the high side and low side each have independent inputs which allow maximum flexibility of input control signals in the application. The PWM input signal (high level) can be 3.3 V, 5 V or up to V_{DD} logic input to cover all possible applications. The bootstrap diode for the high−side driver bias supply is integrated in the chip. The high−side driver is referenced to the switch node (HS) which is typically the source pin of the high−side MOSFET and drain pin of the low−side MOSFET. The low−side driver is referenced to V_{SS} which is typically ground. The functions contained are the input stages, UVLO protection, level shift, bootstrap diode, and output driver stages.

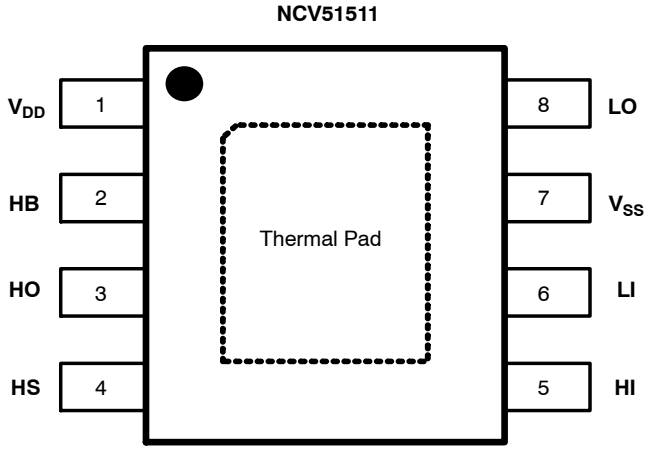

Figure 2. NCV51511 Pin Connection

NCV51511 PIN DESCRIPTION

Pin No.	Pin Name	Description
1	V_{DD}	Logic and low−side gate driver power supply voltage
2	HB	High−side floating supply
3	HO	High−side driver output
4	HS	High−voltage floating supply return
5	HI	Logic input for High−side gate driver output
6	LI	Logic input for Low−side gate driver output
7	V_{SS}	Logic Ground
8	LO	Low−side driver output
−	Exposed PAD	Connect to Pin 7 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Synchronous Buck Controller

To make the high side and low side input signal for NCV51511 and use the close loop control for the Synchronous Buck application, the evaluation board utilized NCP1034. The NCP1034 is high voltage PWM controller designed for synchronous buck DC/DC applications with input voltage up to 100 V.

The switching frequency is programmable from 25 kHz up to 500 kHz allowing the flexibility to tune for efficiency and size.The operating frequency is set by an external resistor connected from the Rt pin to ground.

The soft start time is set by capacitor connected between SS/SD pin and ground this function is used for controlling the output voltage slope and limiting start up currents.

To prevent over current condition, the NCP1034 has Overcurrent Protection function. The programmed current limit is set by external resistor between OCset and GND. And the voltage drop across the low side MOSFET RDSON is connect through resistor and into OCin. Within the IC, value is compared with the programmed overcurrent limit.

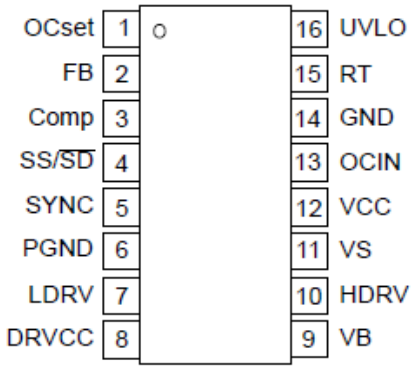

Figure 3. NCP1034 Pin Connections

NCP1034 PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	OC_{SET}	Current limit set point. A resistor from this pin to GND will set the positive and negative current limit threshold
2	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divier to set the output voltage and provide feedback to the error amplifier
3	COMP	Output of error amplifier. An extermal resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
4	SS/SD	Soft−Start / Shutdown. This pin provides user programmable soft start function. External capacitor connected from this pin to ground sets the startup time of the output voltage. The conveter can be shutdown by pulling this pin below 0.3 V.
5	SYNC	The internal oscillator can be synchronized to an external clock via this pin and other IC□s can be synchro-nized via this pin to internal oscillator. If it is not used this pin should be connected via 10 k□ resistor to ground
6	P_{GND}	Power Ground. This pin serves as a separate ground for the MOSFET driver and should be connected to the system□s power ground plane.
7	LDRV	Output driver for low side MOSFET
8	$DRVV_{CC}$	This pin provides biasing for the internal low side driver. A minimum of 0.1 uF, high frequency capacitor must be connected from this pin to power ground.
9	VB	This pin powers the high side driver and must be connected to a voltage higher than input voltage. A minimum of 0.1 uF, high frequency capacitor must be connected from this pin to switch node.
10	HDRV	Output driver of rhigh side MOSFET.
11	V_S	Switch Node. This pin is connected to the source of the upper MOSFET and the drain of the lower MOSFET.
12	V_{CC}	This pin provides power for the internal blocks of the IC. A minimum of 0.1 uF, high frequency capacitor must be connencted from this pin to ground.
13	OC_{IN}	Overcurrent sensing input. A serial resistor from this pin to drain of low MOSFET must be used to limit the current into this pin.
14	GND	Signal ground for internal reference and control circuitry
15	R_T	Connecting a resistor from this pin to ground sets the oscillator frequency.
16	UVLO	An external voltage divider is used to set the undervoltage threshold levels.

In this board, the NCP1034 only make the high side and low side input PWM signal and utilize close loop control with protection function. So, the VS is connect with GND and supplied voltage to VB directly.

If the engineers want to know more features or performance of the NCP1034, refer to the datasheet.

Auxiliary Power Controller

EVB auxiliary power designed for power supply to both VCC of the synchronous buck controller and VDD for NCV51511 driver IC. This bock is also consist of DC/DC buck converter. The auxiliary power controller used the NCV33163 to cover the wide input voltage, which is monolithic power switching regulators optimized for DC/DC converter applications.

This device consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a shigh current output switch. Protective features consist of cycle by cycle current limiting, and internal thermal shutdown.

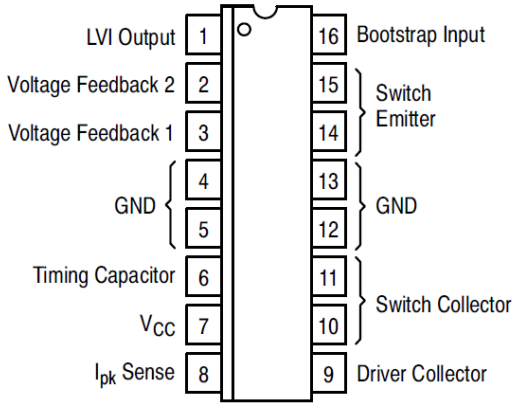

Figure 4. NCV33163 Pin Connections

If the enginners want to know more features or performance of the NCV33163, refer to the datasheet.

Jumper Setup

There are three jumpers on the EVB, with the help of which the engineers to start setup EVB for testing. Table below lists the purpose of the jumpers and their default setup.

EVB JUMPER SETUP

Header Label	Purpose	Default
JP1	High side Input signal connection to the gate driver HIN	Short
JP2	Low side Input signal connection to the gate driver LIN	Short
JP3	Auxiliary power connection to the Sync buck controller and driver IC Short : Sync buck and NCV51511 using auxiliary power output for VDD. Open : Sync buck and NCV51511 using external power directly from the J3 Connector.	Short

Typical Operation

The NCP1034 only make the high side and low side input PWM signal and the NCV33163 control the regulated voltage for power supply to both the Sync buck and gate driver VDD.

Typical output signals of NCP1034 controller and VDD regulated voltage are illustrated in Figure 5 when the JP1 and JP2 open condition. HDRV and LDRV pin are the signals generated by the controller to drive NCV51511. The HDRV make full turn on signal and the LDRV make minimum turn on due to no feedback from the output voltage. The user can confirm in this stage that the control signal and Auxiliary power operate well.

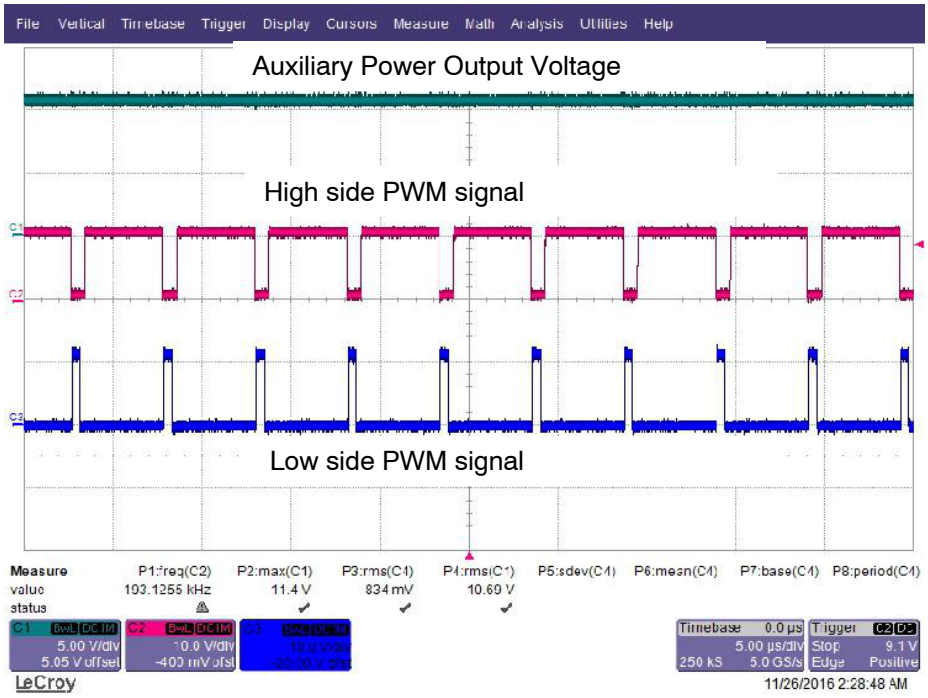

Figure 5. NCP1034 Controller Output Signals and Regulated Output Voltage of AUX Power

Measure the operating waveforms of NCV51511 input to output signal when synchronous buck close loop control at connect JP1 and JP2 as shown in Figure 6.

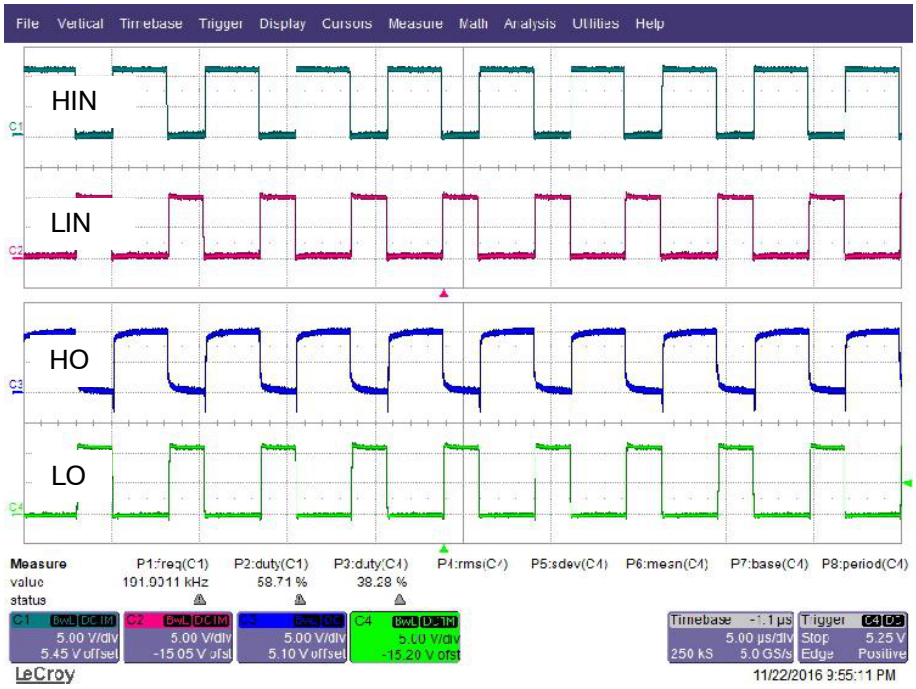

Figure 6. NCV51511 Input to Output Signal

The NCV51511 utilized high speed gate driving for synchronous buck and half bridge applications. In these applications, the ringing voltage occurred by parasitic inductance of the primary power path, consisting of the input capacitor and switching MOSFETs (C_{oss}).

To reduce the ringing phenomenon, the first step is to optimize the PCB layout to reduce parasitic components of the power path. And the second step is adding a series resistor with the bootstrap capacitor to slow down the turn−on transition of the high side MOSFET.

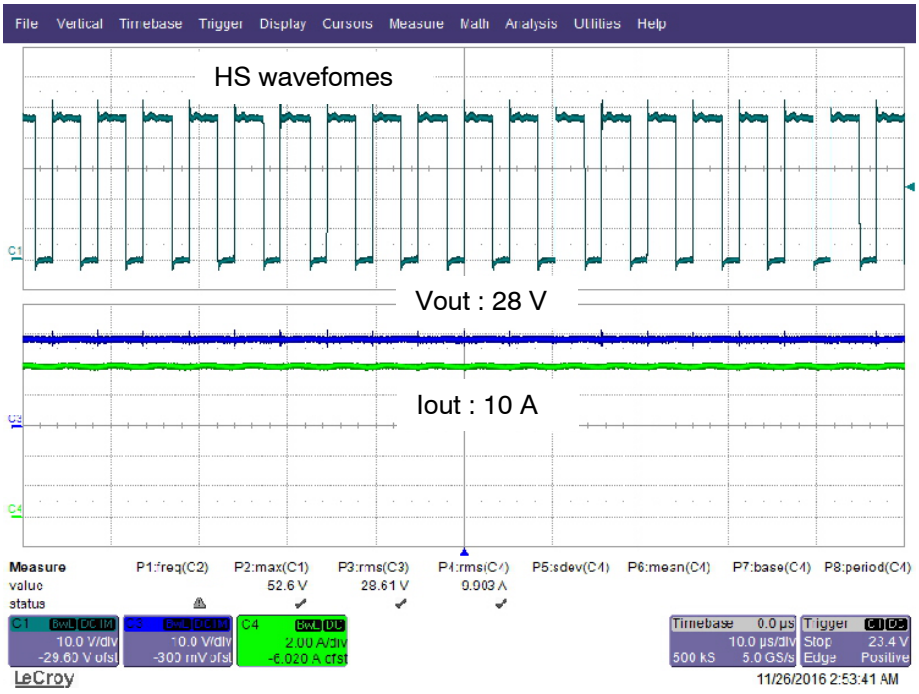

Figure 7. Switching Node Waveforms at Full Load Condition

Figure 8 presents the EVB line voltage response, where the input voltage step changes with a slew rate 16 V / ms from 40 V to 56 V, then back to 56 V to 40 V.

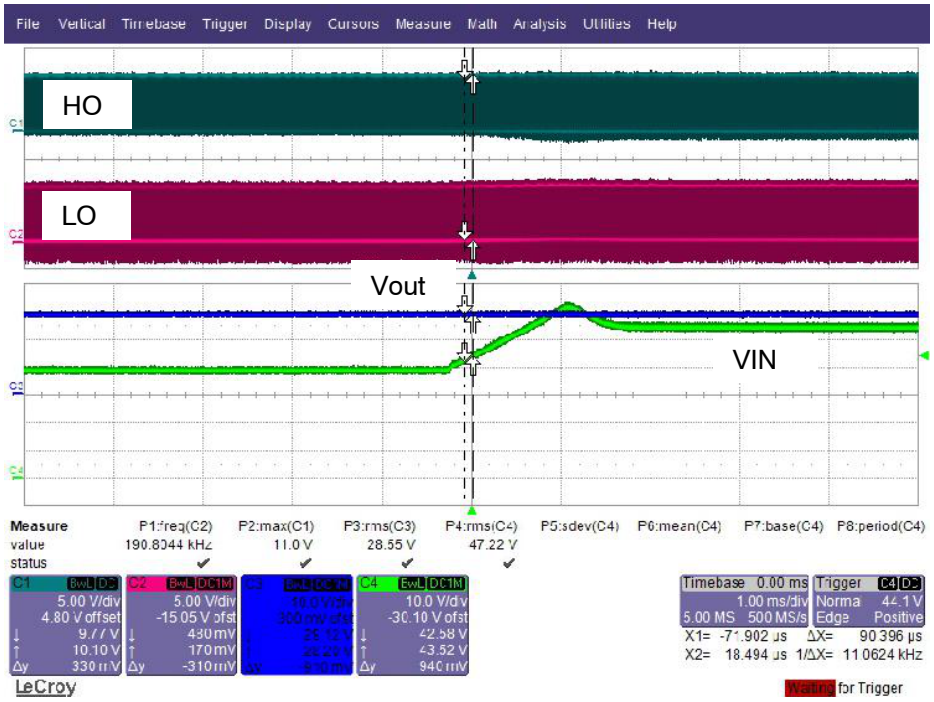

Figure 8. Line Response when Input Voltage Change 40 V to 56 V

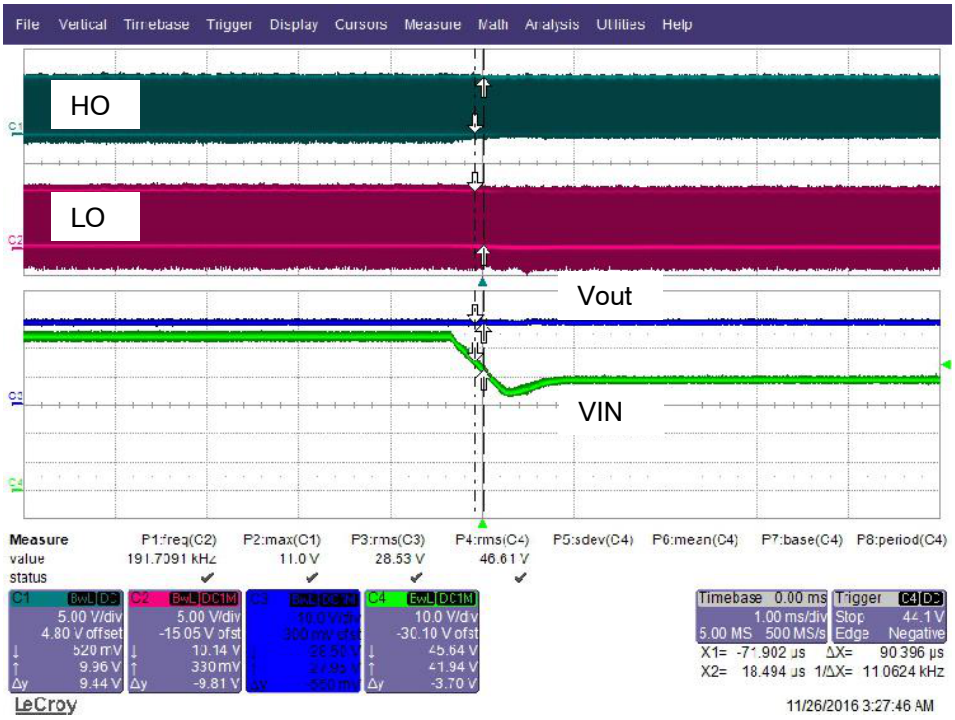

Figure 9. Line Response when Input Voltage Change 56 V to 40 V

Figure 10 presents the EVB output load response, where the output current step changes with a slew rate 40 A / ms from 0 A to 10 A, then back to 10 A to 0 A.

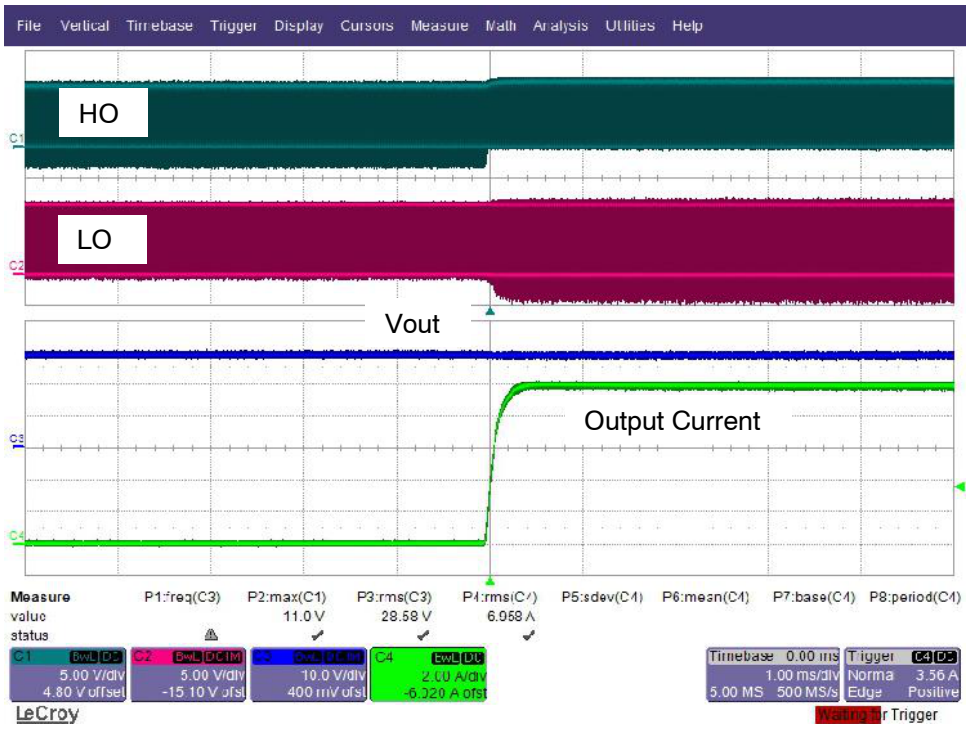

Figure 10. Load Response when Output Current Change 0 A to 10 A

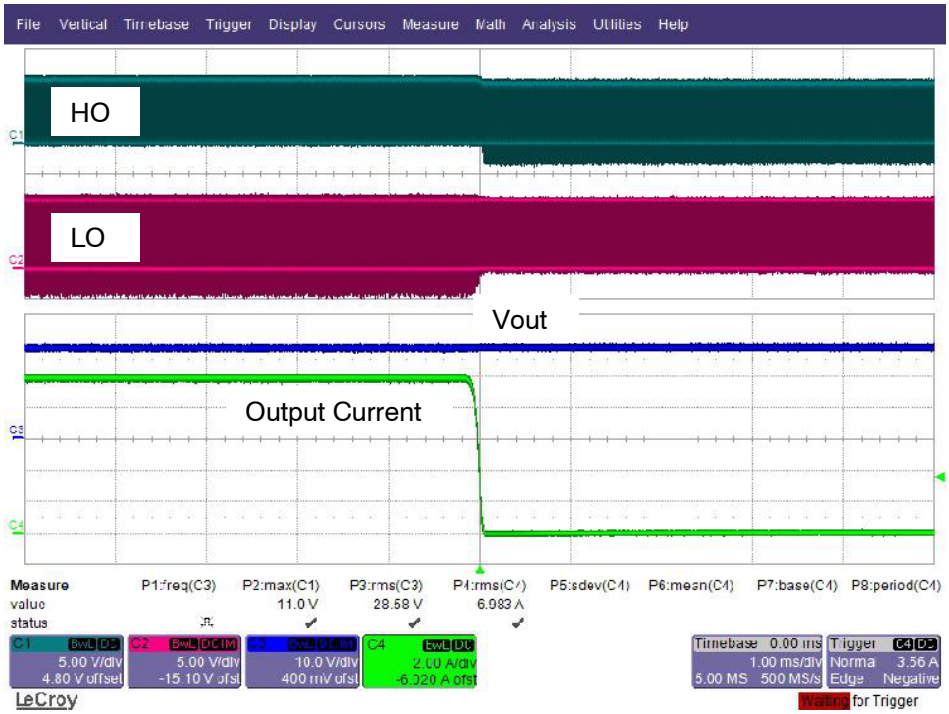

Figure 11. Load Response when Output Current Change 10 A to 0 A

System Efficiency

Fig x presents the system efficiency of the EVB under different input voltage The EVB demonstrated that the 300 W synchronous buck application can approach 97.2% peak system efficiency at heavy load condition. Furthermore, the light load system efficiency is above 95% when the output power around 50 Watt.

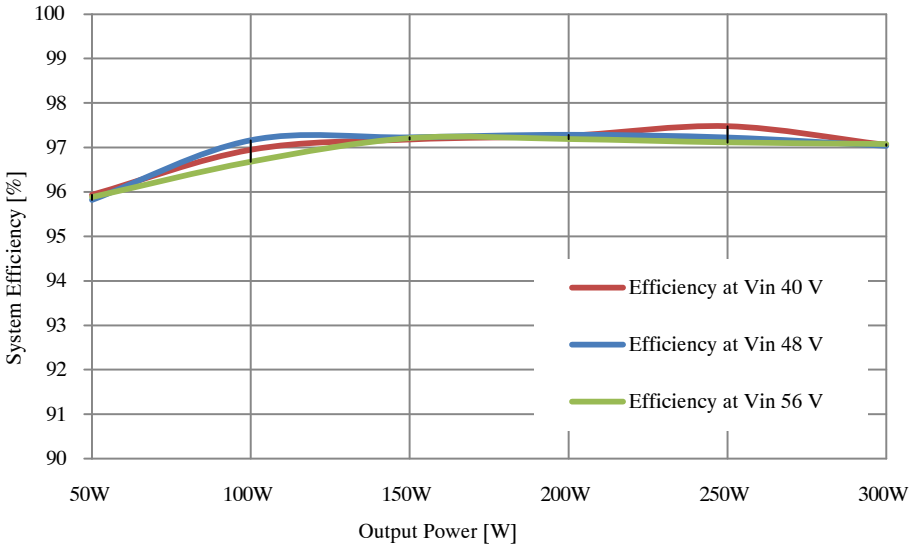

Figure 12. System Efficiency by the Input Voltage

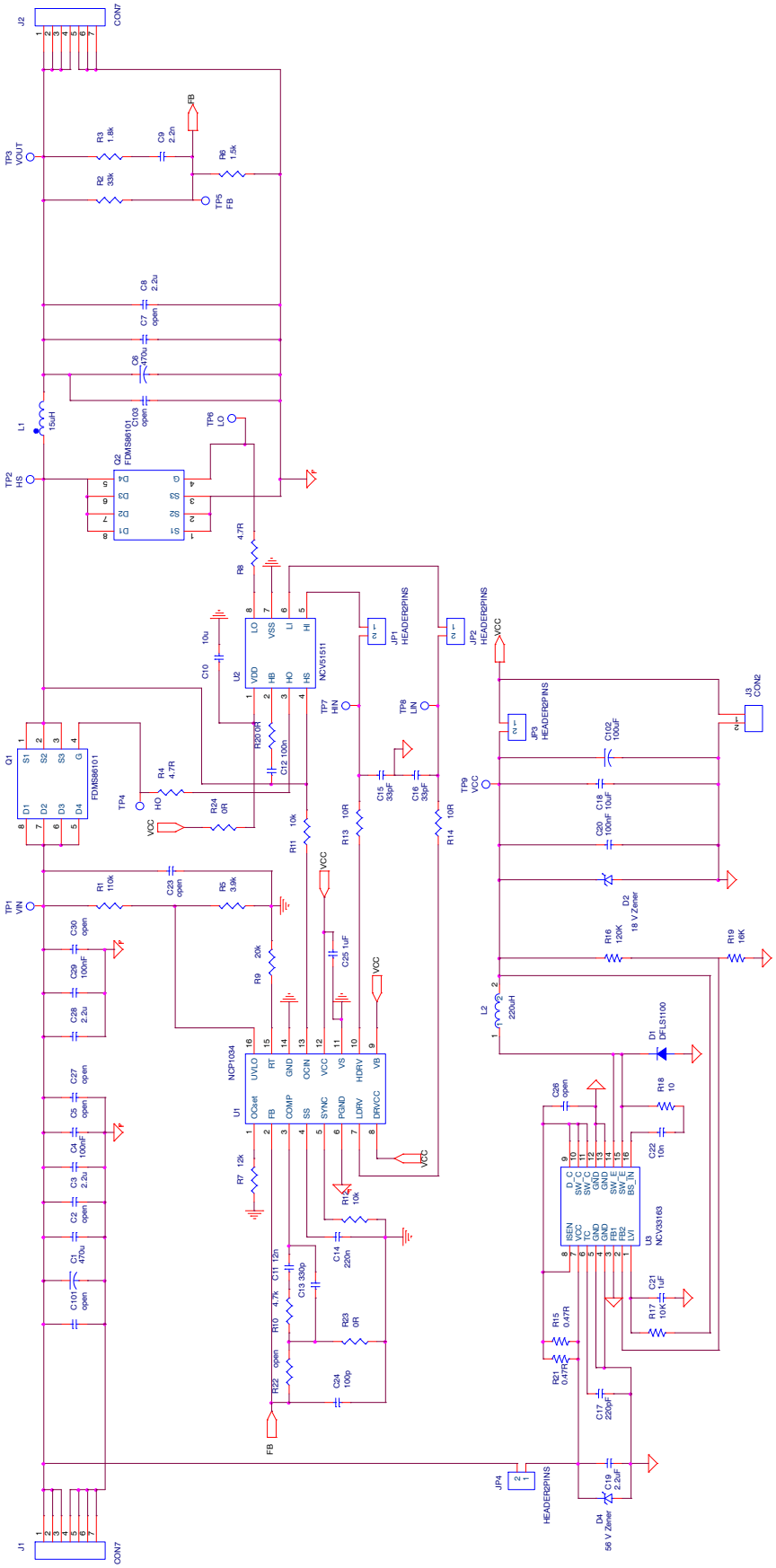

Figure 13. Synchronous Buck Converter Schematics

LIST OF TEST POINTS

TP	Reference	Description
TP1	VIN	DC Input Power Supply
TP2	HS	High Voltage Floating Supply Return
TP3	VOUT	Regulated DC Output Voltage
TP4	HO	High Side Driver Output
TP5	FB	Regulated Output Feedback Voltage
TP6	LO	Low Side Driver Output
TP7	HIN	Logic Input for High Side Gate Drive
TP8	LIN	Logic Input for Low Side Gate Drive
TP9	VDD	Gate Driver Power Supply
TP10	AUX_FB	Auxiliary Power Feedback Voltage
TP11	GND	Ground
JP1	JUMPER 1	High Side Logic Input Connection
JP2	JUMPER 2	Low Side Logic Input Connection
JP3	JUMPER 3	Auxiliary power connection for supply V_{DD} both Sync buck controller and driver IC
JP4	JUMPER 4	Auxiliary power input connection

BILL OF MATERIALS

Reference	Vendor	Part Number	Type	Value	PC/Board
C1,C6	SAMYOUNG	KMG 100 V/ 470uF	EL−Cap	100 V / 470uF	2
C3, C8, C19, C28	TDK	C3216X7S2A225K160AB	MLCC_3216	100 V / 2.2uF	4
C4, C29	TDK	C3216X7R2A104K160AA	MLCC_3216	100 V / 100nF	2
C9	TDK	C2012CH1H222J085AA	MLCC_2012	50 V / 2.2nF	1
C10,C18	TDK	C2012X5R1E106M125AB	MLCC_2012	25 V / 10uF	2
C11	TDK	C2012C0G1H123J060AA	MLCC_2012	25 V / 12nF	1
C12	TDK	C1608X8R1E104K080AA	MLCC_1608	25 V / 100nF	1
C13	TDK	CGJ4C2C0G2A331J060AA	MLCC_2012	50 V / 330pF	1
C14	TDK	C2012X8R1E224K125AA	MLCC_2012	25 V / 220nF	1
C15, C16	TDK	CGJ4C2C0G2A330J060AA	MLCC_2012	50 V / 33pF	2
C17	TDK	CGJ4C2C0G2A221J060AA	MLCC_2012	50 V / 220pF	1
C20	TDK	C2012X7R1H104K125AE	MLCC_2012	25 V / 100nF	1
C21, C25	TDK	C2012X7R1E105K085AB	MLCC_2012	25 V / 1uF	2
C22	TDK	C2012C0G1E103J060AA	MLCC_2012	25 V / 10nF	1
C24	TDK	C2012 C0G1E101J060AA	MLCC_2012	25 V / 100pF	1
C102	SAMYOUNG	16 V / 100uF	EL−Cap	16 V / 100uF	1
C2,C5, C7, C23, C26, C27, C30, C101, C103		−	OPEN	OPEN	9
D1, D3	DIODES	DFLS1100	SMD	100 V / 1A	2
D2	ON	MMSZ18VCF	SOD 123	18 V Zener	1
D4	ON	MM5Z56V	SOD 123	56 V Zener	1
L1	Coilcraft	SER2918H−153	SMD	15uA	1
L2	TDK	CLF10040T−221M	SMD	220uA	1
Q1,Q2	ON	FDMS86101	POWER 56	100 V / 60 A	1
R1	Yageo	RC0805JR−07114RL	CHIP_R_2012	110K	1
R2	Yageo	RC0805JR−07333RL	CHIP_R_2012	33K	1

BILL OF MATERIALS

Reference	Vendor	Part Number	Type	Value	PC/Board
R3	Yageo	RC0805JR−07182RL	CHIP_R_2012	1.8K	1
R4,R8	Yageo	RC0805JR−074R7RL	CHIP_R_2012	4.7R	2
R5	Yageo	RC0805JR−07392RL	CHIP_R_2012	3.9K	1
R6	Yageo	RC0805JR−07152RL	CHIP_R_2012	1.5K	1
R7	Yageo	RC0805JR−07123RL	CHIP_R_2012	12K	1
R9,	Yageo	RC0805JR−07203RL	CHIP_R_2012	20K	1
R10	Yageo	RC0805JR−07472RL	CHIP_R_2012	4.7K	1
R11, R12, R17	Yageo	RC0805JR−07103RL	CHIP_R_2012	10K	3
R13, R14, R18	Yageo	RC0805JR−07100RL	CHIP_R_2012	10R	3
R15, R21	Susumu	RL1632R−R0470−F	CHIP_R_3216	0.47R	2
R16	Yageo	RC0805JR−07124RL	CHIP_R_2012	120K	1
R19	Yageo	RC0805JR−07163RL	CHIP_R_2012	16K	1
R20	Yageo	RC0603JR−07000RL	CHIP_R_1608	0R	1
R22, R24	Yageo	RC0805JR−07000RL	CHIP_R_2012	0R	2
U1	ON Semiconductor	NCP1034			1
U2	ON Semiconductor	NCV51511			1
U3	ON Semiconductor	NCV33163			1
JP1, JP2, JP3, JP4	Hirose Electric	A2−40PA−2.54DSA	Jumper		4
J1, J2	MOLEX	5268−07	Connector		2
J3	MOLEX	5268−02	Connector		1

Drawings of Layers

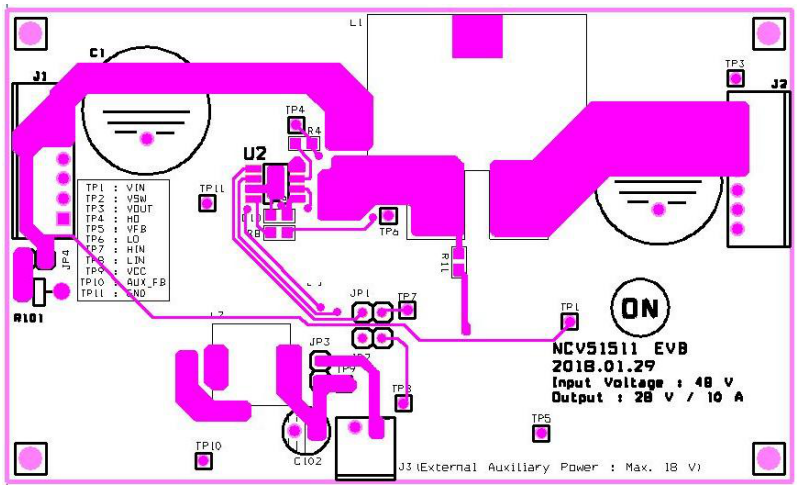

Figure 14. Top View

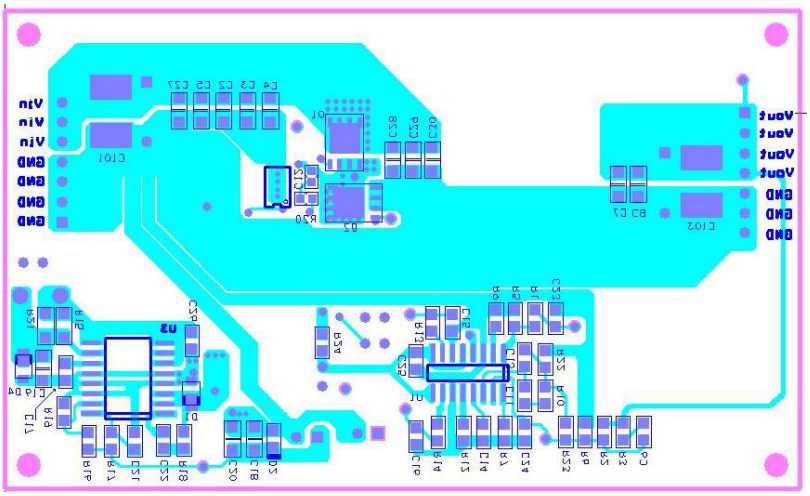

Figure 15. Bottom View

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