UM11746

RD33775ACNCEVB

Rev. 2 — 25 August 2022 User manual

Document information

Information	Content
Keywords	CCMU, MC33665A, MC33775A
Abstract	User manual to work with centralized cell monitoring unit (CCMU) in controller area network flexible data rate (CAN FD) to perform voltage monitor and passive balancing with MC33775A.

Revision history

Rev	Date	Description
2	20220825	Modifications • Section 2, Section 3, and Section 4: updated text
1	20220802	initial version

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY.

It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

This document provides guidelines to use RD33775ACNCEVB.

2.1 Kit contents

The RD33775ACNCEVB kit contents include:

- RD33775ACNCEVB
- One transport protocol link (TPL) daisy chain cable
- One power and CAN interface cable
- Four cell interface cables
- Quick start guide

2.2 Additional hardware

NXP offers the following board solutions to check the functionality of devices and support the setup in testing the devices.

- BATT-14CEMULTAOR: 14-cell battery pack or a battery emulator
- BATT-14EXTENDER: battery emulator extender

3 Getting to know the hardware

3.1 Board overview

The RD33775ACNCEVB supports as a hardware reference design for centralized cell monitoring unit to communicate directly via CAN or CAN FD. The MC33665ATF4AE populated on RD33775ACNCEVB is a gateway router that can route TPL messages with CAN or CAN FD communication protocol. The MC33775A is a battery cell controller from NXP to monitor the cell voltages, temperatures, and passive balance. RD33775ACNCEVB can support to monitor up to 56 cells.

Note: *MC33665ATF4AE is used in RD33775ACNCEVB, any reference in this documentation as MC33665A is to be considered as MC33665ATF4AE.*

3.2 Board features

The main features of RD33775ACNCEVB are:

- CAN or CAN FD communication up to 5 Mbit/s to MC33665A
- Onboard CAN transceiver TJA1443
- Configurable CAN communication and CAN FD arbitration speeds using population variant of resistors for CFG0 and CFG1 pins
- Configurable CAN ID (ID0_STB_OD, ID1, ID2, and ID3) for MC33665A using population variant of resistors
- Four MC33775A battery cell controllers
- Voltage monitoring and passive cell balancing functionality for 56 cells (emulator or relevant)
- Capacitive isolation for daisy chain communication of onboard MC33775A devices
- Transformer isolation for offboard daisy chain communication and from TPL port 0 of MC33665A to MC33775A
- Flexible loopback configuration for single chain or two independent daisy chains without loopback

3.3 Block diagram

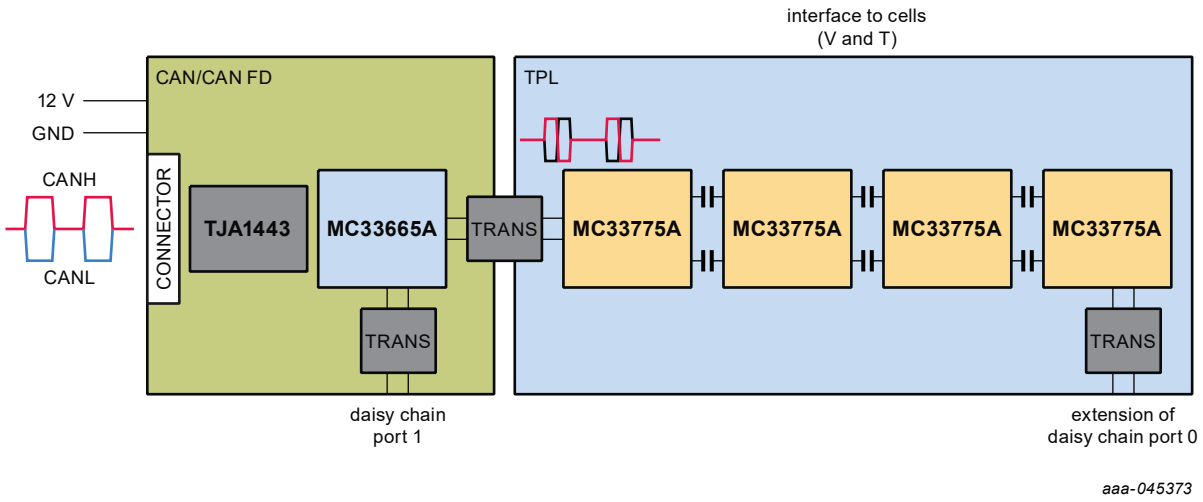

Figure 1. RD33775ACNCEVB block diagram

3.4 Board description

The RD33775ACNCEVB is the reference design for CCMU which can communicate directly with CAN or CAN FD.

Figure 2 shows the sections for the gateway IC MC33665A and four MC33775A battery cell controllers. MC33665A and TJA1443 CAN transceiver interface circuit is part of the low-voltage section which can be connected to 12 V and ground. It can communicate on low voltage (< 16 V) with standard tools and control units with J25 connector. TPL port 0 of MC33665A is interfaced to the first MC33775A onboard with transformer isolation. TPL port 1 of MC33665A is interfaced to J2 for offboard communication with battery cell controllers or to support the loopback for battery cell controller (BCC) devices on daisy chain port 0.

Contact NXP engineering team for using TPL_AUTOWAKE function of MC33665A in RD33775ACNCEVB.

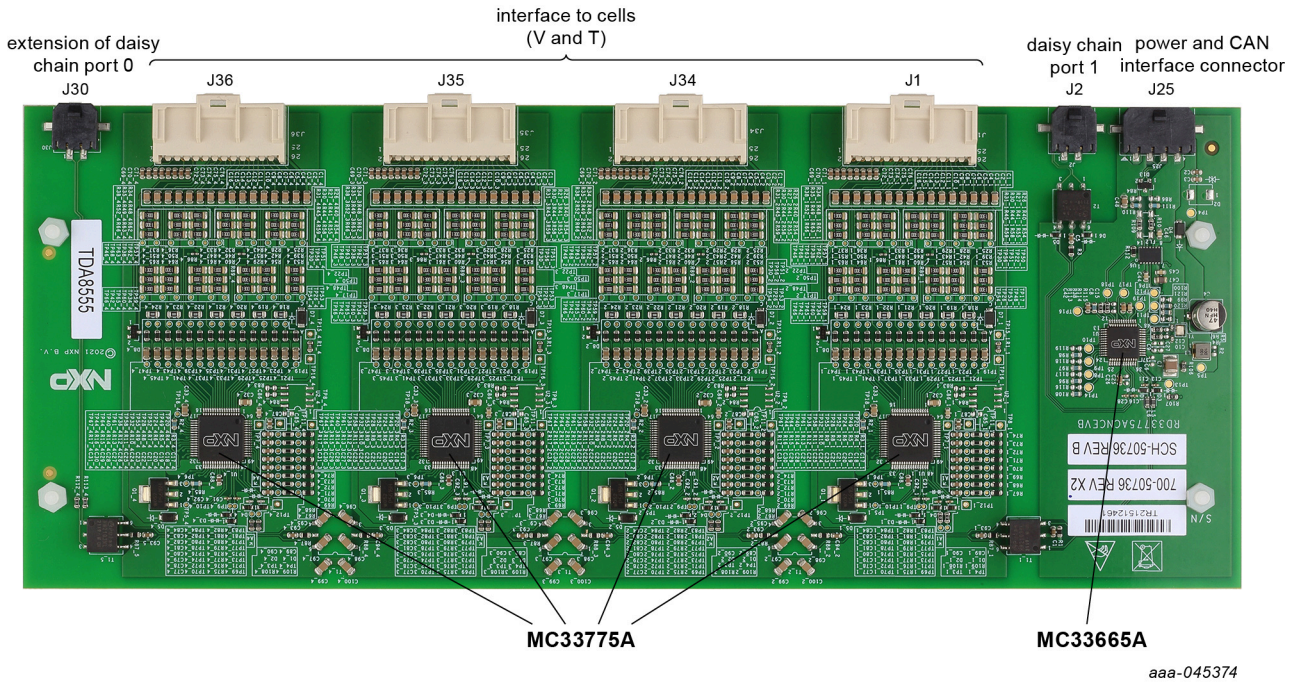

Figure 2. RD33775ACNCEVB description

MC33775A battery cell controllers are populated on the high-voltage section of the board. Galvanic isolation is maintained from high-voltage section of the board to low voltage with transformers. Maintaining the safety precautions of the lab and setup, cells emulators or relevant can be connected directly to J1, J34, J35, and J36 connectors. Low-pass filter and passive cell balancing resistors are populated and interfaced from cell connections to MC33775A. Four analog temperature measurements can be supported for every MC33775A. Features in MC33775A can be tested for 14 cell voltage, module voltage, and four temperature measurements. For more information, refer to the MC33775A data sheet.

TJA1443 is used as CAN transceiver for MC33665A. Split resistor termination is used for CAN termination (120 Ω). Common mode choke is depopulated onboard with bridge resistors to interface with TJA1443. Based on setup and requirements, FL2 common mode choke can be populated onboard. Refer to the schematics of RD33775ACNCEVB for MC33665A CAN interface circuit. Figure 3 is a short extract to understand the CAN termination of RD33775ACNCEVB.

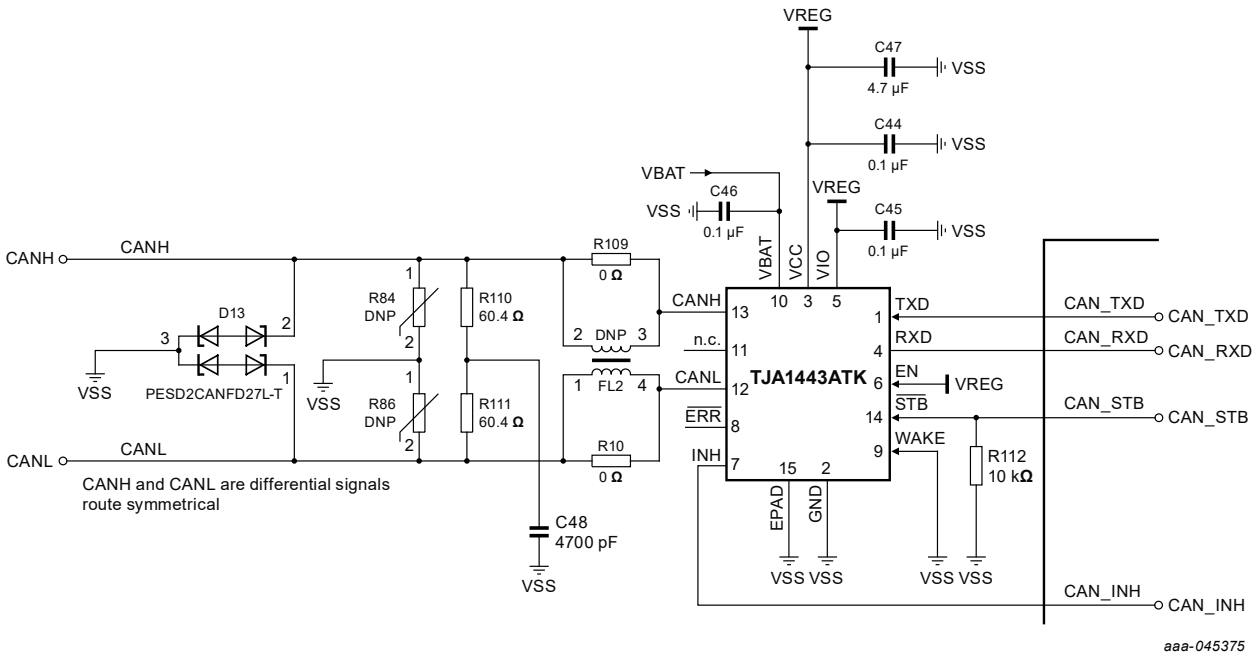

Figure 3. CAN transceiver interface

Check the need of external 120 Ω termination when interfacing CAN tools to RD33775ACNCEVB. If necessary, populate R84 and R86 with 60 Ω resistors.

CFG0, CFG1, ID0_STB_OD, ID1, ID2, and ID3 pins are important for communicating with MC33665A via CAN or CAN FD. CFG0 and CFG1 are used for setting baud rate for CAN or arbitration baud rate for CAN FD. ID0_STB_OD, ID1, ID2, and ID3 are used to set the CAN ID for communicating with MC33665A. Refer to the data sheet of MC33665A before setting the CAN ID to MC33665A. See Table 1 for setting of pin CFG0 and pin CFG1 of MC33665A.

Table 1. CFG pins of MC33665A

CFG1	CFG0	Baud rate (CAN or CAN FD arbitration)
0	0	250 kbit/s
0	1	500 kbit/s (default configuration)
1	0	1 Mbit/s
1	1	reserved

Figure 4 shows the interface circuit of MC33665A for setting the CFG0, CFG1, ID0_STB_OD, ID1, ID2, and ID3 pins. Pull-up resistors and pull-down resistors can be populated appropriately on RD33775ACNCEVB to set the respective pins of MC33665A HIGH or LOW.

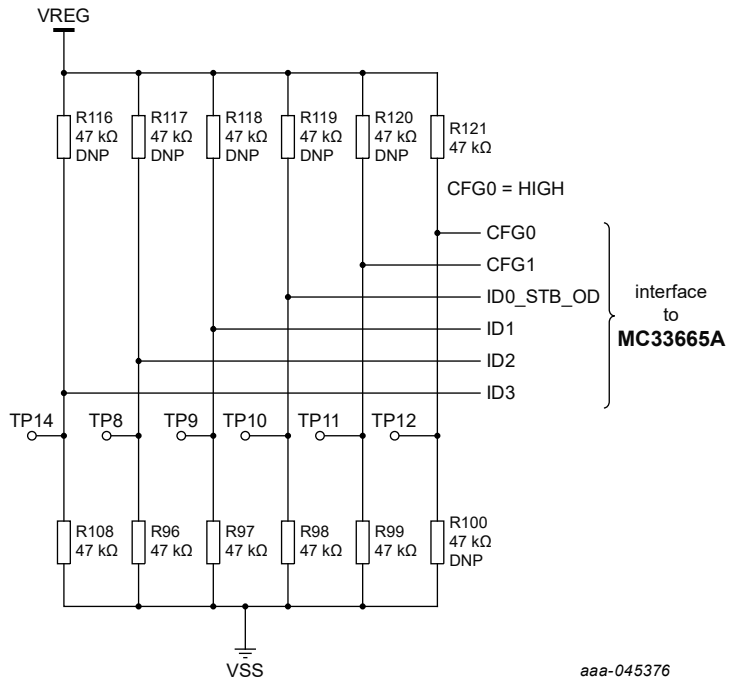

Figure 4. CAN HW settings for MC33665A

Based on the circuit shown in Figure 4, CFG0 is set to HIGH and CFG1 is set to LOW. CAN communication can be established with 500 kbit/s of baud rate and CAN FD arbitration baud rate is fixed at 500 kbit/s. ID0_STB_OD, ID1, ID2, and ID3 are set to zero.

3.5 Connectors

RD33775ACNCEVB has J25 which is a low-voltage connector for power and CAN. J2, J1, J34, J35, J36, and J30 are connectors to be considered as part of high voltage based on test setup.

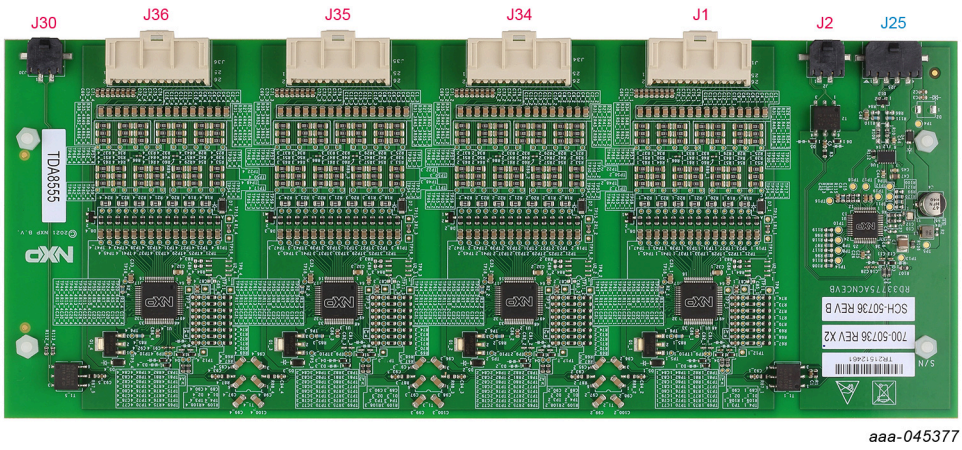

Figure 5. RD33775ACNCEVB connectors

Pin configuration of connectors is shown in Table 2 to Table 8.

Table 2. Power and CAN connector - J25

Pin number	Connection	Description
1	VBAT	connection to 12 V
2	CANH	used for CANH interface for external communication
3	CANL	used for CANL interface for external communication
4	GND	ground connection for MC33665A and interface boards

Table 3. Daisy chain TPL port 1 - J2

Pin number	Connection	Description
1	TPL1_P	daisy chain port 1 positive
2	TPL1_N	daisy chain port 1 negative

Table 4. Cell terminal and temperature - J1

Pin number	Connection	Description
1	GND_B1	ground for MC33775A B1
2	B1_NTC7	temperature measurement; NTC7 for MC33775A B1
3	GND_B1	ground for MC33775A B1
4	B1_NTC6	temperature measurement; NTC6 for MC33775A B1
5	GND_B1	ground for MC33775A B1
6	B1_NTC2	temperature measurement; NTC2 for MC33775A B1
7	GND_B1	ground for MC33775A B1
8	B1_NTC1	temperature measurement; NTC1 for MC33775A B1
9	GND_B1	ground for MC33775A B1
10	GND_B1	ground for MC33775A B1
11	B1_C1P	cell 1 positive for MC33775A B1
12	B1_C1M	cell 1 negative for MC33775A B1
13	B1_C3P	cell 3 positive for MC33775A B1
14	B1_C2P	cell 2 positive for MC33775A B1
15	B1_C5P	cell 5 positive for MC33775A B1
16	B1_C4P	cell 4 positive for MC33775A B1
17	B1_C7P	cell 7 positive for MC33775A B1
18	B1_C6P	cell 6 positive for MC33775A B1
19	B1_C9P	cell 9 positive for MC33775A B1
20	B1_C8P	cell 8 positive for MC33775A B1
21	B1_C11P	cell 11 positive for MC33775A B1
22	B1_C10P	cell 10 positive for MC33775A B1
23	B1_C13P	cell 13 positive for MC33775A B1

Table 4. Cell terminal and temperature - J1*...continued*

Pin number	Connection	Description
24	B1_C12P	cell 12 positive for MC33775A B1
25	B1_C14P-PWR	power for MC33775A B1
26	B1_C14P	cell 14 positive for MC33775A B1

Table 5. Cell terminal and temperature - J34

Pin number	Connection	Description
1	GND_B2	ground for MC33775A B2
2	B2_NTC7	temperature measurement; NTC7 for MC33775A B2
3	GND_B2	ground for MC33775A B2
4	B2_NTC6	temperature measurement; NTC6 for MC33775A B2
5	GND_B2	ground for MC33775A B2
6	B2_NTC2	temperature measurement; NTC2 for MC33775A B2
7	GND_B2	ground for MC33775A B2
8	B2_NTC1	temperature measurement; NTC1 for MC33775A B2
9	GND_B2	ground for MC33775A B2
10	GND_B2	ground for MC33775A B2
11	B2_C1P	cell 1 positive for MC33775A B2
12	B2_C1M	cell 1 negative for MC33775A B2
13	B2_C3P	cell 3 positive for MC33775A B2
14	B2_C2P	cell 2 positive for MC33775A B2
15	B2_C5P	cell 5 positive for MC33775A B2
16	B2_C4P	cell 4 positive for MC33775A B2
17	B2_C7P	cell 7 positive for MC33775A B2
18	B2_C6P	cell 6 positive for MC33775A B2
19	B2_C9P	cell 9 positive for MC33775A B2
20	B2_C8P	cell 8 positive for MC33775A B2
21	B2_C11P	cell 11 positive for MC33775A B2
22	B2_C10P	cell 10 positive for MC33775A B2
23	B2_C13P	cell 13 positive for MC33775A B2
24	B2_C12P	cell 12 positive for MC33775A B2
25	B2_C14P-PWR	power for MC33775A B2
26	B2_C14P	cell 14 positive for MC33775A B2

Table 6. Cell terminal and temperature - J35

Pin number	Connection	Description
1	GND_B3	ground for MC33775A B3
2	B3_NTC7	temp - NTC7 for MC33775A B3
3	GND_B3	ground for MC33775A B3
4	B3_NTC6	temp - NTC6 for MC33775A B3
5	GND_B3	ground for MC33775A B3
6	B3_NTC2	temp - NTC2 for MC33775A B3
7	GND_B3	ground for MC33775A B3
8	B3_NTC1	temp - NTC1 for MC33775A B3
9	GND_B3	ground for MC33775A B3
10	GND_B3	ground for MC33775A B3
11	B3_C1P	cell 1 positive for MC33775A B3
12	B3_C1M	cell 1 negative for MC33775A B3
13	B3_C3P	cell 3 positive for MC33775A B3
14	B3_C2P	cell 2 positive for MC33775A B3
15	B3_C5P	cell 5 positive for MC33775A B3
16	B3_C4P	cell 4 positive for MC33775A B3
17	B3_C7P	cell 7 positive for MC33775A B3
18	B3_C6P	cell 6 positive for MC33775A B3
19	B3_C9P	cell 9 positive for MC33775A B3
20	B3_C8P	cell 8 positive for MC33775A B3
21	B3_C11P	cell 11 positive for MC33775A B3
22	B3_C10P	cell 10 positive for MC33775A B3
23	B3_C13P	cell 13 positive for MC33775A B3
24	B3_C12P	cell 12 positive for MC33775A B3
25	B3_C14P-PWR	power for MC33775A B3
26	B3_C14P	cell 14 positive for MC33775A B3

Table 7. Cell terminal and temperature - J36

Pin number	Connection	Description
1	GND_B4	ground for MC33775A B4
2	B4_NTC7	temp - NTC7 for MC33775A B4
3	GND_B4	ground for MC33775A B4
4	B4_NTC6	temp - NTC6 for MC33775A B4
5	GND_B4	ground for MC33775A B4
6	B4_NTC2	temp - NTC2 for MC33775A B4
7	GND_B4	ground for MC33775A B4

Table 7. Cell terminal and temperature - J36*...continued*

Pin number	Connection	Description
8	B4_NTC1	temp - NTC1 for MC33775A B4
9	GND_B4	ground for MC33775A B4
10	GND_B4	ground for MC33775A B4
11	B4_C1P	cell 1 positive for MC33775A B4
12	B4_C1M	cell 1 negative for MC33775A B4
13	B4_C3P	cell 3 positive for MC33775A B4
14	B4_C2P	cell 2 positive for MC33775A B4
15	B4_C5P	cell 5 positive for MC33775A B4
16	B4_C4P	cell 4 positive for MC33775A B4
17	B4_C7P	cell 7 positive for MC33775A B4
18	B4_C6P	cell 6 positive for MC33775A B4
19	B4_C9P	cell 9 positive for MC33775A B4
20	B4_C8P	cell 8 positive for MC33775A B4
21	B4_C11P	cell 11 positive for MC33775A B4
22	B4_C10P	cell 10 positive for MC33775A B4
23	B4_C13P	cell 13 positive for MC33775A B4
24	B4_C12P	cell 12 positive for MC33775A B4
25	B4_C14P-PWR	power for MC33775A B4
26	B4_C14P	cell 14 positive for MC33775A B4

Table 8. Daisy chain TPL port 0 extension - J30

Pin number	Connection	Description
1	RDTXP_B4	daisy chain port 0 extension; RDTX positive from B4
2	RDTXN_B4	daisy chain port 0 extension; RDTX negative from B4

4 Configuring the hardware

4.1 Test setup

RD33775ACNCEVB can be used in different setup configurations to check the performance of MC33665A and MC33775A. Figure 6 is a minimal hardware setup to check most of the functions and features built in RD33775ACNCEVB. The BATT-14CEMULATOR board can emulate a multi-cell (14 cells) battery pack that can be easily connected to evaluation boards from NXP (check BMS connector pin configuration). The BATT-14EXTENDER allows for the connection up to four evaluation boards using only one single battery emulator. Cell terminal and temperature (J1, J34, J35, J36) interface cable from RD33775ACNCEVB are compatible to BATT-EXTENDER and BATT-14CEMULATOR.

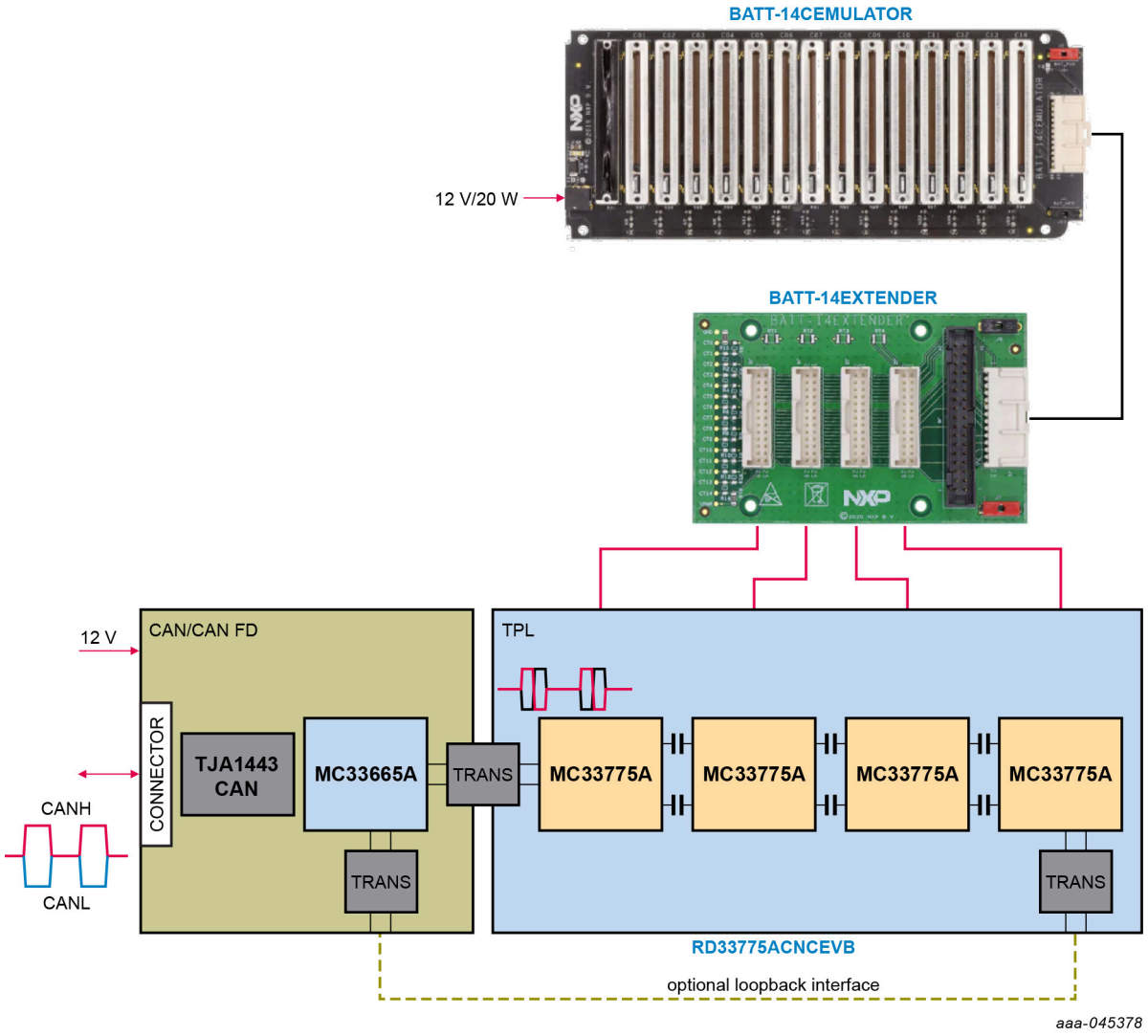

Figure 6. RD33775ACNCEVB test setup

J25 connector can be used to power MC33665A and communicate with CAN or CAN FD to RD33775ACNCEVB. CAN tools can be interfaced to J25 for establishing CAN or CAN FD communication with RD33775ACNCEVB.

- Set up the communication to RD33775ACNCEVB using the data sheets of MC33665A and MC33775A.
- Set the CFG0, CFG1, ID0_STB_OD, ID1, ID2, and ID3 based on external CAN (FD) communication.
- Based on test requirements, external MC33775A BCC devices can be connected to RD33775ACNCEVB.
  - Connect to J30 as extension to daisy chain port 0 from fourth MC33775A
  - Connect to J2 as second daisy chain of MC33775A BCC devices to daisy chain port 1 of MC33665A
- External MC33771C/MC33772C can be connected to J2 as interface to daisy chain port 1 of MC33665A. Note: MC33771C/MC33772C BCC devices from NXP should not be connected to J30.

- Connect 12 V to BATT-14CEMULATOR and RD33775ACNCEVB after crosschecking the interface connections and boards based on test plan.

5 Available accessories

Table 9. Accessories

Part number	Description
BATT-14EXTENDER	battery emulator extender
BATT-14CEMULATOR	14-cell battery pack to supply MC33771C EVBs
BATT-TPLCABLE20	TPL, two-wire, twisted, 20 cm long cable
BATT-TPLCABLE50	TPL, two-wire, twisted, 50 cm long cable
BATT-14CTCABLE25	cell terminal (CT) cable, 14 cells, 25 cm long

6 Legal information

6.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Safety of high-voltage evaluation products — The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits.

The product does not comply with IEC 60950 based national or regional safety standards. NXP Semiconductors does not accept any liability for damages incurred due to inappropriate use of this product or related to non-insulated high voltages. Any use of this product is at customer's own risk and liability. The customer shall fully indemnify and hold harmless NXP Semiconductors from any liability, damages and claims resulting from the use of the product.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

6.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com

Date of release: 25 August 2022
Document identifier: UM11746