MPQ5850

36V, Smart Diode Controller with Reverse Protection, AEC-Q100 Qualified

DESCRIPTION

The MPQ5850 is a smart diode controller that can drive an external N-channel MOSFET to replace a Schottky diode for reverse input protection. The device's 20mV ultra-low dropout minimizes power loss and enables a low minimum input voltage, which makes the MPQ5850 well-suited for cold-crank conditions in automotive applications. The 4µA shutdown current also makes the device ideal for battery-powered applications. The ultra-fast transient response meets stringent ISO16750 requirements.

The MPQ5850 integrates an internal boost to provide a boost voltage that turns on the external N-channel MOSFET, even at a low input voltage (V_{IN}). An open-drain, power good signal indicates when the external N-channel MOSFET is fully on.

The MPQ5850 is available in a TSOT23-8 (2mmx3mm) package.

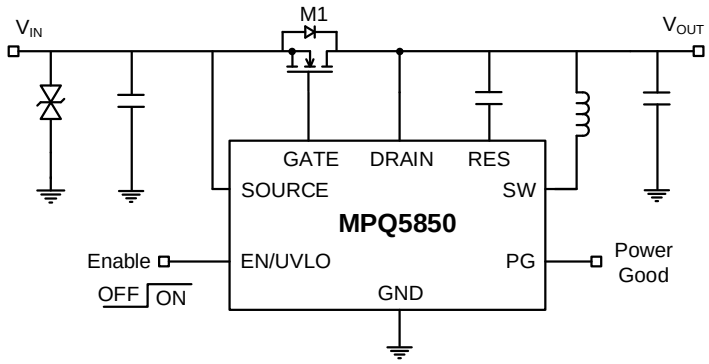
FEATURES

- Built to Handle Tough Automotive Transients:
  - -36V Blocking Voltage
  - Load Dump Up to 42V
  - Cold Crank Down to 0V
  - Rectifies AC Frequency Up to 100kHz
  - Strong Gate Drive Ability: 170mA Pull-Up and 430mA Pull-Down
- Extended Vehicle Battery Life:
  - Low Quiescent Current in Standby Mode (4µA)
  - Low Quiescent Current in Steady State (30µA)
- Reduced Board Size:
  - Available in a TSOT23-8 (2mmx3mm) Package
- Additional Features:
  - 20mV Ultra-Low Dropout
  - Integrates a Boost Converter
  - Power Good (PG) Indication for RES Out of Regulation, Fast Pull-Up, and Part Disabling
  - Available in AEC-Q100 Grade 1

APPLICATIONS

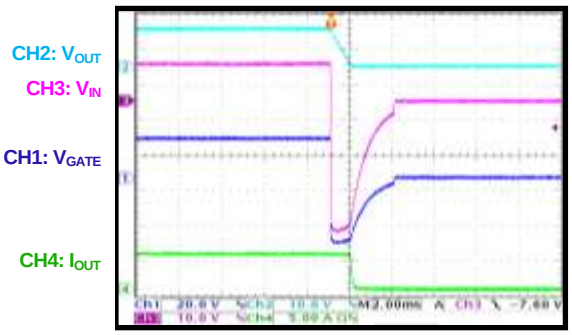
- Automotive System Protection
- Automotive ADAS Systems (Cameras)
- Automotive Infotainment Systems, Including Digital Clusters and Head Units
- Battery-Powered Systems

TYPICAL APPLICATION



Negative Pulse

I_{OUT} = 5A



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ5850GJ MPQ5850GJ-AEC1	TSOT23-8 (2mmx3mm)	*See Below*	Level 1

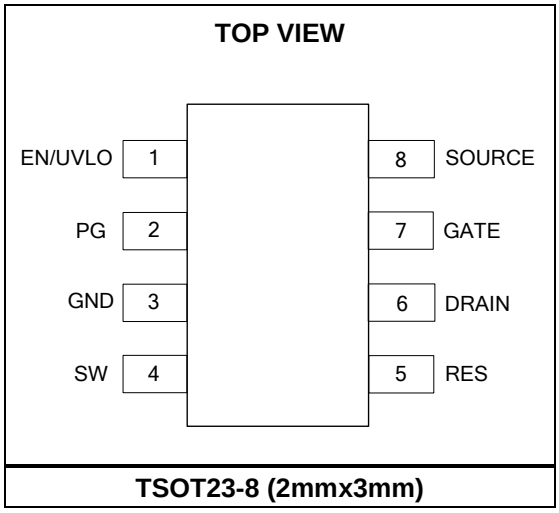
* For Tape & Reel, add suffix -Z (e.g. MPQ5850GJ-Z).
** Moisture Sensitivity Level Rating

TOP MARKING (MPQ5850GJ & MPQ5850GJ-AEC1)

BNNY

BNN: Product code of MPQ5850GJ and MPQ5850GJ-AEC1
Y: Year code

PACKAGE REFERENCE



TSOT23-8 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN/UVLO	**Enable pin.** Pull EN below the specified threshold (1V) to shut down the chip. Pull EN above the threshold (1.2V) to enable the chip. A resistor divider connected between EN/UVLO and SOURCE can be used to raise the under-voltage lockout (UVLO) threshold. Do not float the EN/UVLO pin, and connect it to DRAIN if the shutdown feature not used.
2	PG	**Open-drain power good pin.** The PG pin asserts low if the device is disabled, the reservoir supply is out of regulation, or if the fast pull-up path is active for longer than 17µs. Float PG or connect it to GND if it is not used.
3	GND	**Ground connection of the device.** Connect GND to the ground plane of the board.
4	SW	**Switch node of internal boost regulator.** Connect an inductor between the SW and DRAIN pins.
5	RES	**Reservoir supply.** RES is the power supply for the external N-channel MOSFET gate driver. Connect a minimum 1µF ceramic capacitor between the RES and DRAIN pins.
6	DRAIN	**Drain connection.** Connect the DRAIN pin to the drain of the external power MOSFET. DRAIN is the power supply of the internal circuitry, and also controls the MOSFET's gate voltage. Connect a minimum 4.7µF capacitor from DRAIN to ground, and place this capacitor as close as possible to the device.
7	GATE	**Gate connection.** Connect the GATE pin to the gate of the external power MOSFET.
8	SOURCE	**Source connection.** Connect the SOURCE pin to the source of the external power MOSFET. The voltage sensed on this pin works with the DRAIN voltage to control the MOSFET gate.

ABSOLUTE MAXIMUM RATINGS (1)

SOURCE, EN/UVLO ..... -36V to +42V
DRAIN ..... -0.3V to +42V
DRAIN - SOURCE ..... -2V to +52V
GATE - SOURCE ..... -0.3V to +13V
RES ..... -0.3V to V_{DRAIN} + 13V
SW ..... -0.3V to +57V
PG ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
TSOT23-8 (2mmx3mm) 1.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) ..... Class 2 (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 36V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

TSOT23-8 (2mmx3mm)
JESD51-7 (5) ..... 85 ..... 20 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{SOURCE} = $V_{EN/UVLO}$ = 12V, V_{RES} = 22V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage						
Drain voltage at start-up	V_{DRAIN_UVLO}			2.8	3.2	V
Drain voltage UVLO falling	$V_{DRAIN\_UVLO\_F}$		2.4	2.6	2.8	V
Reservoir UVLO rising	V_{RES_UVLO}		8	11	13	V
Reservoir UVLO hysteresis	$V_{RES\_UVLO\_HYS}$			0.2		V
Quiescent current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		4	10	µA
		V_{EN} = 0V, T_J = -40°C to +150°C			20	µA
	I_Q	V_{EN} = 2V, in regulation, system input current, T_J = 25°C		30	50	µA
		V_{EN} = 2V, in regulation, system input current, T_J = -40°C to +125°C (6)			100	µA
		V_{EN} = 2V, in regulation, system input current, T_J = 125°C to 150°C			200	µA
Rectifier						
Source to drain regulation voltage	V_{SD}		10	20	30	mV
Source to drain fast pull-up threshold	V_{SD_FPU}		50	75	100	mV
Source to drain fast pull-down threshold	V_{SD_FPD}		-15	-4	0	mV
Drain current	I_D	Gate driver in regulation		50		µA
Source current	I_{S_R}	V_{SOURCE} = -36V			-1	mA
Fast pull up current	I_{FPU}	$V_{GATE-RES}$ = -7V	170			mA
Fast pull down current	I_{FPD}	$V_{GATE-SOURCE}$ = 5V	430			mA
Reverse biased gate-source voltage	V_{GS_RB}	V_{SOURCE} = -5V, I_{GATE} = 1mA		0.01	0.3	V
		V_{SOURCE} = -36V, I_{GATE} = 1mA		0.01	0.3	V
Gate turn-on delay time	t_{ON}	Step (V_{SOURCE} - V_{DRAIN}) from -100mV to +3V, $V_{RES-DRAIN}$ = 13V, $C_{GATE-SOURCE}$ = 10nF		1.2	2	µs
Gate turn-off delay time	t_{OFF}	Step (V_{SOURCE} - V_{DRAIN}) from 3V to -100mV, $V_{RES-DRAIN}$ = 13V, $C_{GATE-SOURCE}$ = 10nF		1	2	µs
Gate rising time	t_{RISING} (6)	Step (V_{SOURCE} - V_{DRAIN}) from -100mV to +3V, $V_{RES-DRAIN}$ = 13V, $C_{GATE-SOURCE}$ = 10nF		300		ns
Gate falling time	$t_{FALLING}$ (6)	Step (V_{SOURCE} - V_{DRAIN}) from 3V to -100mV, $V_{RES-DRAIN}$ = 13V, $C_{GATE-SOURCE}$ = 10nF		100		ns
Maximum rectification frequency (6)	f_{MAX}	V_{PP} = 6V, $C_{GATE-SOURCE}$ = 15nF	50			kHz
		V_{PP} = 2V, $C_{GATE-SOURCE}$ = 15nF	100			

ELECTRICAL CHARACTERISTICS *(continued)*

V_{SOURCE} = $V_{EN/UVLO}$ = 12V, V_{RES} = 22V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Boost Converter						
Reservoir regulation voltage	V_{REG}		10	12	14	V
Reservoir regulation UVLO hysteresis	$V_{REG\_UVLO\_HYS}$	V_{REG} - V_{RES_UVLO} - $V_{RES\_UVLO\_HYS}$		1.2		V
Boost current limit	I_{BOOST}		160	220	280	mA
SW leakage	I_{SW}				1	µA
Boost power switch on resistance	R_{SW}			1.5	3.5	Ω
Boost rectifier diode voltage drop	V_{DIODE}	I_{DIODE} = 220mA		0.9		V
Enable Pin						
Enable threshold rising	V_{EN}		1.0	1.2	1.4	V
Enable threshold falling	V_{EN_F}		0.8	1	1.2	V
Enable hysteresis	V_{EN_H}			200		mV
Enable leakage	I_{EN}	V_{EN} = 3V			1	µA
Power Good Flag						
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
Thermal shutdown (6)	T_{SD}			175		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			25		°C

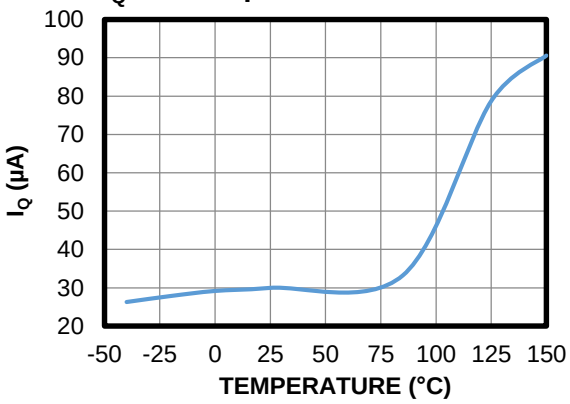
Note:

6) Derived from bench characterization. Not tested in production.

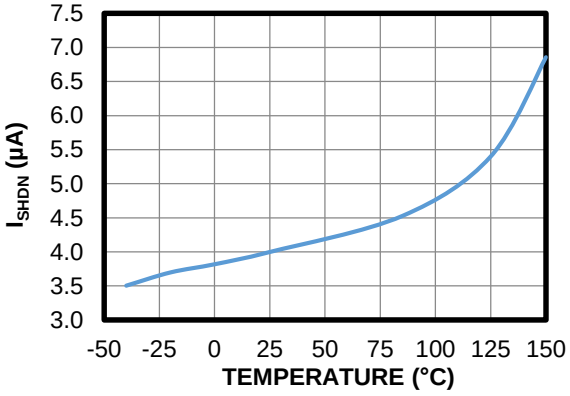
TYPICAL CHARACTERISTICS

V_{IN} = 12V, L = 68µH, T_J = -40°C to +150°C, unless otherwise noted.

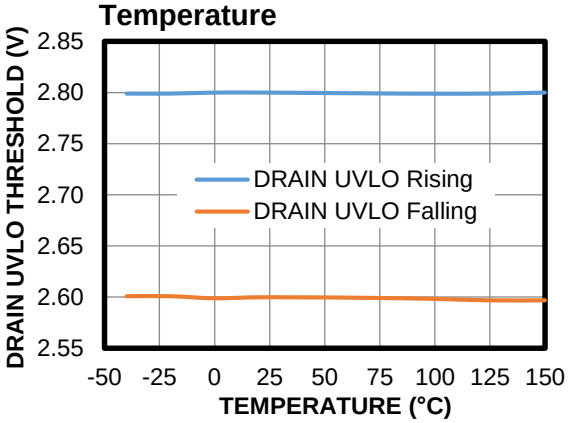
I_Q vs. Temperature



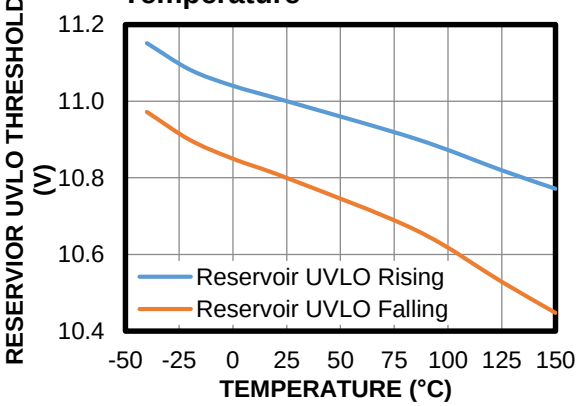
I_{SHDN} vs. Temperature



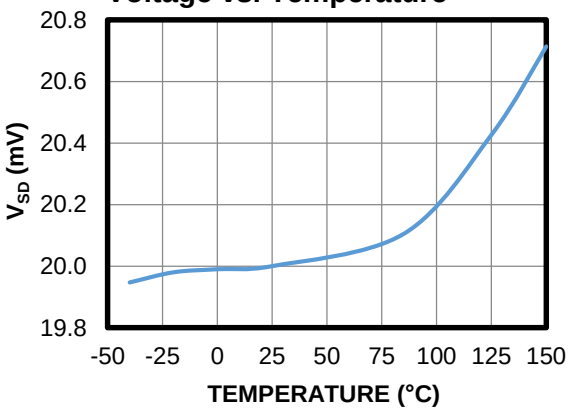
Drain UVLO Threshold vs. Temperature



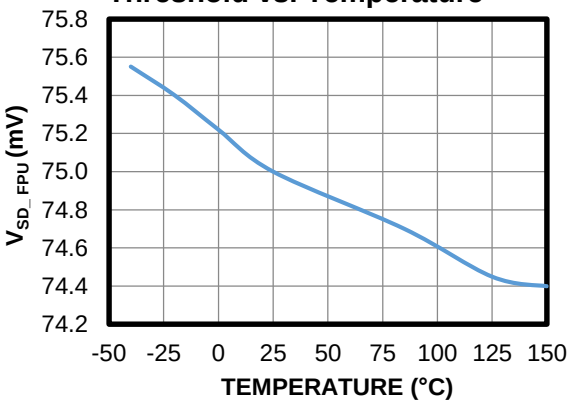
Reservoir UVLO Threshold vs. Temperature



Source to Drain Regulation Voltage vs. Temperature



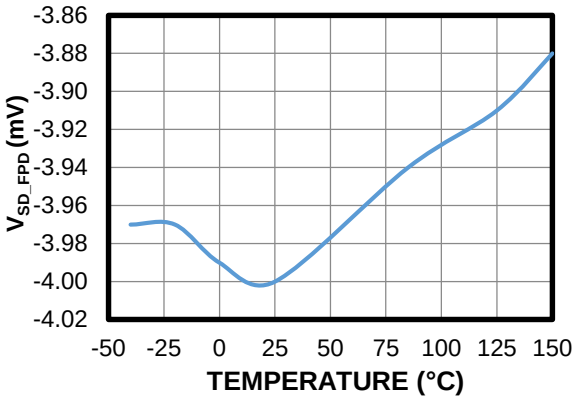
Source to Drain Fast Pull-Up Threshold vs. Temperature



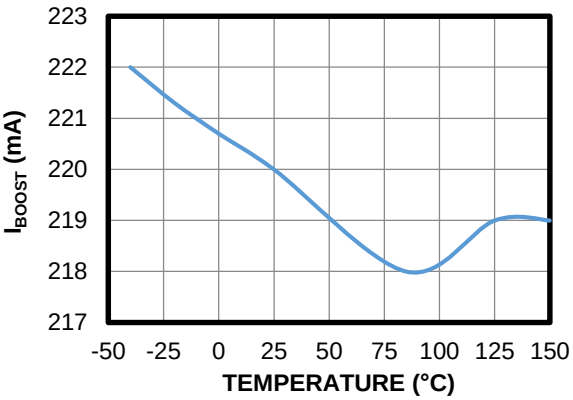
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 68µH, T_J = -40°C to +150°C, unless otherwise noted.

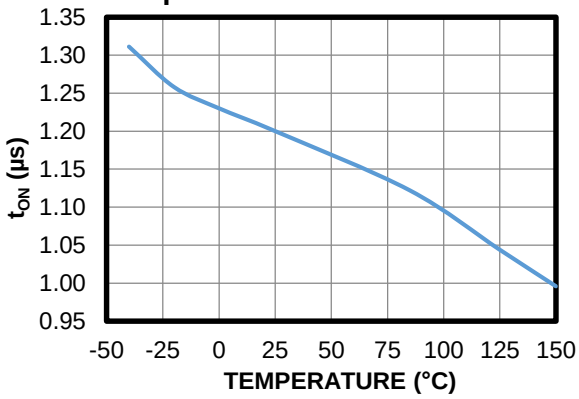
Source to Drain Fast Pull- Down Threshold vs. Temperature



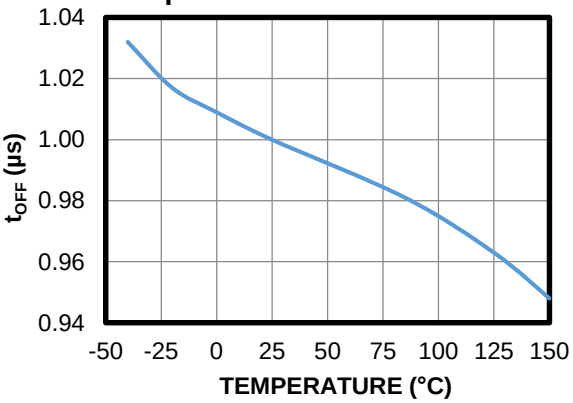
Boost Current Limit vs. Temperature



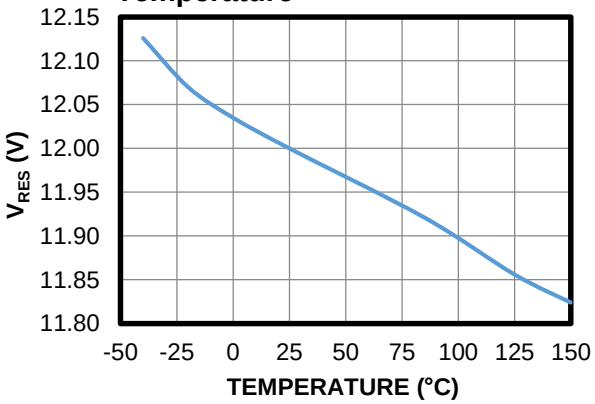
Gate Turn-On Delay Time vs. Temperature



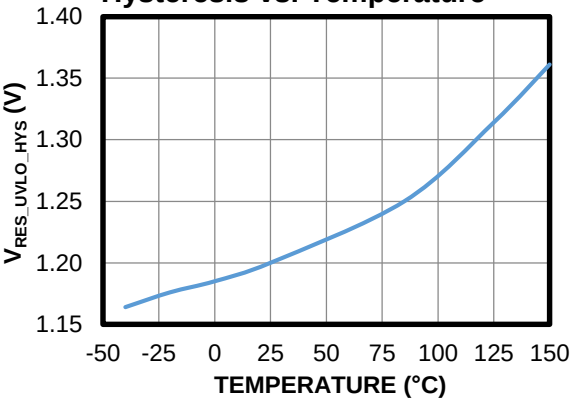
Gate Turn-Off Delay Time vs. Temperature



Reservoir Regulation Voltage vs. Temperature

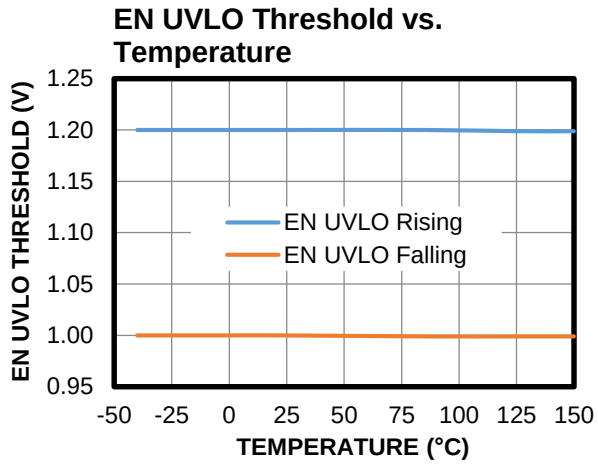


Reservoir Regulation UVLO Hysteresis vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

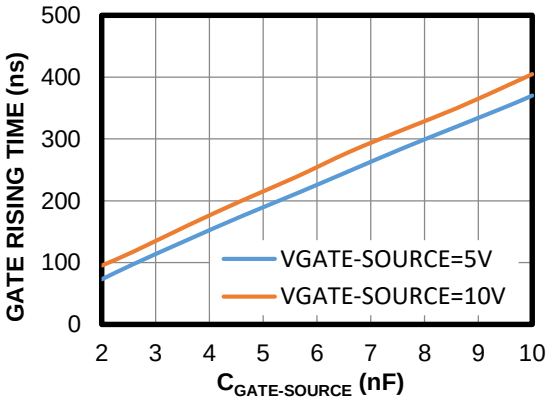
V_{IN} = 12V, L = 68µH, T_J = -40°C to +150°C, unless otherwise noted.



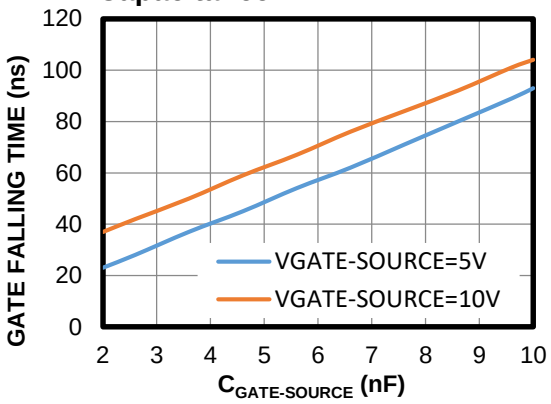
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

Gate Rising Time vs. Gate Capacitance



Gate Falling Time vs. Gate Capacitance

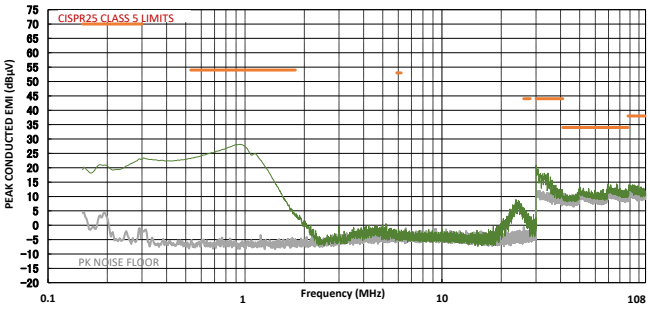


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, C_{OUT} = 470µF, T_A = 25°C, unless otherwise noted. (7)

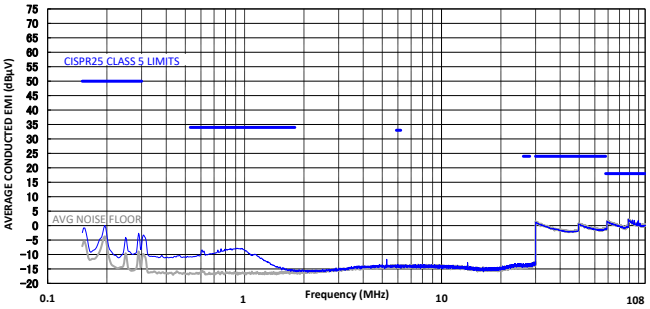
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



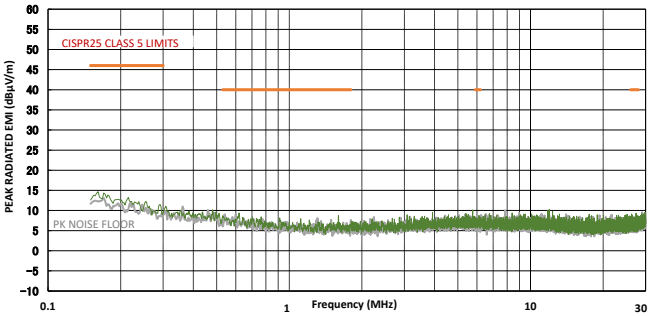
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



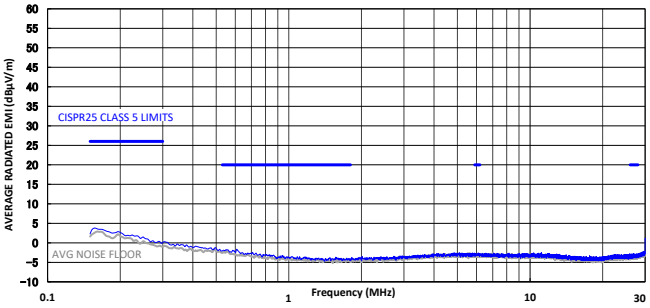
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



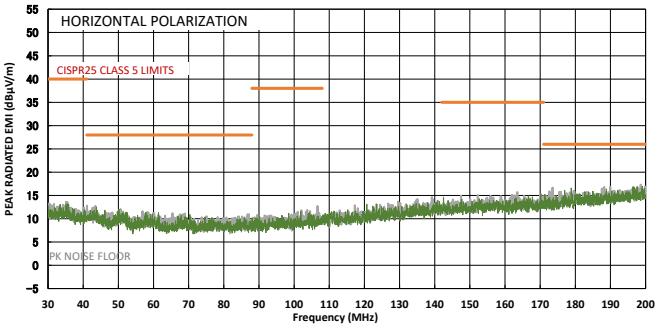
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



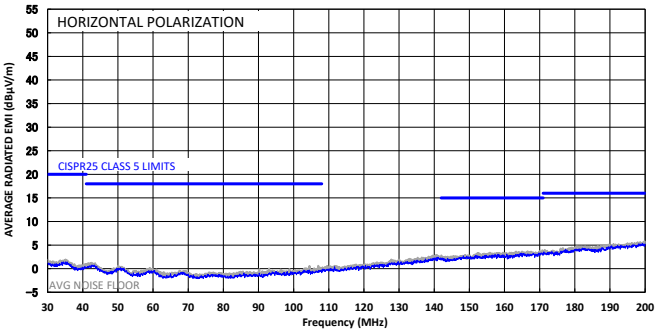
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

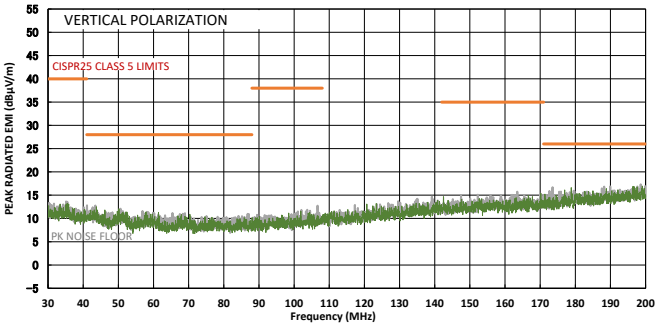


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, C_{OUT} = 470uF, T_A = 25°C, unless otherwise noted. (7)

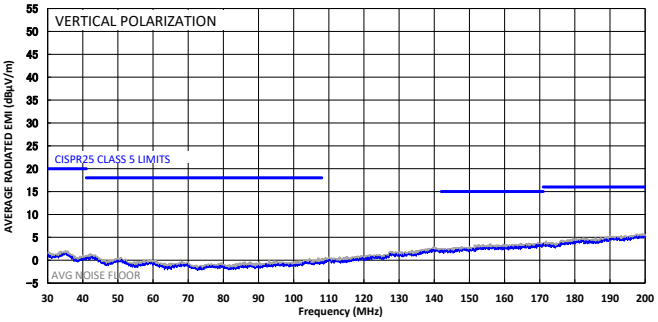
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



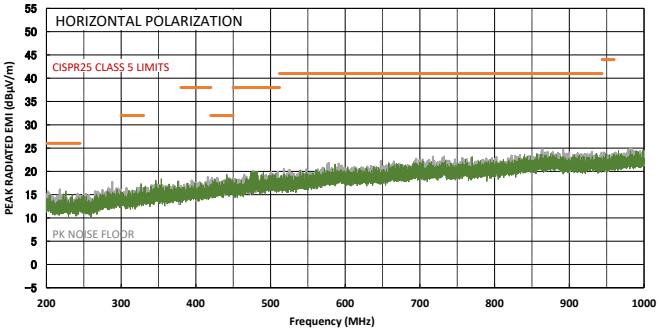
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



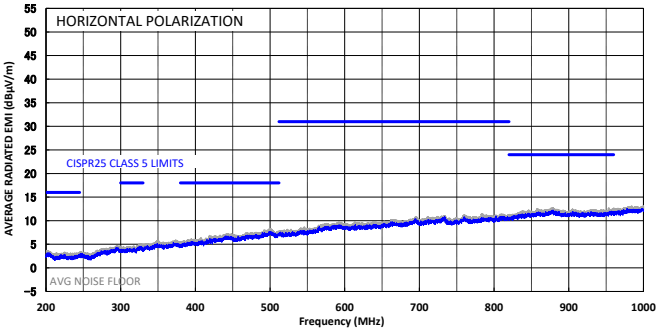
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



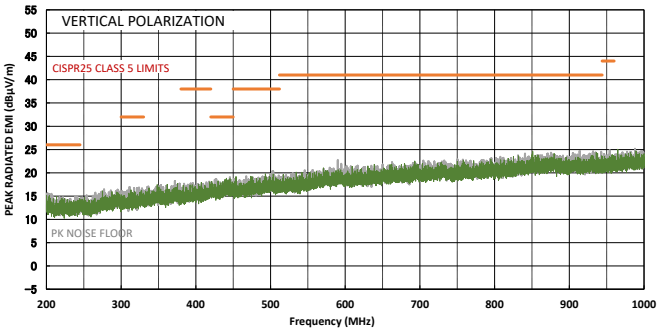
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



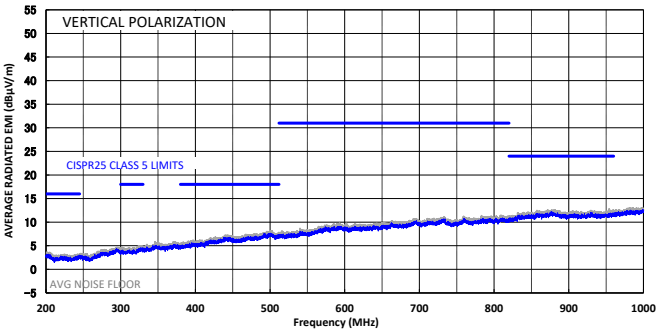
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

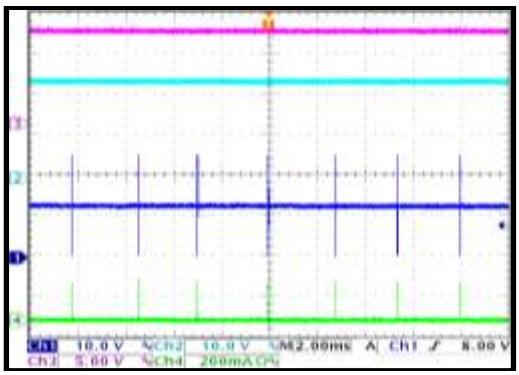
7) The EMC test results are based on the application circuit, and tested on the EVQ5850-J-00A (see Figure 4 on page 26).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

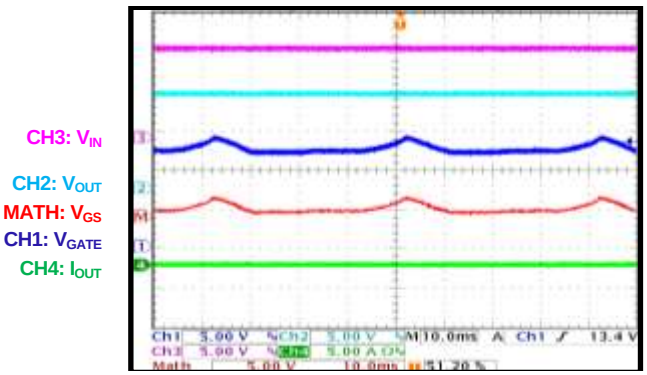
Steady State (for Internal Boost)

I_{OUT} = 0A



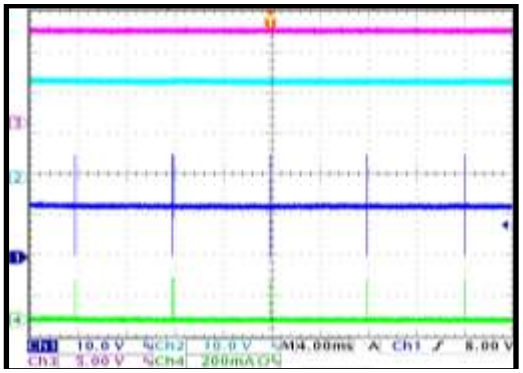
Steady State (for Smart Diode)

I_{OUT} = 0A



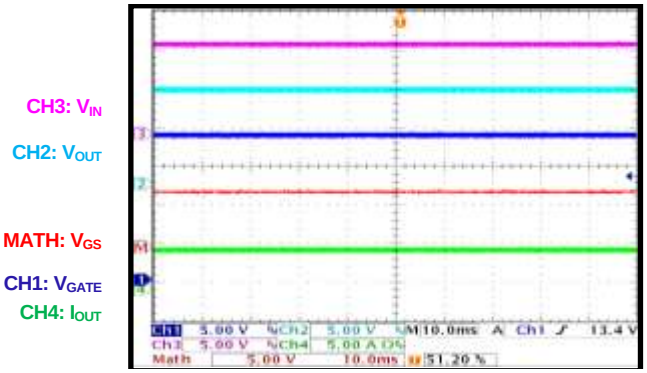
Steady State (for Internal Boost)

I_{OUT} = 5A



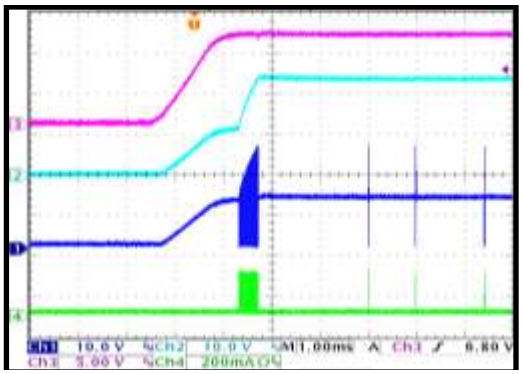
Steady State (for Smart Diode)

I_{OUT} = 5A



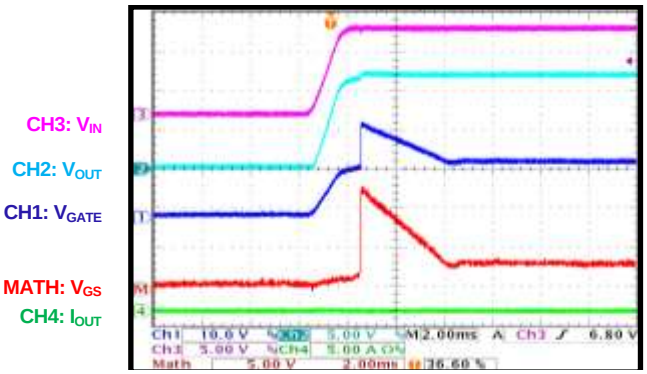
Start-Up through VIN (for Internal Boost)

I_{OUT} = 0A



Start-Up through VIN (for Smart Diode)

I_{OUT} = 0A

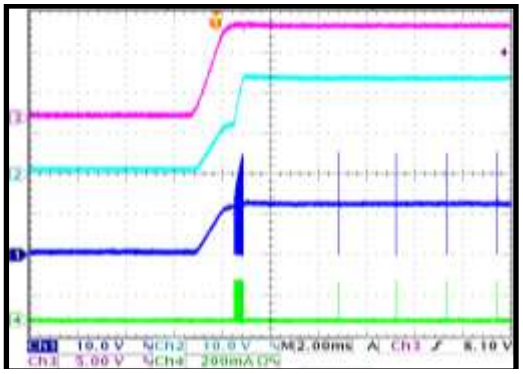


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

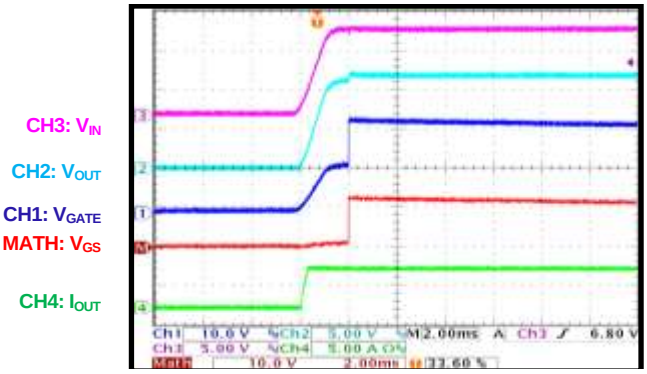
Start-Up through VIN (for Internal Boost)

I_{OUT} = 5A



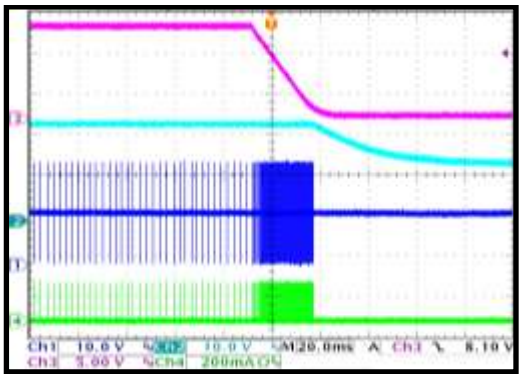
Start-Up through VIN (for Smart Diode)

I_{OUT} = 5A



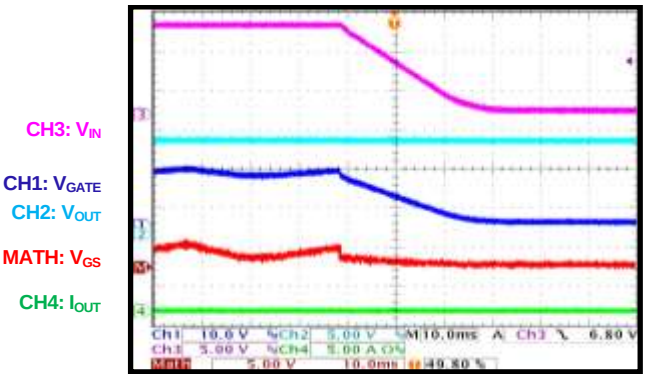
Shutdown through VIN (for Internal Boost)

I_{OUT} = 0A



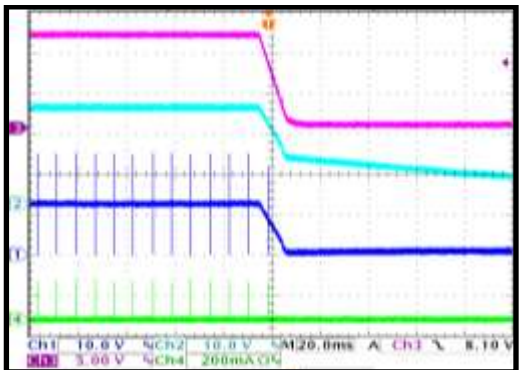
Shutdown through VIN (for Smart Diode)

I_{OUT} = 0A



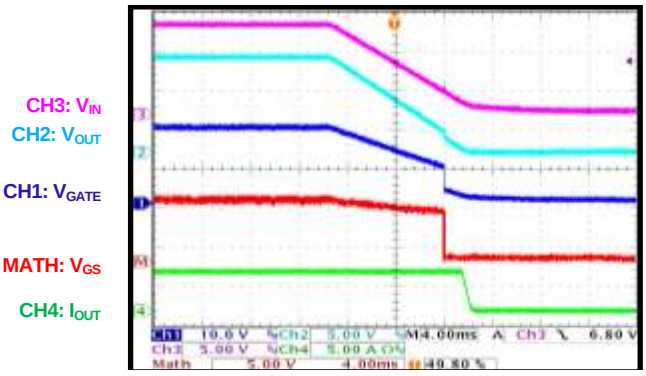
Shutdown through VIN (for Internal Boost)

I_{OUT} = 5A



Shutdown through VIN (for Smart Diode)

I_{OUT} = 5A

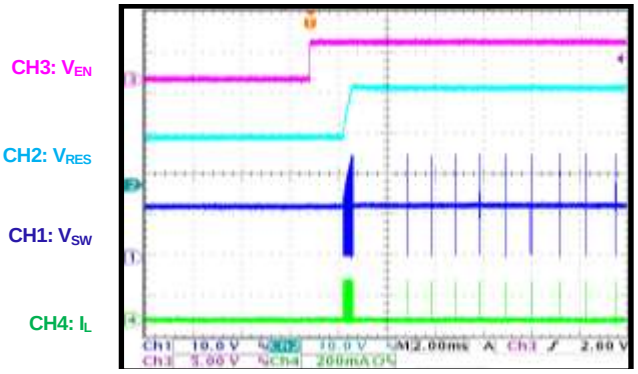


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

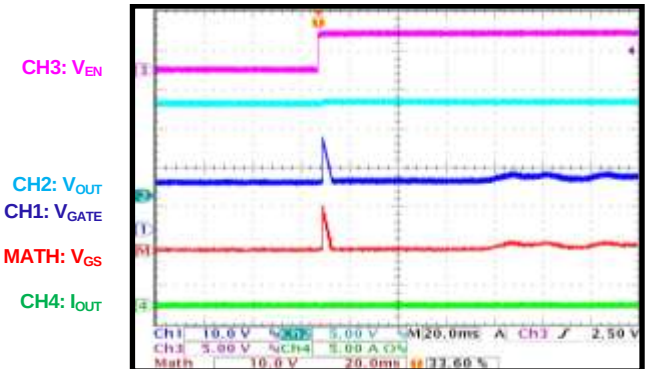
Start-Up through EN (for Internal Boost)

I_{OUT} = 0A



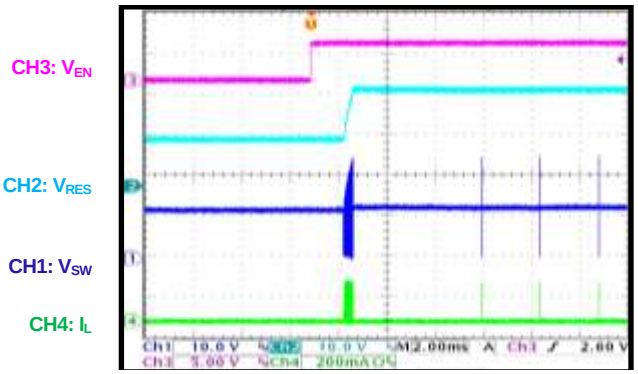
Start-Up through EN (for Smart Diode)

I_{OUT} = 0A



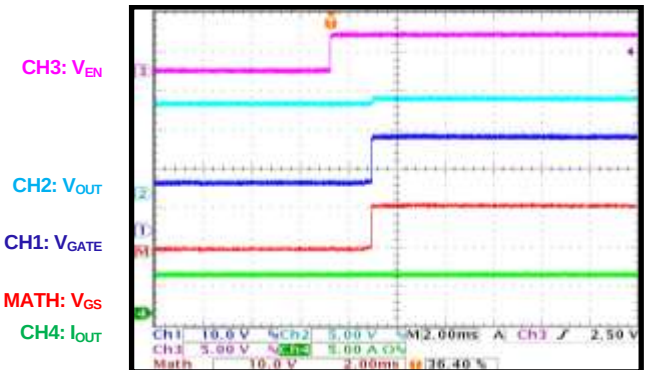
Start-Up through EN (for Internal Boost)

I_{OUT} = 5A



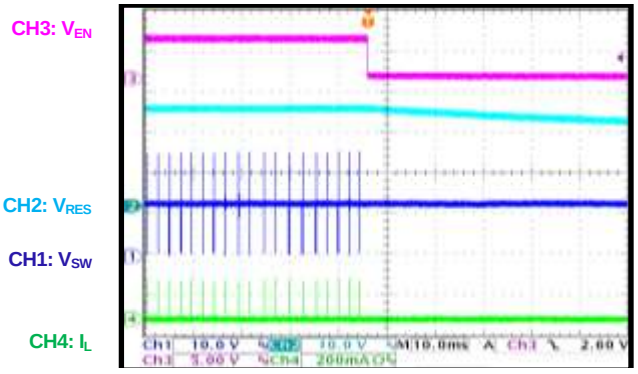
Start-Up through EN (for Smart Diode)

I_{OUT} = 5A



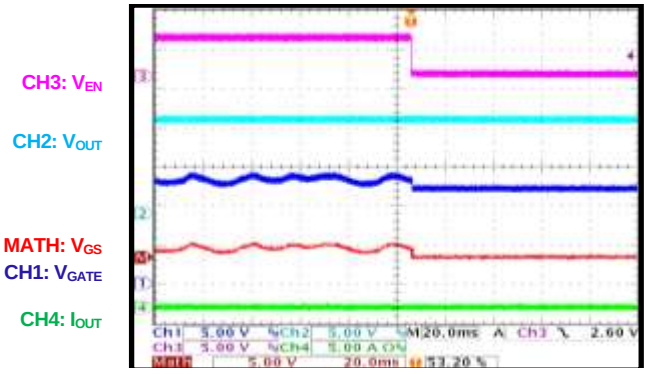
Shutdown through EN (for Internal Boost)

I_{OUT} = 0A



Shutdown through EN (for Smart Diode)

I_{OUT} = 0A

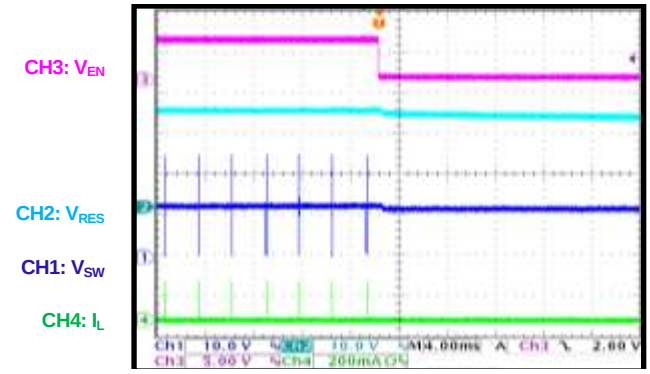


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

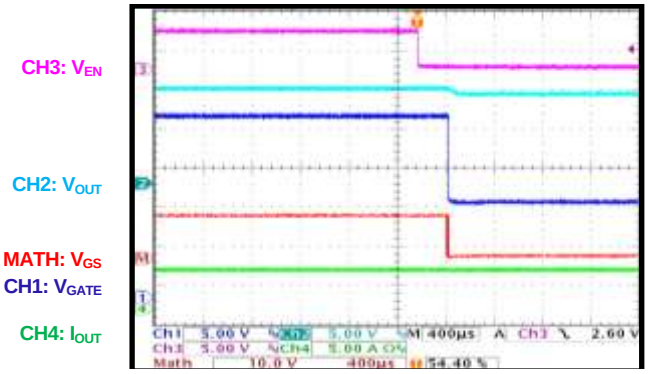
Shutdown through EN (for Internal Boost)

I_{OUT} = 5A



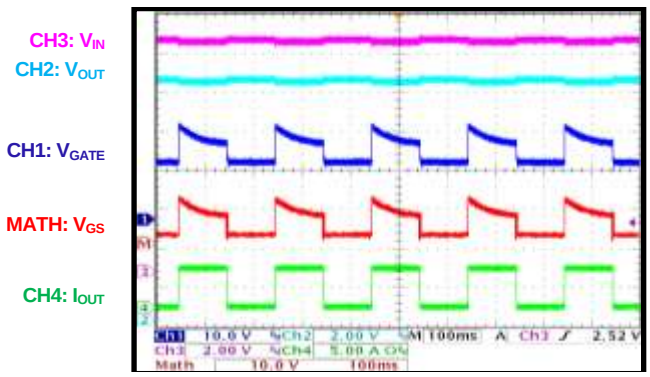
Shutdown through EN (for Smart Diode)

I_{OUT} = 5A



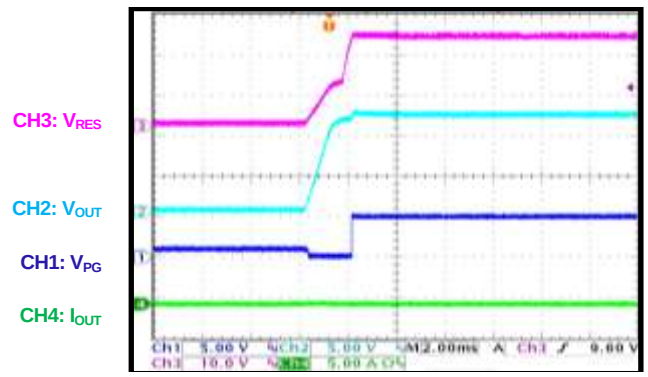
Load Transient

I_{OUT} = 0A to 5A, 6A/µs



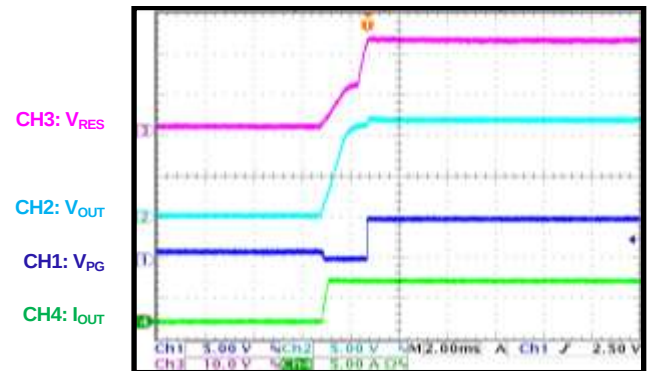
PG Start-Up through VIN

I_{OUT} = 0A



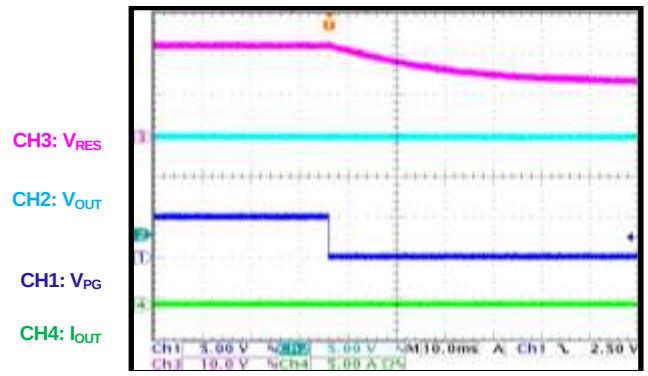
PG Start-Up through VIN

I_{OUT} = 5A



PG Shutdown through VIN

I_{OUT} = 0A

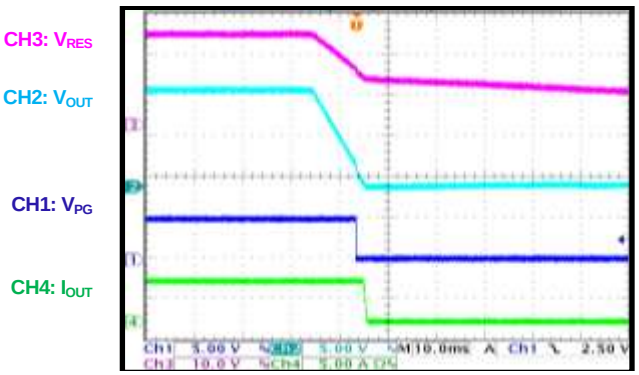


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

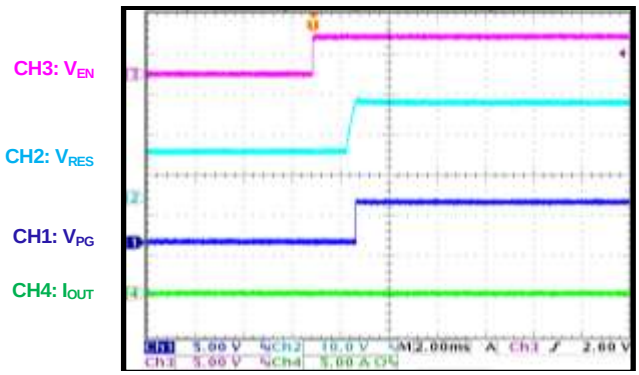
PG Shutdown through VIN

I_{OUT} = 5A



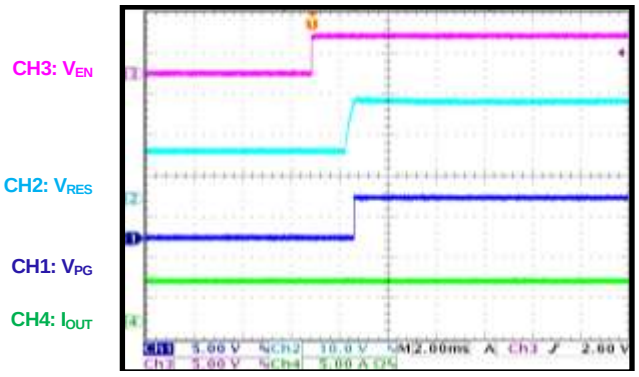
PG Start-Up through EN

I_{OUT} = 0A



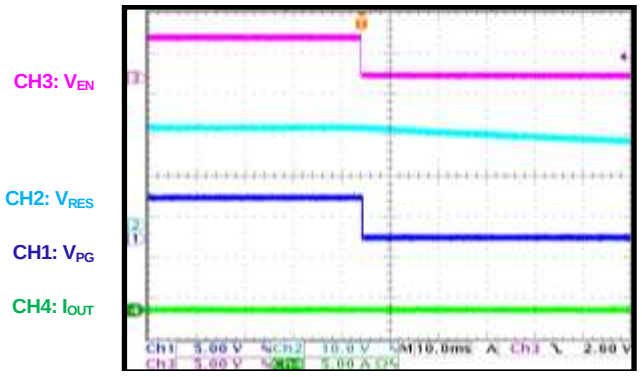
PG Start-Up through EN

I_{OUT} = 5A



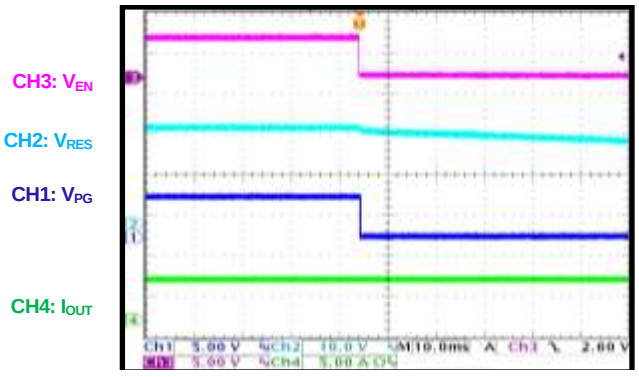
PG Shutdown through EN

I_{OUT} = 0A



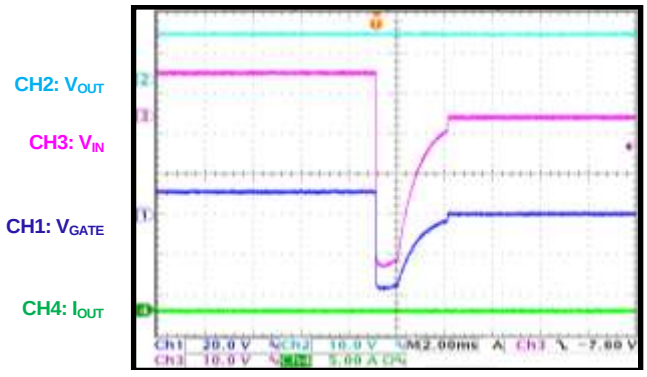
PG Shutdown through EN

I_{OUT} = 5A



Negative Pulse

I_{OUT} = 0A

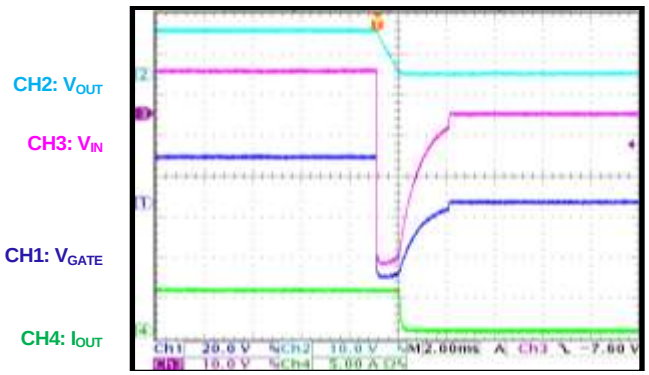


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

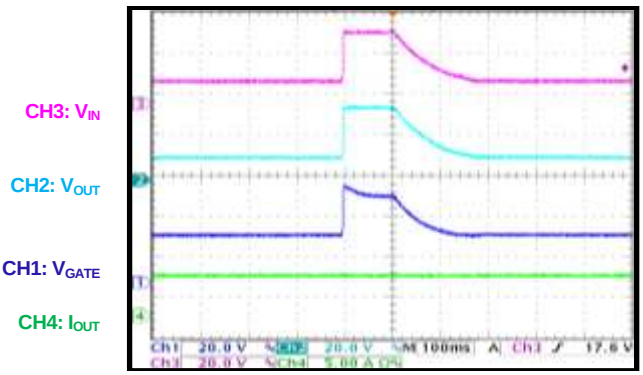
Negative Pulse

I_{OUT} = 5A



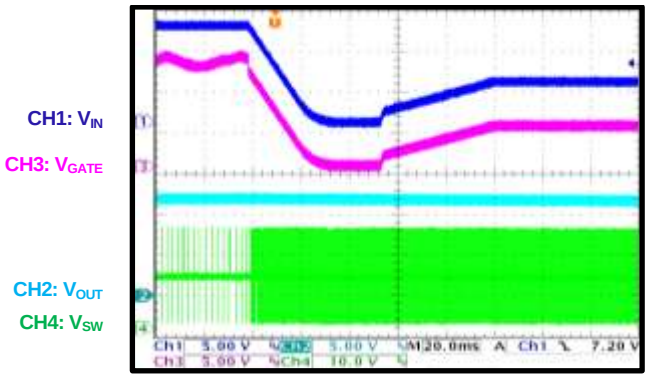
Load Dump

I_{OUT} = 5A



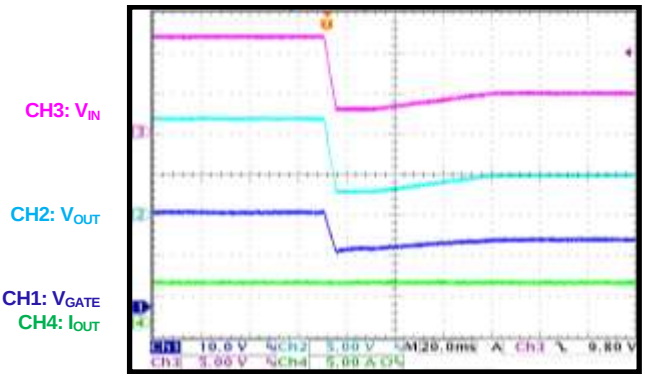
Cold Crank

I_{OUT} = 0A



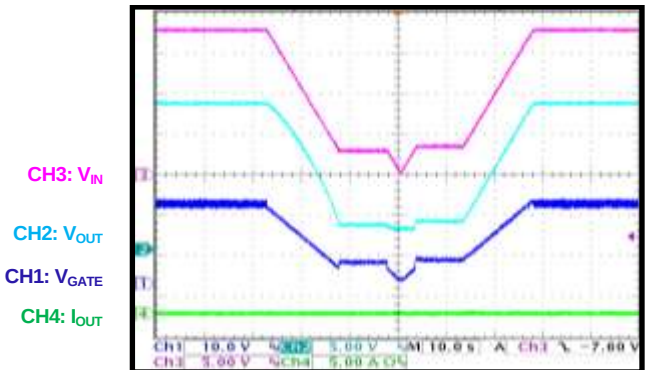
Cold Crank

I_{OUT} = 5A



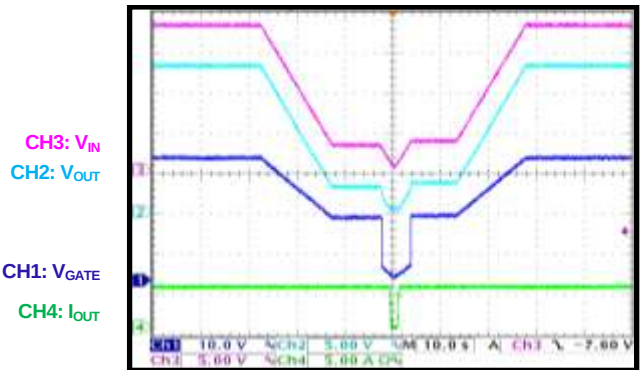
Supply Voltage Ramps Up and Down Slowly

I_{OUT} = 0A



Supply Voltage Ramps Up and Down Slowly

I_{OUT} = 5A

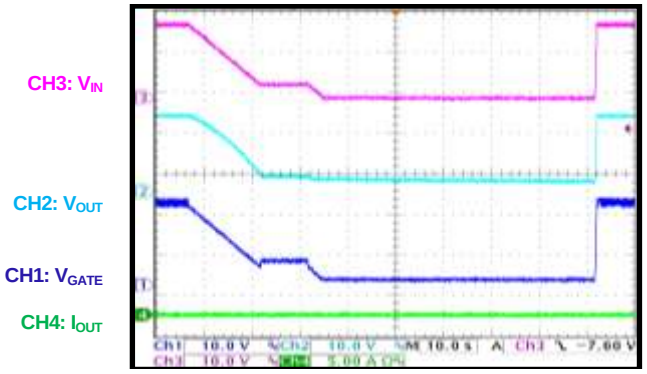


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

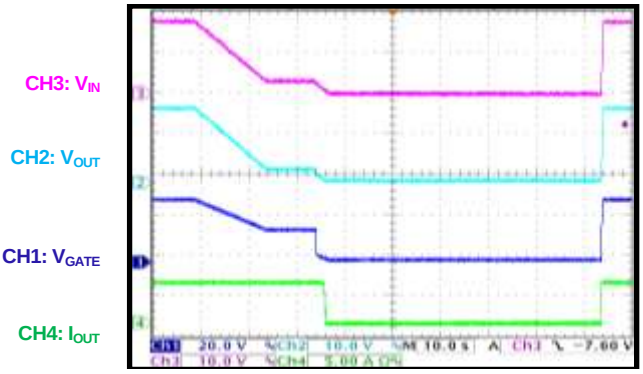
Supply Voltage Ramps Up Quickly and Down Slowly

I_{OUT} = 0A



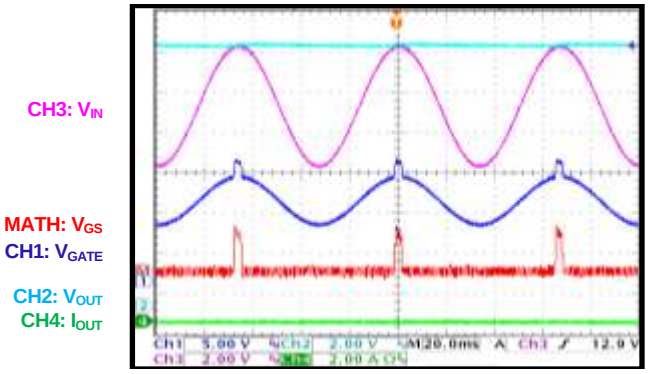
Supply Voltage Ramps Up Quickly and Down Slowly

I_{OUT} = 5A



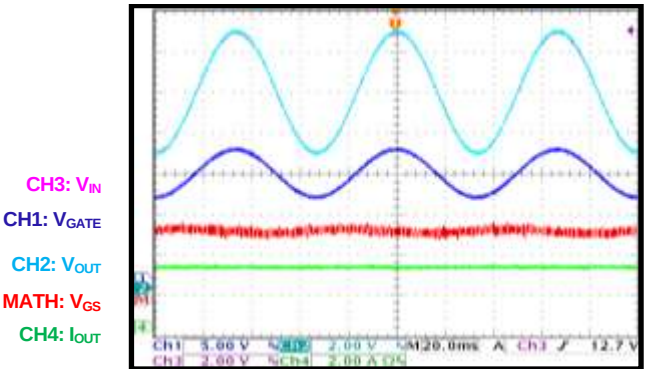
Simultaneous Input

V_{PP} = 6V, f = 15Hz, I_{OUT} = 0A



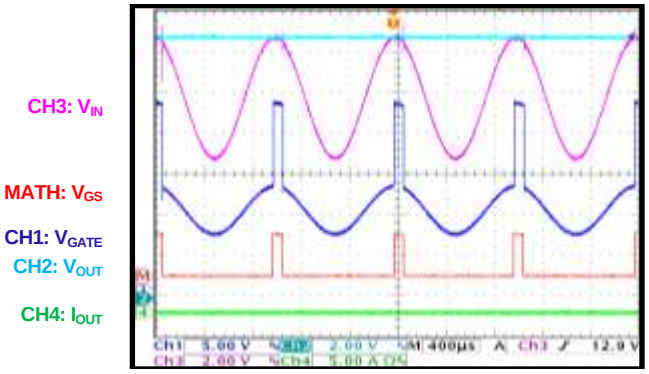
Simultaneous Input

V_{PP} = 6V, f = 1kHz, I_{OUT} = 0A



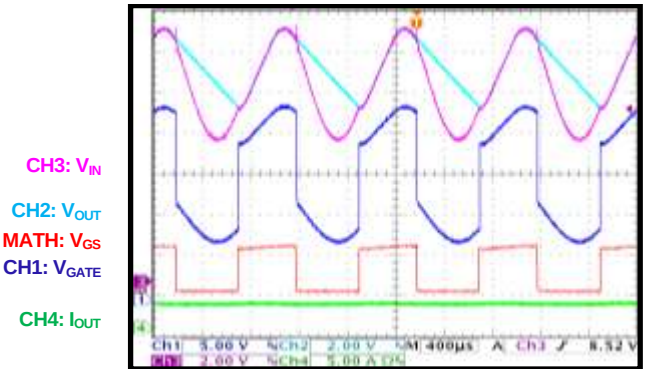
Simultaneous Input

V_{PP} = 6V, f = 1kHz, I_{OUT} = 0A



Simultaneous Input

V_{PP} = 6V, f = 1kHz, I_{OUT} = 3A

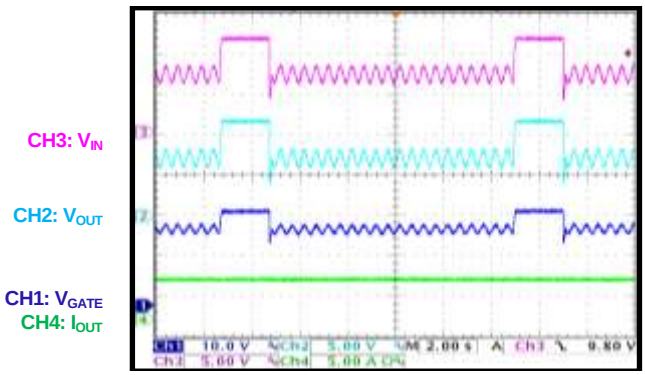


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{OUT} = 5A, L = 68µH, T_A = 25°C, unless otherwise noted.

Start Pulses

I_{OUT} = 5A



FUNCTIONAL BLOCK DIAGRAM

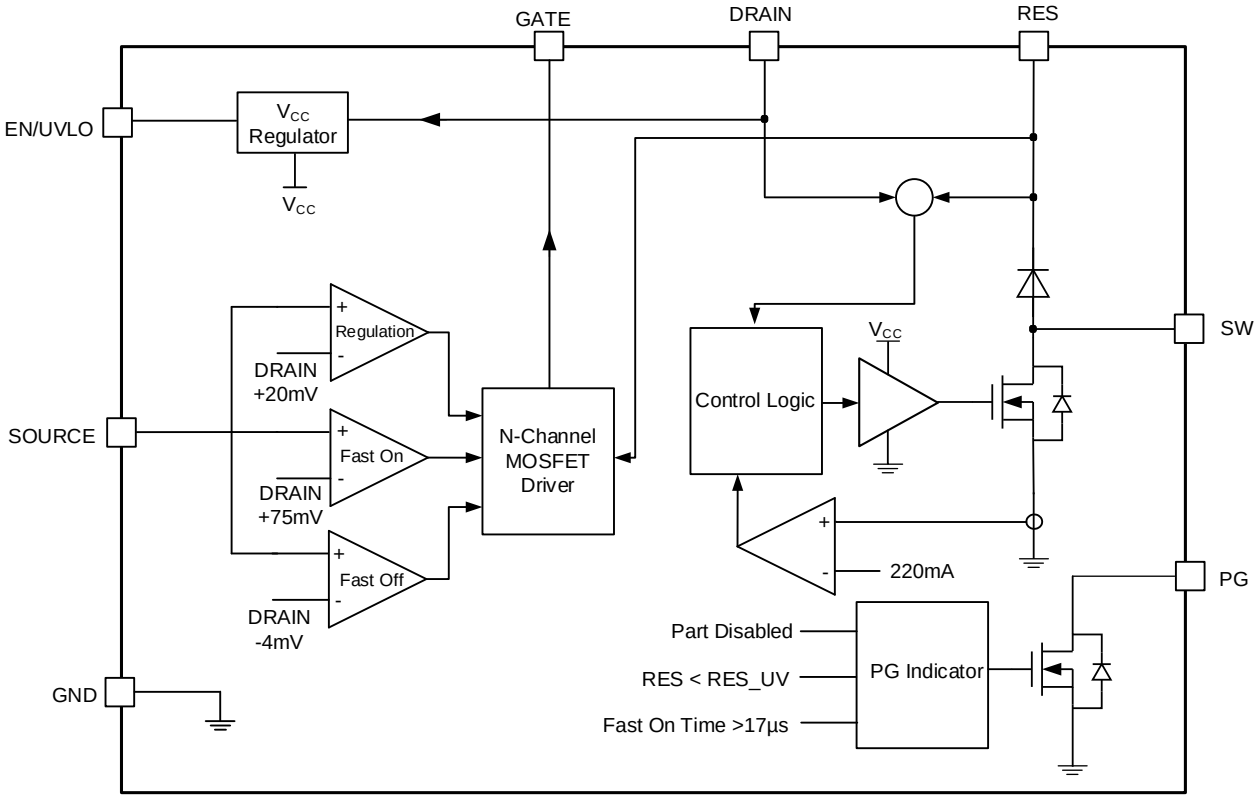


Figure 1: Functional Block Diagram

OPERATION

The MPQ5850 is an 8-pin smart diode controller that drives an external N-channel MOSFET to minimize power loss, including DC forward loss and AC rectification loss.

Smart Diode Operation

During normal operation, when $V_{SOURCE} > V_{DRAIN}$, the MPQ5850 modulates the gate of the external N-channel MOSFET to regulate the source-to-drain voltage to about 20mV. This minimizes power loss and allows small negative currents to be easily detected.

Generally, the source-to-drain voltage is regulated to about 20mV. When the load current rises, the GATE voltage rises until the MOSFET is fully on. If the load current drops, the GATE amplifier drives the MOSFET's gate lower to maintain a 20mV drop.

If the drain-to-source voltage exceeds 20mV, a large current modifies the GATE pin's voltage to regulate the drain-to-source voltage. If a negative current flows through the external N-channel MOSFET, the device detects a source-to-drain negative voltage drop. If the drop exceeds -4mV, the MPQ5850 pulls down the GATE pin to turn off the external N-channel MOSFET quickly. If a forward current flows through the external N-channel MOSFET (either the body or channel), the device detects a source-to-drain forward voltage drop. If the drop exceeds 75mV, the MPQ5850 pulls up the GATE pin to quickly turn on the external N-channel MOSFET. This allows high-frequency AC waveforms (up to 100kHz) to be rectified with minimal system and N-channel MOSFET power loss.

Boost Converter

The integrated boost converter uses fixed peak current mode control. When the reservoir floating supply is below 12V, the boost converter requests another turn-on pulse. This pulse terminates when the inductor current reaches 220mA.

The inductor current should reach 0mA before the next on cycle begins. This sets a maximum frequency (f_{MAX}) depending on V_{DRAIN}. f_{MAX} can be calculated with Equation (1):

$$f_{MAX} = \frac{1}{t_{ON} + t_{OFF}} \quad (1)$$

Where t_{ON} is the on time and t_{OFF} is the off time.

t_{ON} can be estimated with Equation (2):

$$t_{ON} = \frac{I_{PEAK} \times L}{V_{DRAIN} - R_{SW} \times \frac{I_{PEAK}}{2}} \quad (2)$$

t_{OFF} can be calculated with Equation (3):

$$t_{OFF} = \frac{I_{PEAK} \times L}{V_{RES} + V_{DIODE}} \quad (3)$$

Start-Up and Low-Voltage Operation

The MPQ5850 starts in the off state. In this state, the gate is passively pulled to SOURCE, and the boost converter is disabled. Once V_{DRAIN} exceeds the under-voltage lockout (UVLO) threshold, the device enters the disabled state. The device is enabled when it enters a logic high state. In the disabled state, the gate is passively pulled to source, the boost converter is disabled, and the PG pin is pulled low. Once the EN/UVLO pin is pulled high, the device enters the start-up state, which causes the boost converter to turn on. When the reservoir capacitor exceeds the reservoir UVLO threshold, normal operation begins. During normal operation, the gate is actively modulated based on V_{SOURCE} and V_{DRAIN}, and the PG pin is high when the source-to-drain voltage is regulated.

The DRAIN pin is the power supply of the internal circuitry. DRAIN also controls the MOSFET's gate voltage. If V_{DRAIN} exceeds its UVLO threshold, then the MPQ5850 operates normally, even in cold-crank conditions down to 0V. A large electrolytic output capacitor is required under these conditions.

If V_{DRAIN} drops below the UVLO threshold, the device pulls down the GATE pin to SOURCE until the voltage on the reservoir capacitor discharges below V_{RES_UVLO}. This allows the device to minimize forward voltage drops during temporary low voltage transients, such as under cold-crank conditions.

Power Good (PG)

The power good (PG) pin is an open-drain pin designed to indicate the status of the MPQ5850. PG asserts low when the fast pull-up current is active for longer than 17µs, the reservoir capacitor is out of regulation, or the device is disabled. Otherwise, PG de-asserts, and the pin is pulled up to the external source through a pull-up resistor.

APPLICATION INFORMATION

Selecting the Power MOSFET

The power MOSFET must support the maximum steady current during forward operation, and withstand the worst-case battery transients during reverse blocking operation.

The steady state power dissipation is based on the $R_{DS(ON)}$ of the power MOSFET and the load current. If the load is light (I_{LOAD} x $R_{DS(ON)}$ < V_{SD}), the forward drop is regulated to V_{SD} (typically 20mV). The power loss be calculated with Equation (4):

$$P_{CONDUCTION} = V_{SD} \times I_{LOAD} \quad (4)$$

Under heavy loads, the MOSFET is fully enhanced, so power dissipation depends on the $R_{DS(ON)}$ of the MOSFET. The power loss can be estimated with Equation (5):

$$P_{CONDUCTION} = I_{LOAD}^{2} \times R_{DS(ON)} \quad (5)$$

As the high-amplitude ripple on the input is rectified, a MOSFET with the smallest total gate charge (Q_{GTOT}) is required. A MOSFET with smaller Q_{GTOT} not only reduces reverse current during the turn-off delay but it also lowers driver loss.

The operating MOSFET's drain-to-source voltage must be able to support the worst-case conditions, such as when there is a voltage step or the battery voltage goes from a positive to negative voltage. The worst-case condition occurs when V_{IN} is in reverse and V_{OUT} is not discharged to low. V_{DSS} must meet the condition calculated with Equation (6):

$$V_{DSS} \geq V_{OUT} + |V_{IN}| \quad (6)$$

The gate-to-source voltage should be rated to be ±15V or greater.

Selecting the Boost Inductor

The value of the inductor affects the driver's maximum current capability. There is a blanking time in the boost converter, and the inductor current is not detected during the blanking time. The relationship between the blanking time and temperature is shown in Figure 2. To ensure that the inductor current does not exceed 220mA during the blanking time, the inductor value (L) should meet the condition estimated with Equation (7):

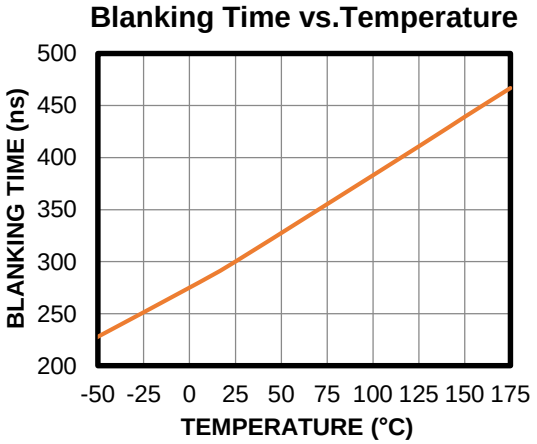


Figure 2: Blanking Time vs. Temperature

$$L > \frac{V_{DRAIN} \times t_{ON\_BLANKING}}{I_{PEAK}} \quad (7)$$

Where V_{DRAIN} is the DRAIN pin's voltage (in V), and I_{PEAK} is the integrated boost converter's current limit (typically 220mA).

Based on the special application to select the required inductor, if V_{DRAIN} is 36V, the inductor should be greater than 49µH in 25ºC temp. Consider the derating of the inductance at different temperatures and currents. It is recommended to select a minimum 68µH inductor with a saturation current exceeding 220mA and a RMS current greater than 80mA. Small-chip inductors (e.g. the LQH2MPZ series from Murata) are recommended. The LQH3NPN series inductors are also suitable.

Selecting the Reservoir Capacitor

Connect a minimum 1µF capacitor, with a minimum 25V rating, from the RES pin to the DRAIN pin. A larger-value capacitor can support the IC if the DRAIN voltage is below its UVLO threshold. Calculate the minimum reservoir capacitance with Equation (8):

$$C_{RES} \geq \frac{I_{GATE} \times (t_S - t_{ON})}{V_{RES\_UVLO\_HYS}} \quad (8)$$

Selecting the Electrolytic Capacitor and Ripple Voltage

During rectification, the electrolytic capacitor (C_{LOAD}) reduces the load's ripple voltage. The load ripple voltage (V_R) is determined by C_{LOAD}, the source ripple frequency, the ripple amplitude, and the load current. The voltage drops with the

frequency. C_{LOAD} can be estimated with Equation (9):

$$C_{LOAD} \geq \frac{4 \times V_{AC} - V_R}{4 \times V_{AC} \times f \times V_R} \times I_{LOAD} \quad (9)$$

Where V_{AC} is the SOURCE voltage ripple amplitude (in V), f is the ripple frequency (in Hz), C_{LOAD} is the capacitance of the electrolytic capacitor (in F), and I_{LOAD} is the load current (in A).

If the ripple voltage (V_R) is below 2V, f is 5kHz, V_{AC} is 3V ($6V_{PP}$), and I_{LOAD} is 5A, then C_{LOAD} is 417µF.

Selecting the TVS Diode

The MPQ5850 can be damaged by the negative pulse on the SOURCE pin, since the voltage of the SOURCE pin is limited to -36V. Connect a TVS diode between SOURCE and GND to protect the part. The SMBJ24CA is recommended, as it can protect the MPQ5850 from negative pulses and over-voltage conditions.

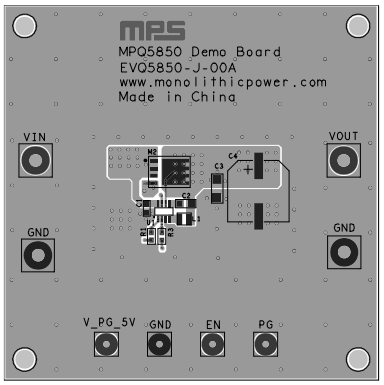
PCB Layout Guidelines [8]

An optimized PCB layout is very important for proper operation. A four-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 3 and follow the guidelines below:

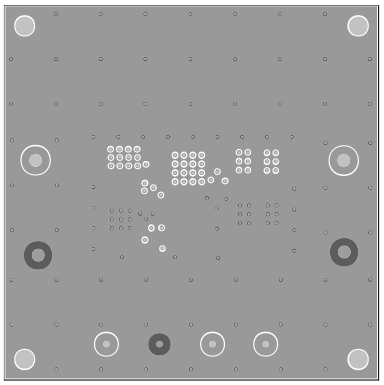
1. Place SW close to the device with short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the IN and GND pins as possible to minimize high-frequency noise.
4. Route SW away from sensitive analog areas.
5. Use multiple vias to connect the power planes to internal layer.

Note:

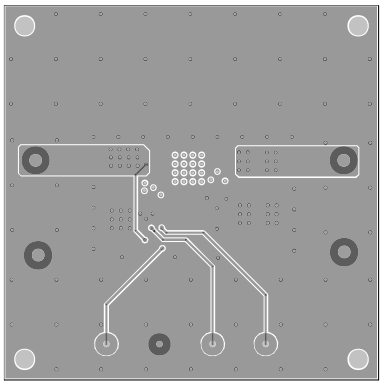
8) The recommended PCB layout is based on the circuit in Figure 4 on page 26.



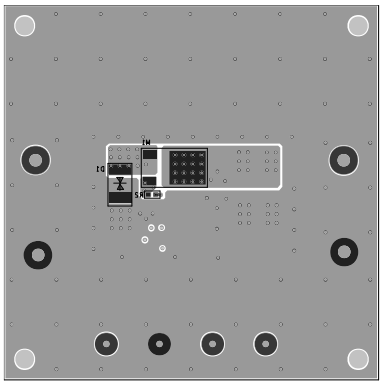
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

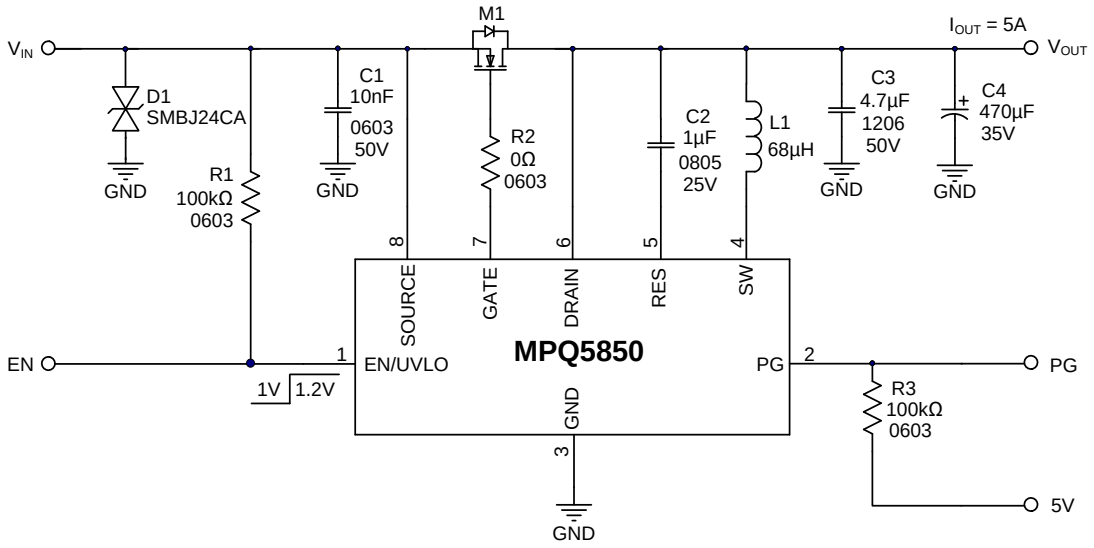
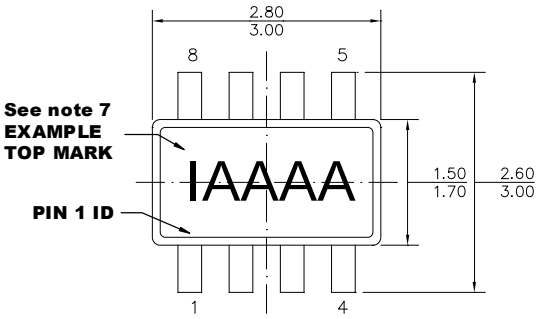


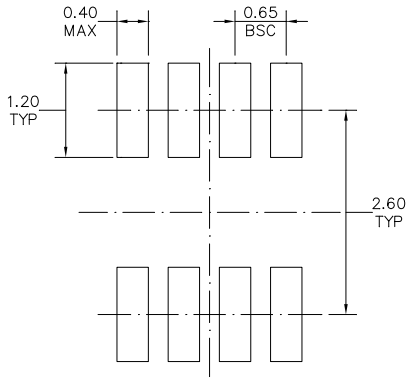
Figure 4: Typical Application Circuit of a 12V Automotive Battery with a 5A Load

PACKAGE INFORMATION

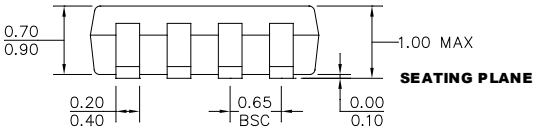
TSOT23-8 (2mmx3mm)



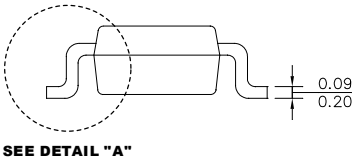
TOP VIEW



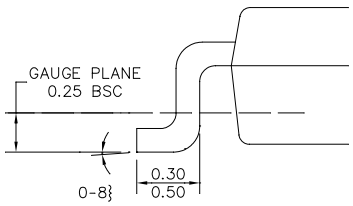
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

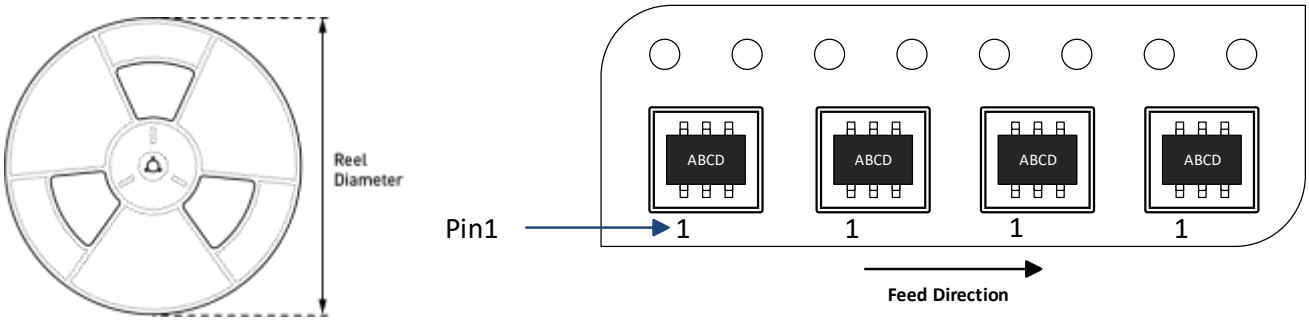


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ5850GJ-Z MPQ5850GJ-AEC1-Z	TSOT23-8	3000	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/27/2021	Initial Release	-
1.1	2/3/2022	Updated the supported cold crank value from “3V” to “0V” in the Features section	1
		Updated the SW pin number to “4” and the RES pin number to “5” in the Pin Functions section	4
		Updated the reservoir UVLO rising min value from “9V” to “8V”	5
		Updated the reservoir regulation UVLO hysteresis conditions from “V_{REG} - V_{RES_UVLO}” to “V_{REG} - V_{RES_UVLO} - $V_{RES\_UVLO\_HYS}$”	6
		Added the Cold Crank waveform where I_{OUT} = 0A to the Typical Performance Characteristics section	18
		Added the updated cold crank description in the Start-Up and Low-Voltage Operation section	22
		Updated the Selecting the Boost Inductor section: added the Blanking Time vs. Temperature curve as Figure 2; added more detailed information; updated the recommended inductor information	24
		Grammar and formatting updates; updated figure numbers	All