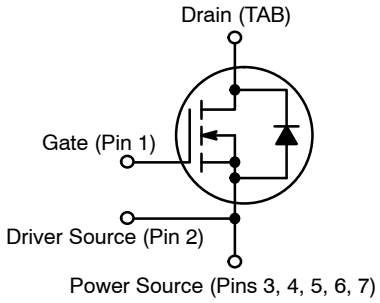
Silicon Carbide (SiC) MOSFET – 22 mohm, 1200 V, M3, D²PAK-7L

NVBG022N120M3S

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
1200 V	30 mΩ @ 18 V	58 A



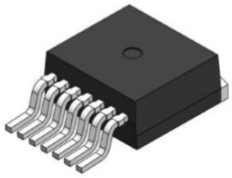
N−CHANNEL MOSFET

Features

- Typ. $R_{DS(on)}$ = 22 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 148 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 148 pF)
- 100% Avalanche Tested
- AEC−Q101 Qualified and PPAP Capable
- These Devices are RoHS Compliant

Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for EV/HEV
- Automotive Traction Inverter



D2PAK−7L
CASE 418BJ

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	1200	V
Gate−to−Source Voltage			V_{GS}	−10/+22	V
Recommended Operation Values of Gate−to−Source Voltage		T_C < 175°C	V_{GSop}	−3/+18	V
Continuous Drain Current (Note 2)	Steady State	T_C = 25°C	I_D	58	A
Power Dissipation (Note 2)	Steady State	T_C = 25°C	P_D	234	W
Continuous Drain Current (Notes 1, 2)	Steady State	T_C = 100°C	I_D	41	A
Power Dissipation (Notes 1, 2)	Steady State	T_C = 100°C	P_D	117	W
Pulsed Drain Current (Note 3)	T_C = 25°C		I_{DM}	159	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode) T_C = 25°C, V_{GS} = −3 V			I_S	53	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 23.1 A, L = 1 mH) (Note 4)			E_{AS}	267	mJ
Maximum Lead Temperature for Soldering (1/8″ from case for 10 seconds)			T_L	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR−4 board using1 in^2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. Peak current might be limited by transconductance
5. E_{AS} of 264 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 23.1 A, V_{DD} = 100 V, V_{GS} = 18 V.

MARKING DIAGRAM

BG022N120M3S = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping
NVBG022N120M3S	D2PAK−7L	800 / Tape & Reel

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THERMAL CHARACTERISTICS

Parameter	Symbol	Typ	Max	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.64	−	°C/W
Junction−to−Ambient − Steady State (Notes 2, 3)	$R_{\theta JA}$	−	40	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF−STATE CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	1200	−	−	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, referenced to 25°C	−	0.3	−	V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	−	−	100	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +22/−10 V, V_{DS} = 0 V	−	−	±1	μA
ON−STATE CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 20 mA	2.04	2.72	4.4	V
Recommended Gate Voltage	V_{GOP}		−3	−	+18	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 18 V, I_D = 40 A, T_J = 25°C	−	22	30	mΩ
		V_{GS} = 18 V, I_D = 40 A, T_J = 175°C	−	47	−	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 40 A	−	34	−	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V	−	3200	−	pF
Output Capacitance	C_{OSS}		−	148	−	
Reverse Transfer Capacitance	C_{RSS}		−	14	−	
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = −3/18 V, V_{DS} = 800 V, I_D = 40 A	−	20	−	nC
Total Gate Charge	$Q_{G(TOT)}$		−	148	−	
Gate−to−Source Charge	Q_{GS}		−	35	−	
Gate−to−Drain Charge	Q_{GD}		−	38	−	
Gate−Resistance	R_G	f = 1 MHz	−	1.5	−	Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, V_{DS} = 800 V, I_D = 40 A, R_G = 4.5 Ω inductive load (Note 6)	−	18	−	ns
Rise Time	t_r		−	24	−	
Turn−Off Delay Time	$t_{d(OFF)}$		−	47	−	
Fall Time	t_f		−	14	−	
Turn−On Switching Loss	E_{ON}		−	485	−	μJ
Turn−Off Switching Loss	E_{OFF}		−	220	−	
Total Switching Loss	E_{tot}		−	705	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Continuous Source−Drain Diode Forward Current	I_{SD}	V_{GS} = −3 V, T_C = 25°C	−	−	53	A
Pulsed Source−Drain Diode Forward Current (Note 2)	I_{SDM}		−	−	159	
Forward Diode Voltage	V_{SD}	V_{GS} = −3 V, I_{SD} = 40 A, T_J = 25°C	−	4.5	−	V

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SOURCE−DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = −3/18 V, I_{SD} = 40 A, dI_S/dt = 1000 A/μs, V_{DS} = 800 V	–	23	–	ns
Reverse Recovery Charge	Q_{RR}		–	146	–	nC
Reverse Recovery Energy	E_{REC}		–	5	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	13	–	A
Charge time	t_A		–	13	–	ns
Discharge time	t_B		–	10	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. E_{ON}/E_{OFF} result is with body diode

TYPICAL CHARACTERISTICS

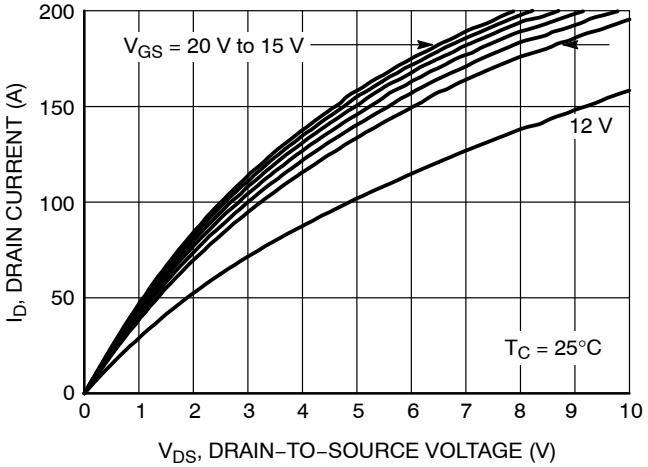


Figure 1. On−Region Characteristics

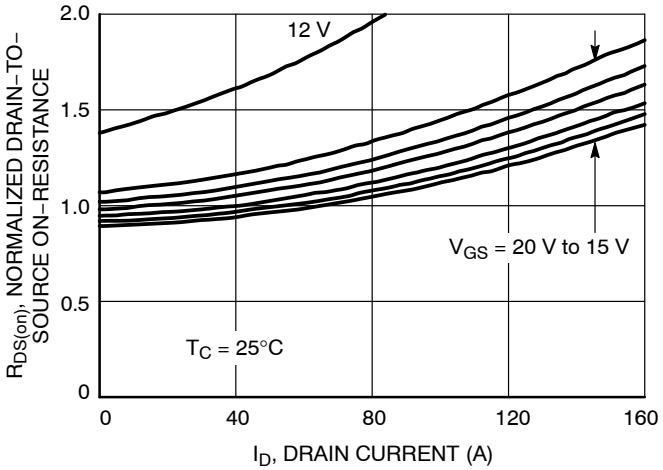


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

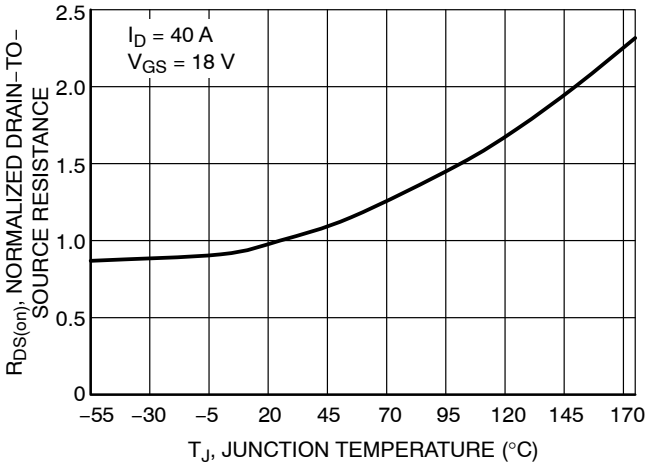


Figure 3. On−Resistance Variation with Temperature

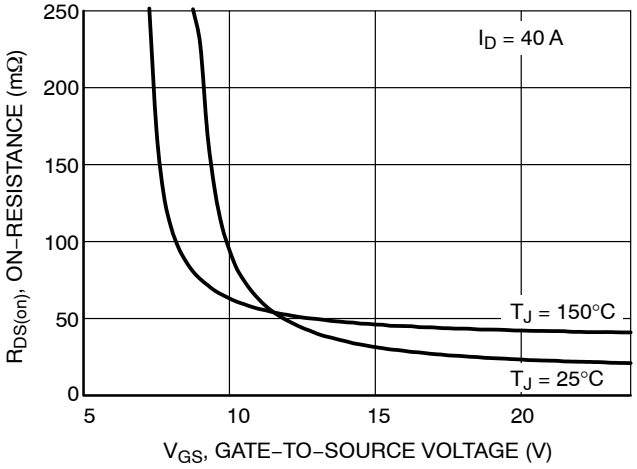


Figure 4. On−Resistance vs. Gate−to−Source Voltage

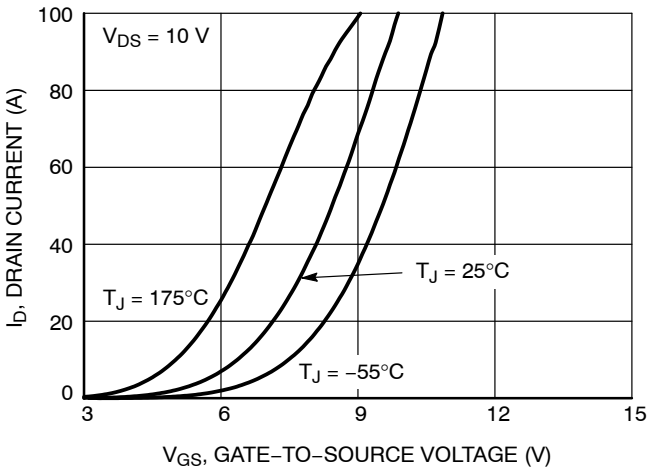


Figure 5. Transfer Characteristics

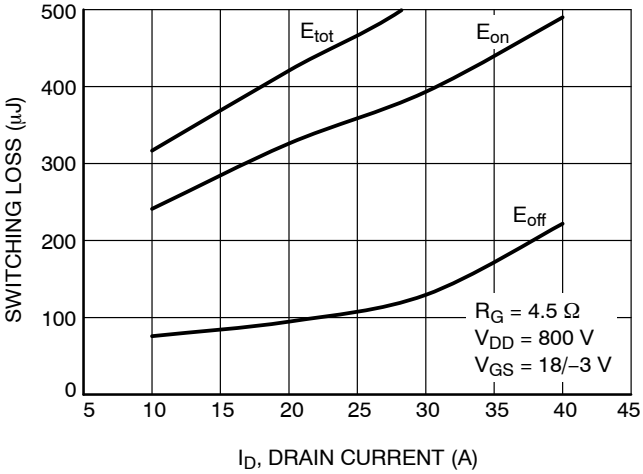


Figure 6. Switching Loss vs. Drain Current

TYPICAL CHARACTERISTICS

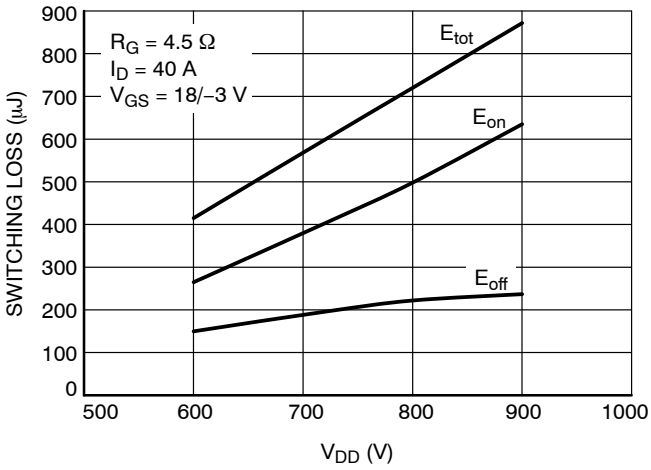


Figure 7. Switching Loss vs. Drain Voltage

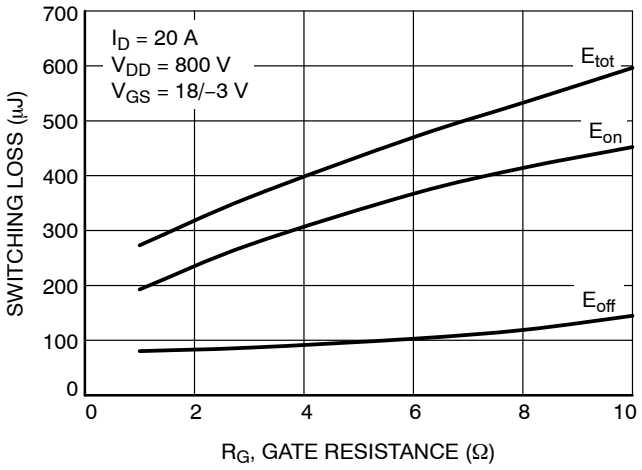


Figure 8. Switching Loss vs. Gate Resistance

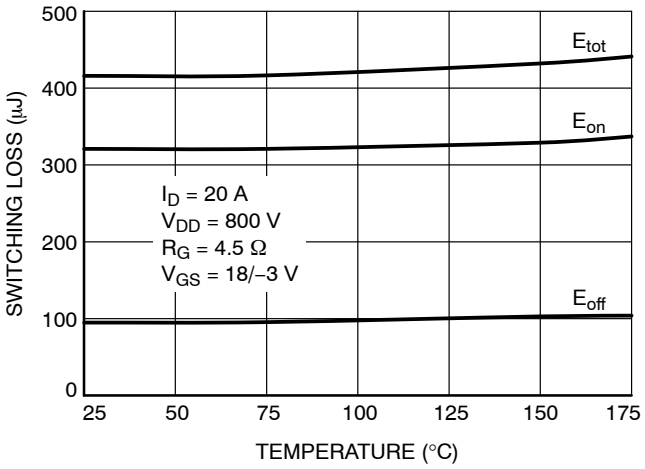


Figure 9. Switching Loss vs. Temperature

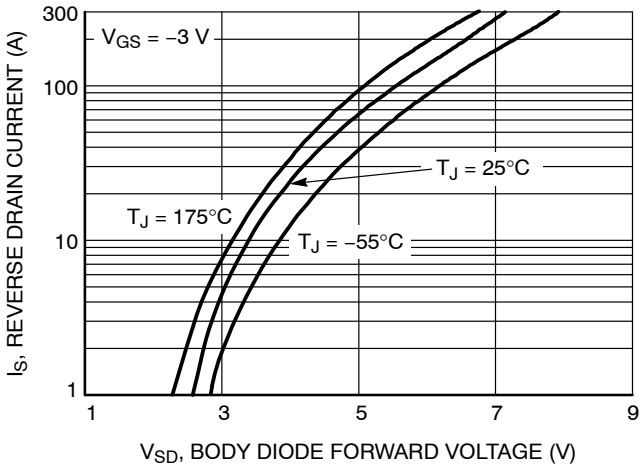


Figure 10. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

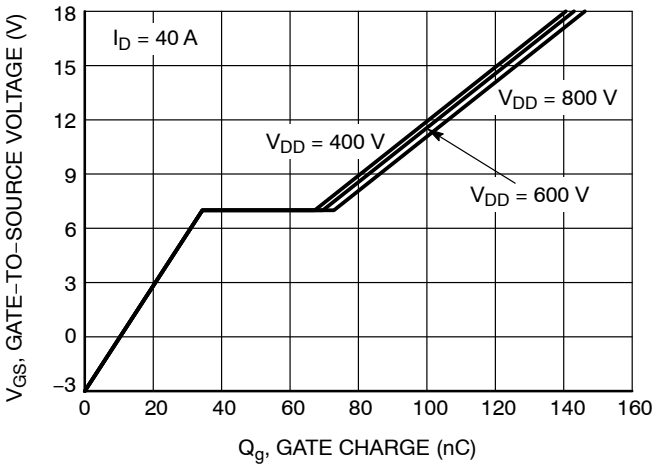


Figure 11. Gate−to−Source Voltage vs. Total Charge

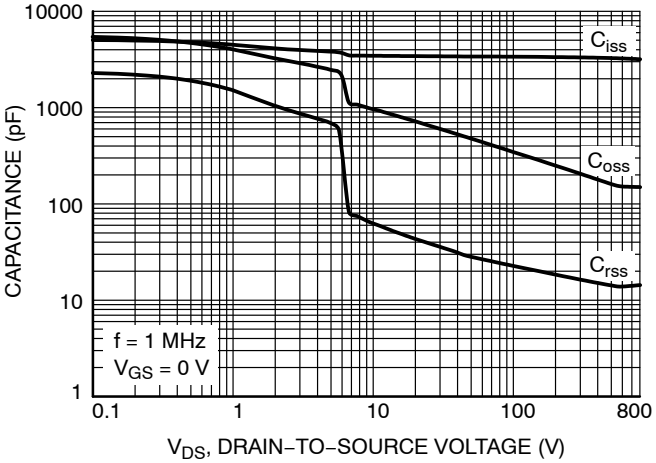


Figure 12. Capacitance vs. Drain−to−Source Voltage

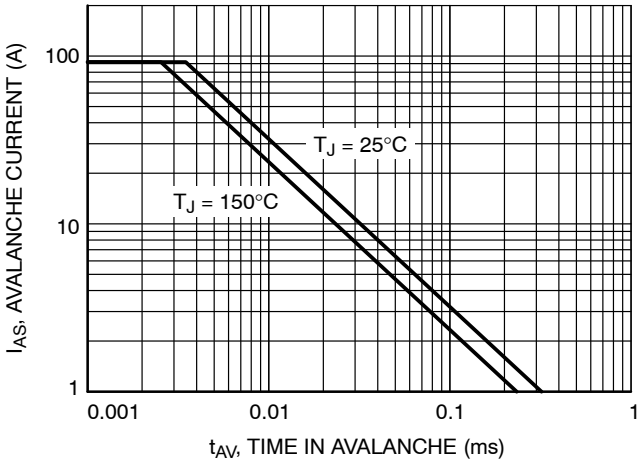


Figure 13. Unclamped Inductive Switching Capability

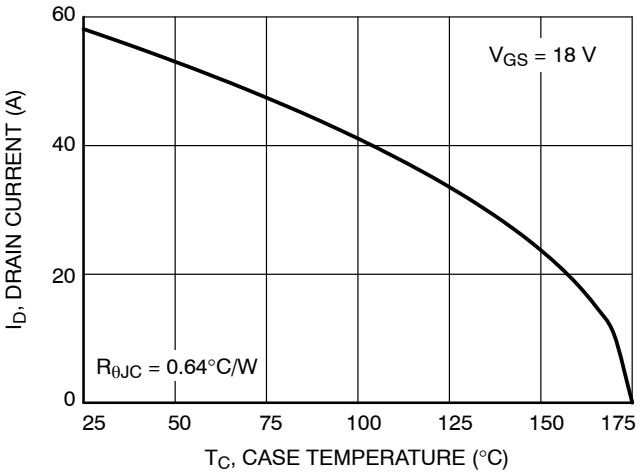


Figure 14. Maximum Continuous Drain Current vs. Case Temperature

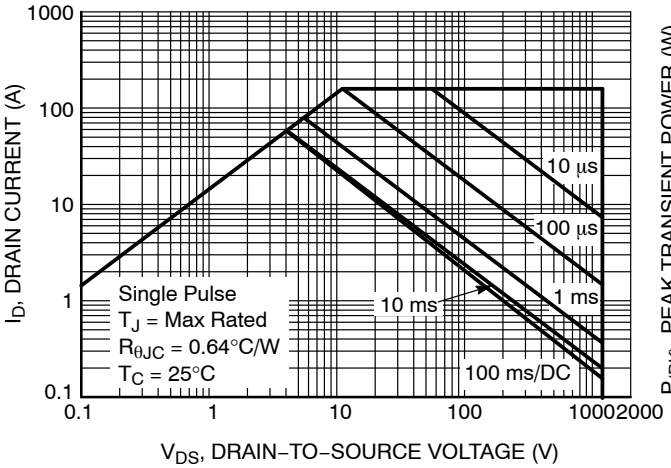


Figure 15. Safe Operating Area

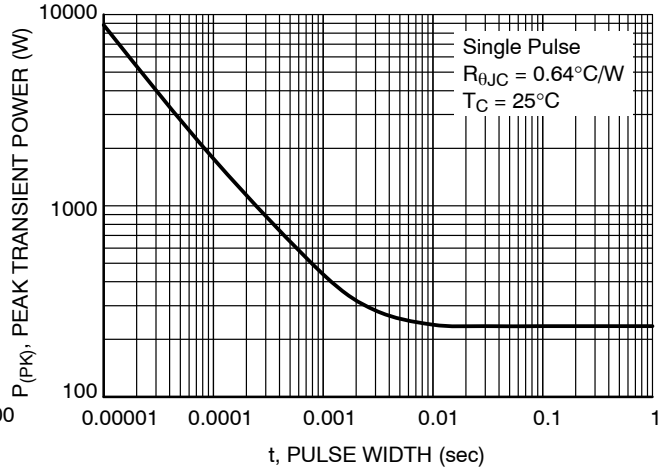


Figure 16. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

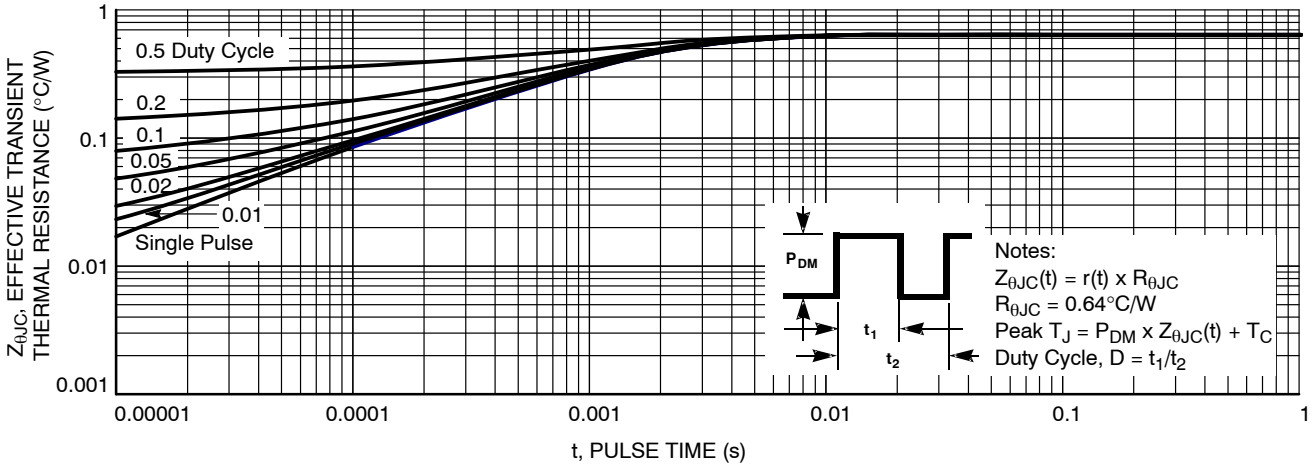


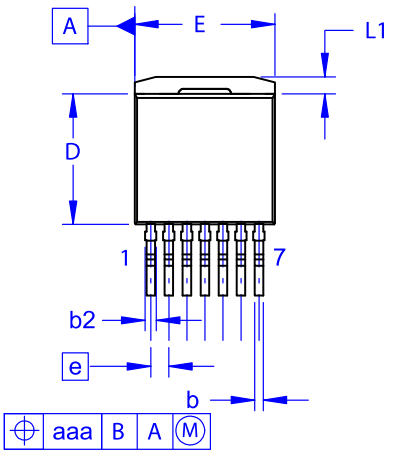
Figure 17. Junction−to−Case Transient Thermal Response

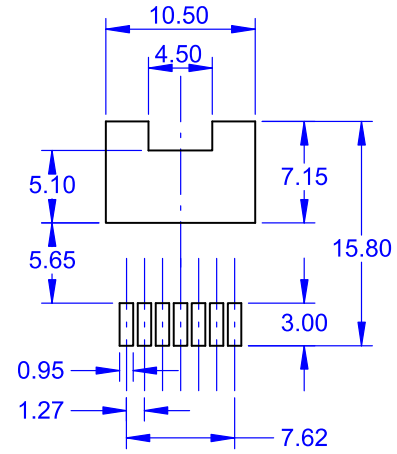
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

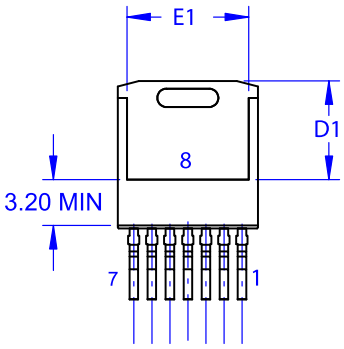
D²PAK7 (TO−263−7L HV)
CASE 418BJ
ISSUE B

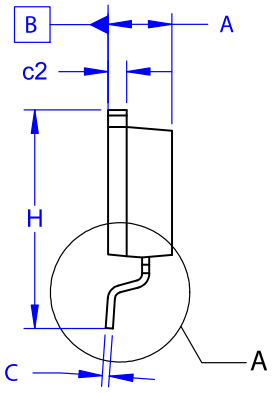
DATE 16 AUG 2019





LAND PATTERN RECOMMENDATION





NOTES:

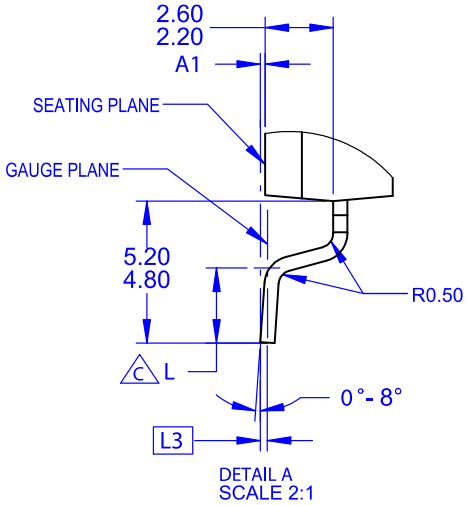
A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**D²PAK7 (TO−263−7L HV)**		**PAGE 1 OF 1**

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