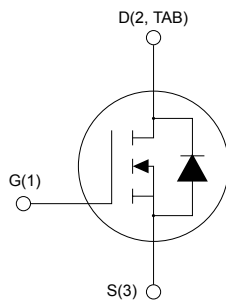
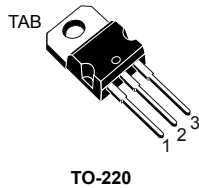


N-channel 600 V, 38 mΩ typ., 56 A MDmesh DM9 Power MOSFET in a TO-220 package



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STP60N043DM9	600 V	43 mΩ	56 A

- Fast-recovery body diode
- Worldwide best R_{DS(on)} per area among silicon-based fast recovery devices
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Power supplies and converters
- LLC resonant converter

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and R_{DS(on)} makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link

[STP60N043DM9](#)

Product summary

Order code	STP60N043DM9
Marking	60N043DM9
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	56	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	35	
$I_{DM}^{(2)}$	Drain current (pulsed)	175	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	245	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1300	A/ μs
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 28\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS} \leq 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.51	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C/W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	775	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 28\text{ A}$		38	43	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	4675	-	pF
C_{oss}	Output capacitance		-	82	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	729	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, open drain	-	0.78	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	78.6	-	nC
Q_{gs}	Gate-source charge		-	29	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	34	-	ns
$t_{r(v)}$	Voltage rise time		-	29	-	ns
$t_{f(i)}$	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 17. Turn-off switching time waveform on inductive load)	-	48	-	ns
$t_{c(off)}$	Crossing time off		-	10	-	ns
$t_{d(v)}$	Current delay time	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	75	-	ns
$t_{r(i)}$	Current rise time		-	3.5	-	ns
$t_{f(v)}$	Voltage fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-on switching time waveform on inductive load)	-	9	-	ns
$t_{c(on)}$	Crossing time on		-	38	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		56	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		175	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 56\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 56\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	170		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.22		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	12		A
t_{rr}	Reverse recovery time	$I_{SD} = 56\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	237		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2.68		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	20.5		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

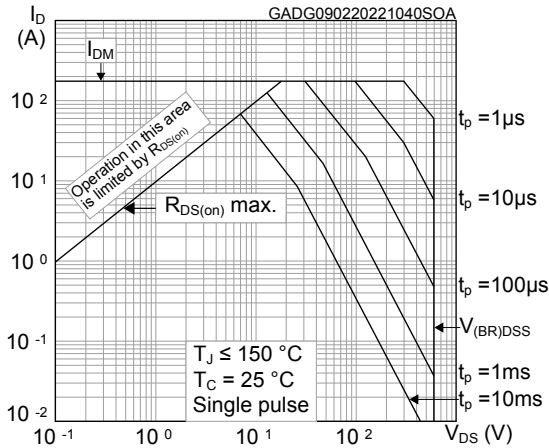


Figure 2. Maximum transient thermal impedance

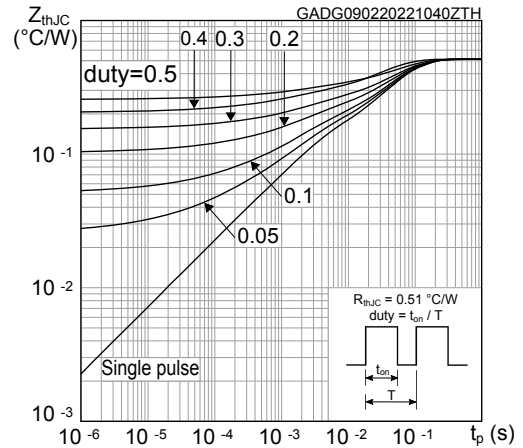


Figure 3. Typical output characteristics

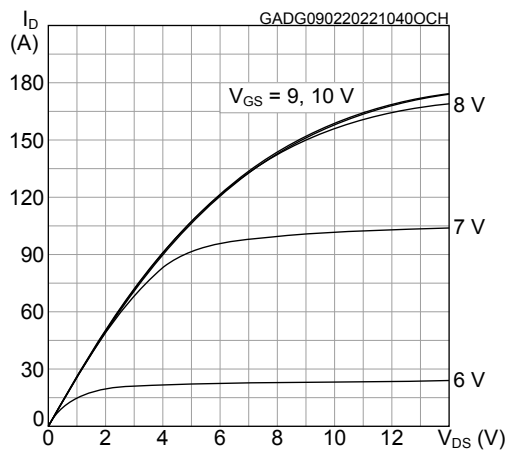


Figure 4. Typical transfer characteristics

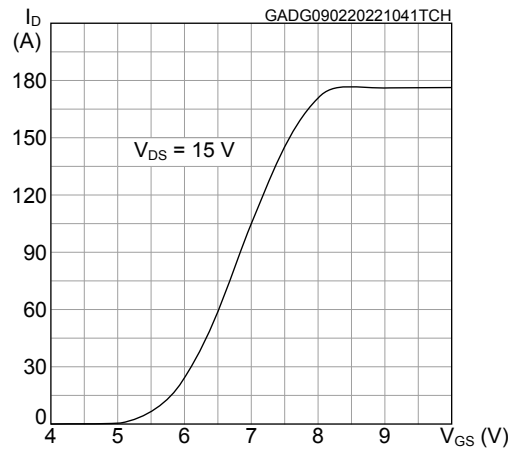


Figure 5. Typical gate charge characteristics

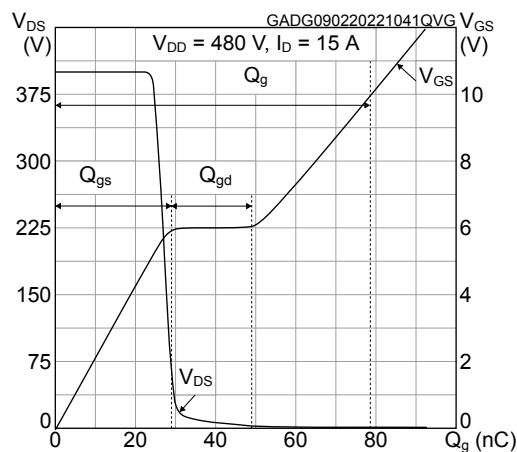


Figure 6. Typical drain-source on-resistance

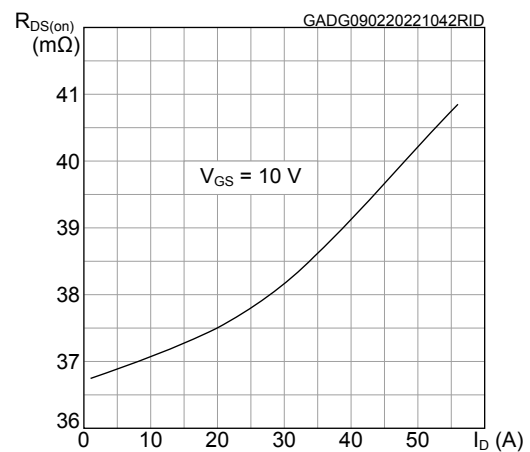


Figure 7. Typical capacitance characteristics

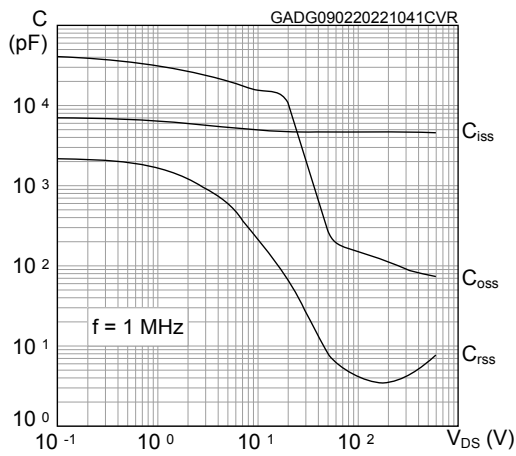


Figure 8. Typical output capacitance stored energy

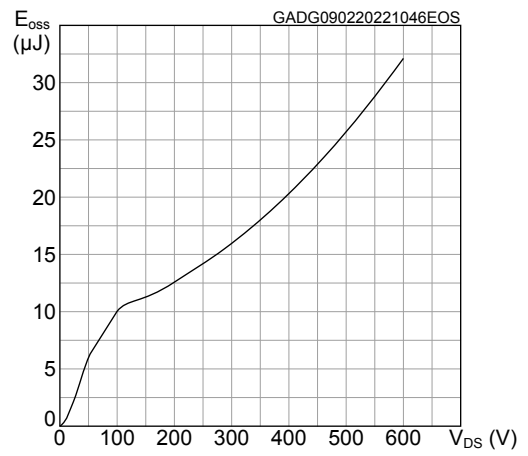


Figure 9. Normalized gate threshold vs temperature

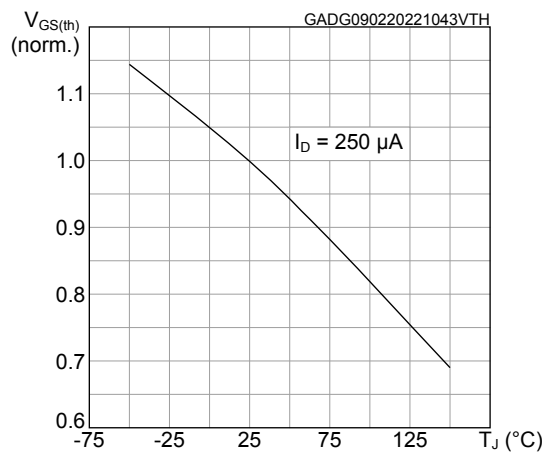


Figure 10. Normalized on-resistance vs temperature

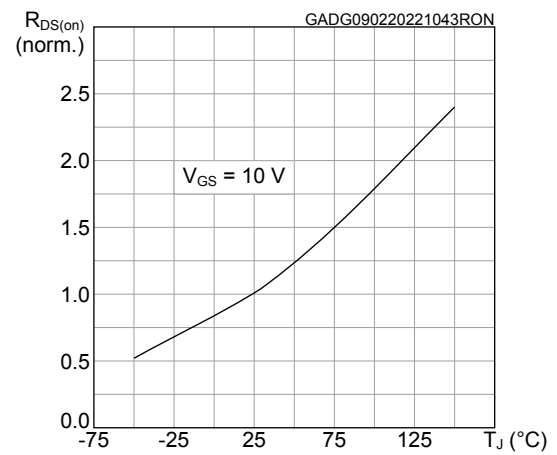


Figure 11. Normalized breakdown voltage vs temperature

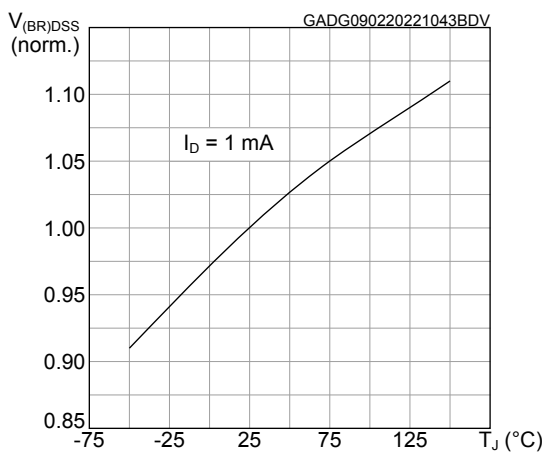
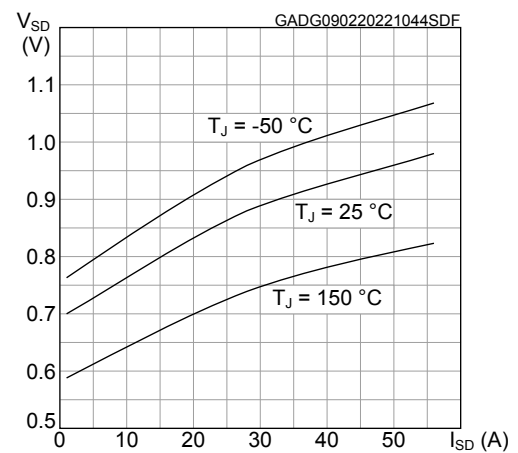
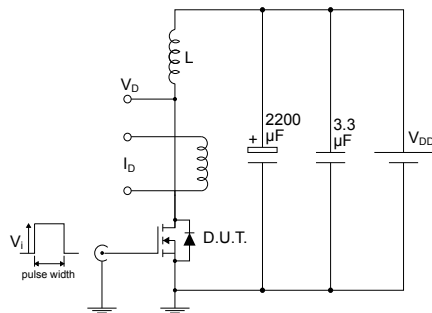


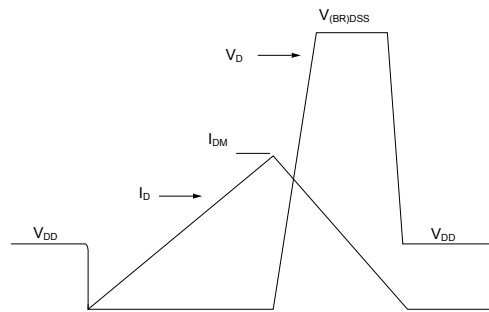
Figure 12. Typical reverse diode forward characteristics



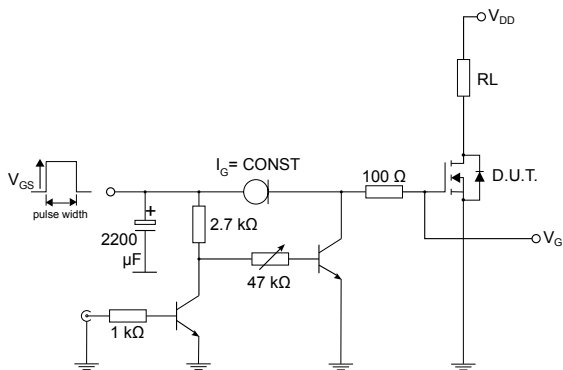
3 Test circuits

Figure 13. Unclamped inductive load test circuit


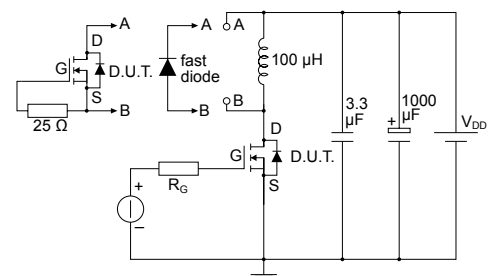
AM01471v1

Figure 14. Unclamped inductive waveform


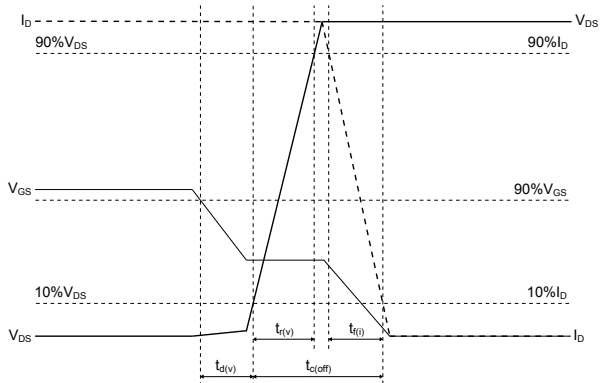
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Figure 15. Test circuit for gate charge behavior


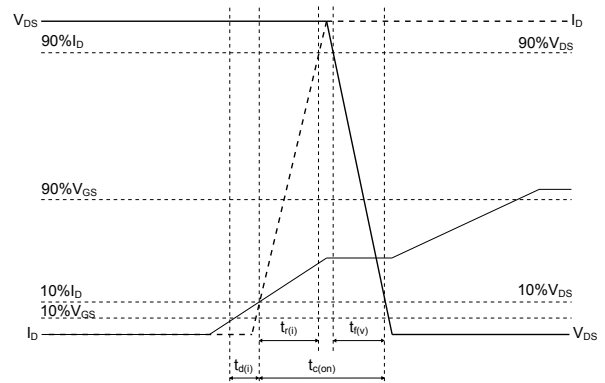
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Figure 16. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 17. Turn-off switching time waveform on inductive load


AM05540v3

Figure 18. Turn-on switching time waveform on inductive load


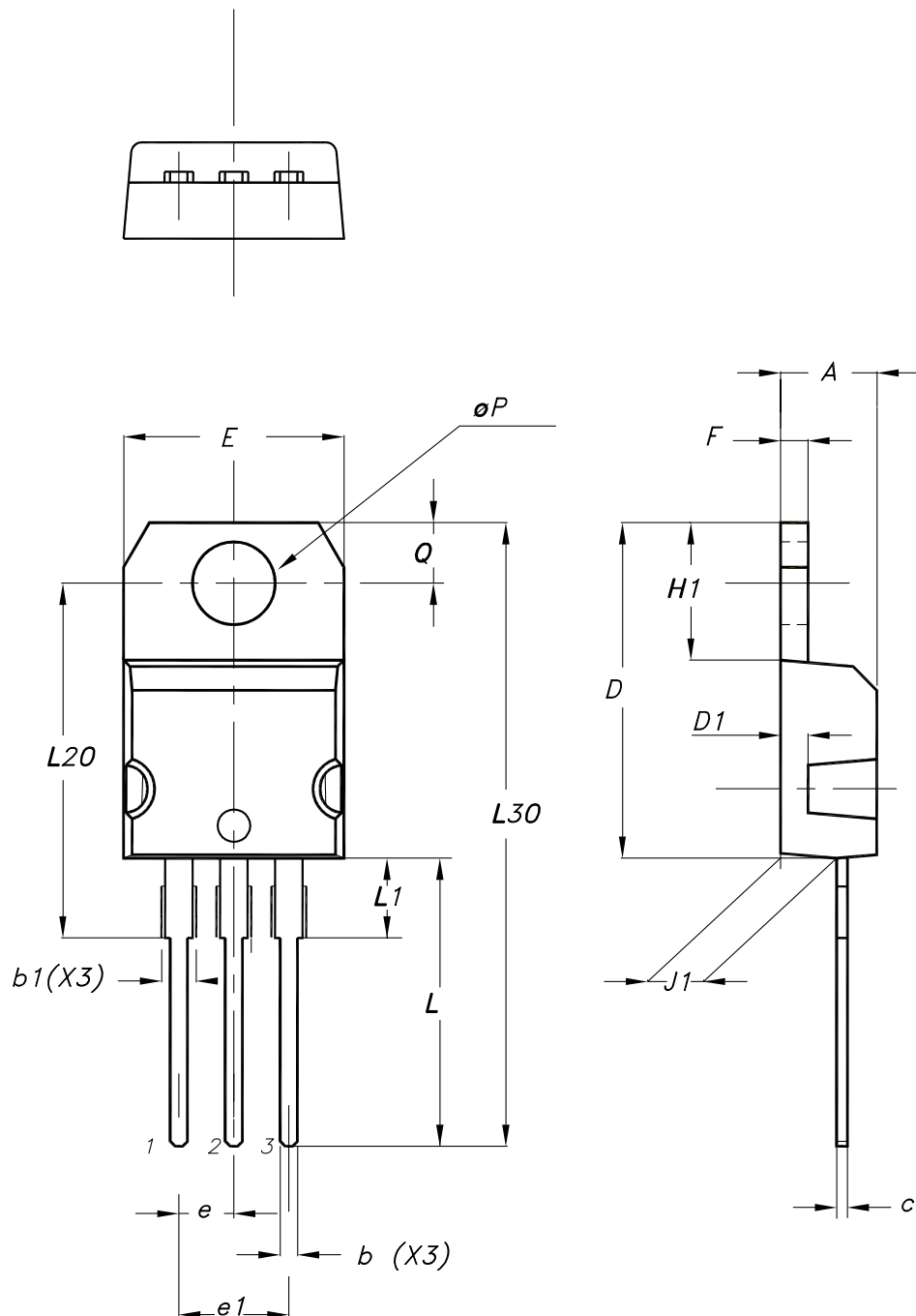
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Feb-2022	1	First release.
06-Sep-2022	2	Updated Features on cover page.

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