Document Number: MC33884
Rev. 4.0, 11/2006

Switch Monitor Interface

33884

SWITCH MONITOR INTERFACE

DW SUFFIX
EG (PB-FREE) SUFFIX
98ASB42344B
24-PIN SOICW

The 33884 Switch Monitor Interface is a monolithic silicon integrated circuit (IC) to perform switch monitoring functions. The device provides efficient interface between electrical switches and low voltage microprocessors. The 33884 supplies switch contact pull-up and pull down current while monitoring the input voltage level. All inputs are protected for transients when implemented with an appropriate static discharge capacitor used on the inputs.

There are four modes of operation: Sleep, Normal, Polling, and Polling + INT Timer.

The Polling and Timer modes are similar, except the Timer mode has the addition of an interrupt that is sent to the microprocessor if a switch is sensed *closed,* or upon the internal interrupt timer *times out*. An interrupt is ultimately sent to the microprocessor. All modes of operation are easily programmed via the Serial Peripheral Interface (SPI) control.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33884DW/R2	-40°C to 105°C	24 SOICW
MCZ33884EG/R2		

Features

- Full Operation with 7.0 V ≤ V_{PWR} ≤ 26 V, Limited Operation with 5.5 V ≤ V_{PWR} ≤ 7.0 V
- Input Voltage Range: -14 V to 40 V
- Interface Directly to Microprocessors Using SPI Protocol
- Wake Up on Change of Monitored Switch Status
- Programmable Wetting Current
- Four Switch-to-Ground Switches
- Six (Fixed Function) Inputs Monitoring Six Switch-to-Ground Switches
- Two (Fixed Function) Inputs Monitoring Two Switch-to-Battery Switches
- Quiescent Current in Sleep Mode ≤ 10 µA
- Reset Input Defaults the Device to Sleep Mode
- Pb-Free Packaging Designated by Suffix Code EG

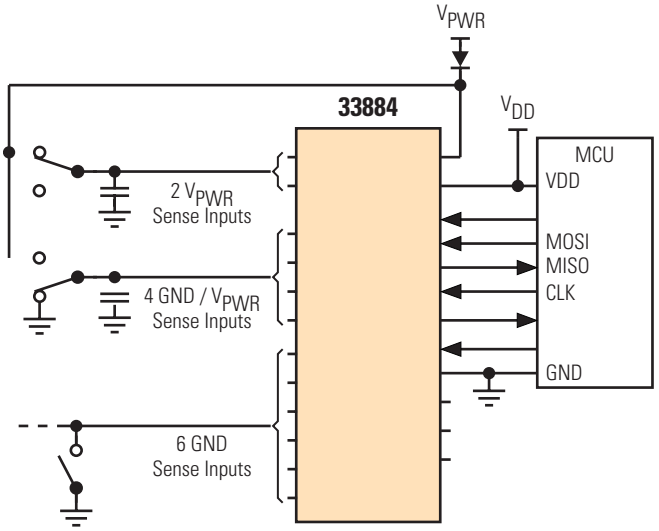


Figure 1. 33884 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

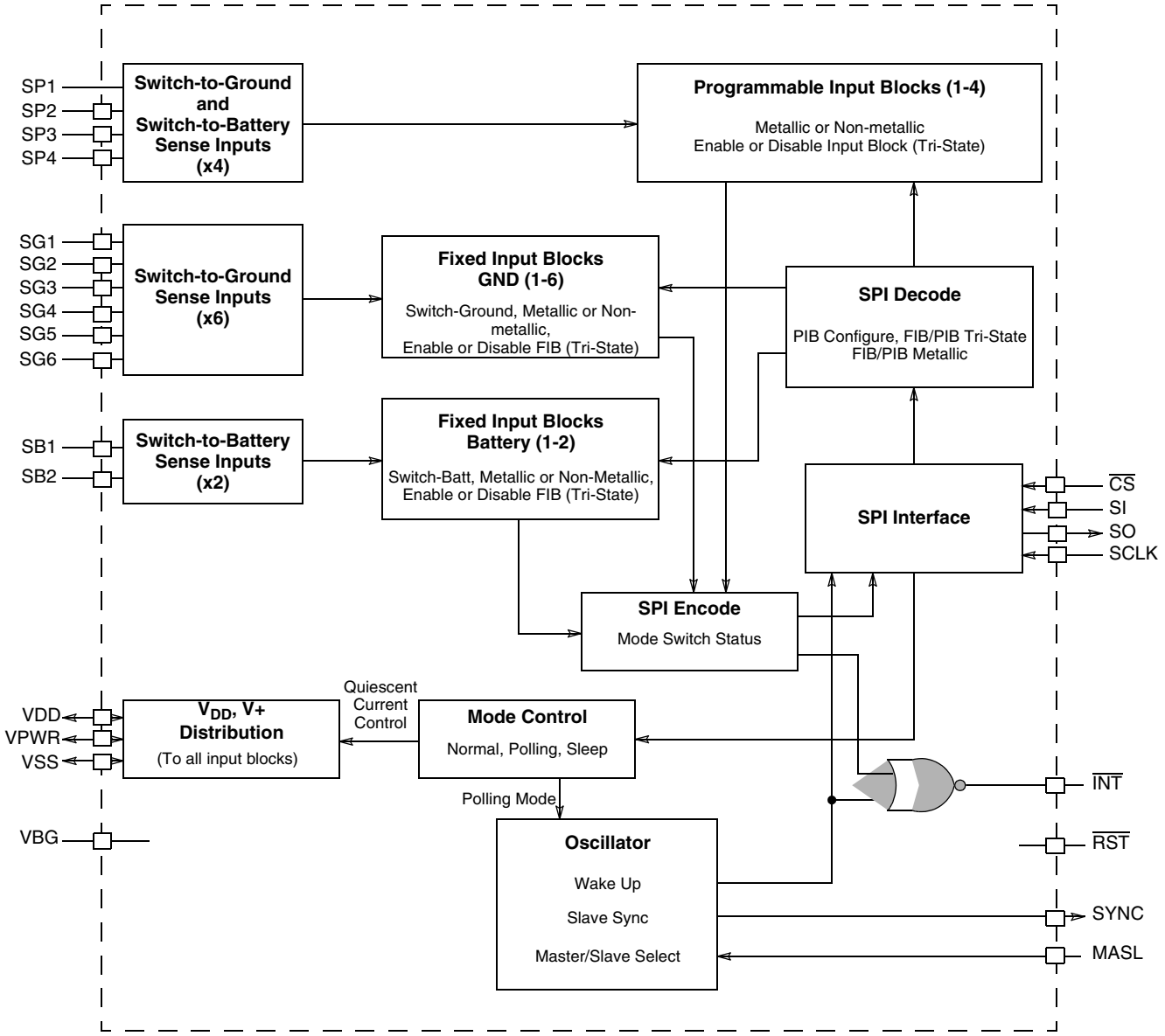


Figure 2. 33884 Simplified Block Diagram

PIN CONNECTIONS

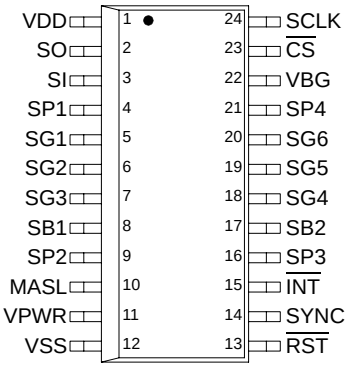


Figure 3. 33884 Pin Connections

Table 1. 33884 Pin Definitions

Pin Number	Pin Name	Formal Name	Definitions
1	VDD	Voltage Power	This pin is 5.0 V logic supply.
2	SO	Serial Output	This pin is the SPI data out.
3	SI	Serial Input	This pin provides data input.
4	SP1	Switch Input One	This pin senses inputs programmed to read switch-to-ground (battery) supply contacts.
5	SG1	Switch-to-Ground Inputs One	This pin is one of six and are switch-to-ground inputs only.
6	SG2	Switch-to-Ground Inputs Two	This pin is one of six and are switch-to-ground inputs only.
7	SG3	Switch-to-Ground Inputs Three	This pin is one of six and are switch-to-ground inputs only.
8	SB1	Switch-to Battery One	This pin is one of two, and senses inputs only.
9	SP2	Switch Input Two	This pin senses inputs programmed to read switch-to-ground (battery) supply contacts.
10	MASL	Master/Slave	This pin identifies which device will be master and which will be slave.
11	VPWR	Voltage Power	This pin is the power source.
12	VSS	Voltage SS	This pin is a ground.
13	$\overline{\text{RST}}$	Reset	This pin is active low reset input to the device.
14	SYNC	Synchronization	This pin is used by the slave IC during the Polling mode.
15	$\overline{\text{INT}}$	Interrupt	This pin is an interrupt output from the device.
16	SP3	Switch Input Three	This pin senses inputs programmed to read switch-to-ground (battery) supply contacts.
17	SB2	Switch-to-Battery Two	This pin is one of two, and senses inputs only.
18	SG4	Switch-to-Ground Inputs Four	This pin is one of six and are switch-to-ground inputs only.
19	SG5	Switch-to-Ground Inputs Five	This pin is one of six and are switch-to-ground inputs only.
20	SG6	Switch-to-Ground Inputs Four	This pin is one of six and are switch-to-ground inputs only.
21	SP4	Switch Input One	This pin senses inputs programmed to read switch-to-ground (battery) supply contacts.
22	VBG	Bandgap Voltage	This pin....

Table 1. 33884 Pin Definitions

Pin Number	Pin Name	Formal Name	Definitions
23	$\overline{CS}$	Chip Select	This pin is transmits communication to the device.
24	SCLK	Serial Clock	This pin clocks the internal 16-bit Shift register of the device.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage $\overline{CS}$, SI, SO, SCLK, $\overline{RST}$, MASL, SYNC, $\overline{INT}$ (1)	V_{DD}	-0.3 to 7.0	V_{DC}
V_{PWR} Supply Voltage (1)	V_{PWR}	-16 to 50	V_{DC}
Switch Input Voltage Range	V_{SI}	-14 to 40	V_{DC}
Recommended Frequency of SPI Operation	f_{SPI}	3.0	MHz
ESD Voltage (2) Human Body Model (3) (4) Machine Model (3) (5)	 V_{ESD1} V_{ESD2}	 4000 200	V
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Case Temperature	T_C	-40 to 105	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (6), (7)	T_{PPRT}	Note 7.	°C
Thermal Resistance (Junction-to-Ambient)	$P\theta_{J-A}$	107	°C/W

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. ESD data available upon request.
3. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω) and ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
4. All pins are tested individually.
5. 1 kV on V_{PWR} and V_{DD} when connected together. See page three.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 105°C, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range Quasi-Functional [8] Fully Operational	 $V_{PWR(QF)}$ $V_{PWR(FO)}$	 5.5 7.0	 —	 7.0 26	V
Supply Current Normal Mode (I_{DD} + I_{PWR}) (All switches open)	$I_{PWR(ON)}$	—	100	300	µA
Supply Current Sleep State ($I_{DD(SS)}$ + $I_{PWR(ON)}$)	$I_{(SS)}$	—	2.0	10	µA
Supply Current Periodic Mode (Polling at 30-50 ms period) (All switches open)		—	26	—	µA
Logic Supply Voltage	V_{DD}	4.75	—	5.25	V
Bandgap Voltage Output Pin (Tested with 130 kΩ ± 0.1% resistor)	V_{BG}	1.18	1.26	1.4	V
Switch Input Pulse Wetting Current Switch to Battery	$I_{W(BAT)}$	7.5	14	25	mA
Switch Input Pulse Wetting Current Switch to Ground	$I_{W(GND)}$	-7.5	-14	-25	mA
Switch Input Sustain Current Switch to Battery	$I_{S(BAT)}$	0.4	0.75	1.25	mA
Switch Input Sustain Current Switch to Ground	$I_{S(GND)}$	-0.4	-0.75	-1.25	mA
Switch Input Tri-State Input Current	$I_{T(SWT)}$	-10	—	10	µA
Switch Input Switch Detection Threshold	I_{TH}	3.25	3.75	4.75	V
Switch Input Switch Input Voltage Range	V_{IN}	-14	—	40	V

Notes

8 SPI inputs and outputs are operational. Fault reporting may not be fully operational within this voltage range. See page five.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 105°C, unless otherwise noted. Typical values, where applicable, reflect the approximate parameter mean with V_{PWR} = 13 V, T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT TIMING					
Pulse Wetting Current Duration	t_{PULSE}	3.0	34	43	ms
Interrupt Delay Time	$t_{INT(DELAY)}$	2.5	—	13	ms
SCLK Frequency vs. SO Load Capacitance 200 pF 160 pF 120 pF	f_{SCLK}	 3.2 3.5 4.0	 — — —	 — — —	MHz
DIGITAL INTERFACE TIMING					
Input Logic Voltage Thresholds (13)	$V_{IN(LOGIC)}$	0.2 x V_{DD}	—	0.7 x V_{DD}	V
SO High State Output Voltage (I_{OH} = 1 mA)	$V_{OH(SO)}$	3.5	—	—	V
SO Low State Output Voltage (I_{OL} = 1 mA)	$V_{OL(SO)}$	—	—	0.4	V
SO Tri-State Leakage Current ($\overline{CS}$ = 0.7 V_{DD}, V_{SO} = 0 to V_{DD})	$I_{T(SO)}$	-40	—	40	µA
SI Pull Down Current (SI = VDD)	I_{SI}	5.0	—	35	µA
SCLK Input Current (0 V = VDD)	I_{SCLK}	-10	—	10	µA
$\overline{CS}$ Pull-Up Current ($\overline{CS}$ = 0 V)	$I_{\overline{CS}}$	-25	—	-5.0	µA
$\overline{RST}$ Pull Down Current ($\overline{RST}$ = 0 V)	$I_{\overline{RST}}$	5.0	—	35	µA
$\overline{INT}$ Low State Output Voltage (I_{OL} = 0.5 mA)	$V_{OL(\overline{INT})}$	—	—	0.4	V
Input Capacitance on SCLK, SI, Tri-State, SO, $\overline{CS}$ (13)	$C_{\overline{IN}}$	—	—	20	pF
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (13) (Required set-up time)	t_{LEAD}	—	100	140	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required set-up time)	t_{LAG}	—	—	50	ns
SI to Rising Edge of SCLK (Required set-up time)	t_{SU2}	—	25	45	ns
Rising Edge of SCLK to SI (Required hold time)	t_{H2}	—	25	45	ns
SO to Rising Edge of SCLK	t_{SU1}	90	125	—	ns
Rising Edge of SCLK to Falling Edge of SO (Hold time)	t_{H1}	90	125	—	ns
SO Rise Time, SO Fall Time (C_L = 200 pF)	$t_{R(SO)}$ $t_{F(SO)}$	—	30	50	ns
SI, $\overline{CS}$, SCLK Incoming Signal Rise Time (13)	$t_{R(SI)}$	—	—	50	ns
SI, $\overline{CS}$, SCLK Incoming Signal Fall Time (13)	$t_{F(SI)}$	—	—	50	ns
Time from Falling Edge of CS to SO Low Impedance (13)	$t_{SO(EN)}$	—	80	110	ns

Notes

9 Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, SCLK, RST, SYNC, MASL. See page five.

10 This parameter is guaranteed by design, however, it has not been production tested.

11 Rise and fall time for incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.

12 Time required for output states data to be available at SO pin.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 105°C, unless otherwise noted. Typical values, where applicable, reflect the approximate parameter mean with V_{PWR} = 13 V, T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Time from Rising Edge of CS to SO High Impedance (13)	$t_{SO(DIS)}$	—	80	110	ns
Time from Falling Edge of SCLK to SO Data Valid (14)	t_{VALID}	—	65	105	ns
Recovery Time for Sequential Transfers	t_{REC}	—	100	120	ns

Notes

13 Time required for output states data to be terminated at SO pin.

14 Time required to obtain valid data out from SO following the falling edge of SCLK.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33884 is a monolithic integrated circuit designed to interface between external electrical system switches and low voltage microprocessors via a Serial Peripheral Interface (SPI). The 33884 monitors the OPEN/CLOSED status of multiple external switches used in a system. The 33884 features four programmable Switch-to-Ground or Battery sense inputs, 6 Switch-to-Ground sense inputs, 2 Switch-to-Battery sense inputs, programmable Wake up Timer, programmable Interrupt Timer, and programmable wetting current settings. All inputs are protected for ESD transients when implemented with the appropriate ESD capacitor.

There are numerous applications for this device in aircraft, aerospace, robotic, process & control, automotive, and security systems. Potential applications exist where switch status verification for safety, fault tolerant operation, or process control function purposes are critical.

The 33884 has four modes of operation: Sleep, Normal, Polling, and Polling + INT Timer.

The 33884 is designed to provide a robust interface between system switch contacts and a microprocessor. Each 33884 input provides the switch contact with high levels of wetting current during switch closure. After the input switch has been closed for 20 ms, the wetting current is reduced, hence reducing power dissipation in the IC. The response to a SPI command will always return Switch Status, Master/ Slave, INT Flag, and Mode settings. The following section describes the programming modes and features of the 33884.

MICROPROCESSOR INTERFACE

The M33884 directly interfaces to 3.3 or 5.0 V MCU. SPI serial clock frequencies in excess of 5.0 MHz may be used for programming and reading switch input status. Figure 4 shows the configuration between an MCU and one 33884.

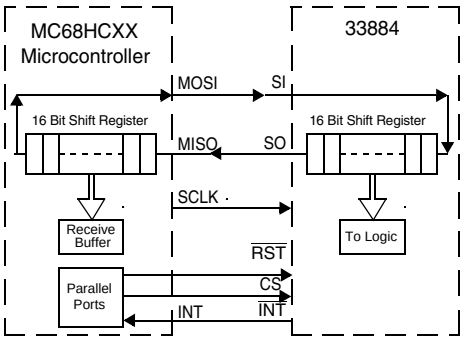


Figure 4. SPI Interface with Microprocessor

The 33884, though originally designed for automotive use, is very useful in a variety of other applications, i.e., computer, telecommunications, and industrial fields. It is parametrically specified over an input battery/supply voltage of 9.0 to 16.0 V but is designed to operate over a considerably wider range of 5.5 to 26.5 V.

Two or more 33884 devices may be used in a module system when implemented in a parallel or serial configuration. Figure 5 and Figure 6 show the parallel and serial configurations respectively. When using the Serial configuration, 32 clock cycles are required for a complete transfer of data to the 33884.

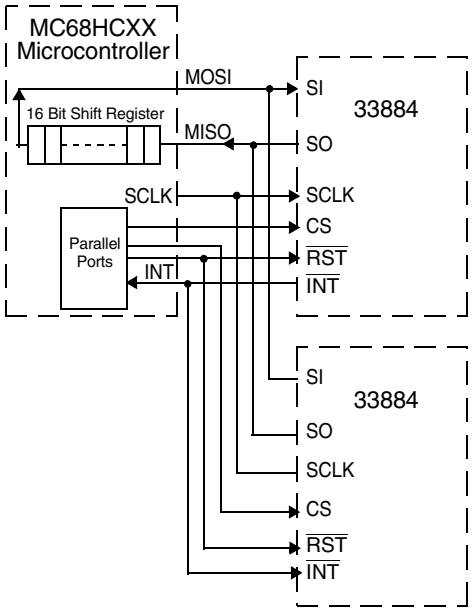


Figure 5. SPI Parallel Interface with Microprocessor

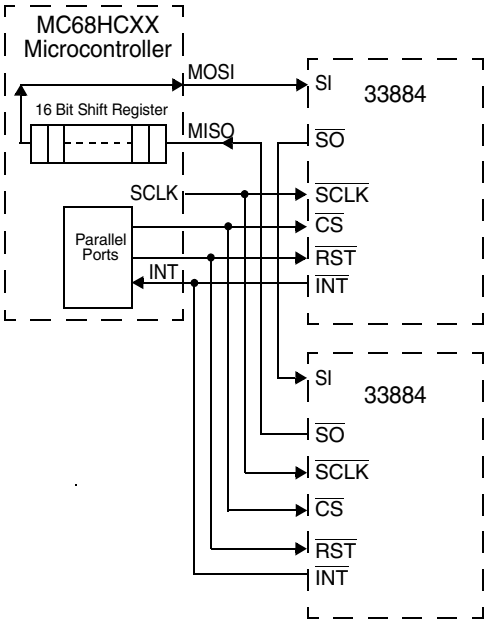


Figure 6. SPI Serial Interface with Microprocessor

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT ($\overline{CS}$)

The MCU system selects the 33884 to receive its communication through the Chip Select ($\overline{CS}$) pin. With the $\overline{CS}$ in a logic low state, command words may be sent to the 33884 via the Serial Input (SI) pin. Switch status is received by the MCU via Serial Output (SO) pin. The falling edge of $\overline{CS}$ enables the SO output, latches the state of the Interrupt ($\overline{INT}$) pin, Operating mode and the state of the external switch inputs. The rising edge of $\overline{CS}$ disables the SO driver, resets the $\overline{INT}$ pin to logic [1], activates the received command word, and allows the 33884 to act upon new data obtained from switch inputs. To avoid any spurious data, it is essential the high-to-low and low-to-high transition of the $\overline{CS}$ signal occur only when System Clock (SCLK) is in a logic low state. Internal to the 33884 is an active pull-up on $\overline{CS}$ pin.

SYSTEM CLOCK (SCLK)

The System Clock (SCLK) pin clocks the internal 16-bit Shift register. The Serial Input (SI) data is latched into the Input Shift register on the rising edge of SCLK signal. The Serial Output (SO) pin shifts the switch status bits out on the falling edge of SCLK. False clocking of the Shift register must be avoided to guarantee validity of data. It is essential the SCLK pin be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason it is recommended, though not necessary, the SCLK pin be commanded to a low logic state as long as the device is not accessed ($\overline{CS}$ in logic high state). When the $\overline{CS}$ is in a logic high state, any signal on the SCLK and SI pin will be ignored and the SO pin is Tri-Stated (high impedance).

SERIAL INPUT (SI)

This Serial Input (SI) pin is used for serial instruction data input. SI information is latched into the Input register on the rising edge of SCLK. A logic high state present at SI when SCLK rises, programs a logic [1] into the command word on rising edge of the $\overline{CS}$ signal. To program a complete word, 16 bits of information must be entered into the 33884. Internal to the IC is an active pull down on the SI pin.

SERIAL OUTPUT (SO)

The Serial Output (SO) pin is the output from the Shift register. The SO pin remains Tri-Stated until the $\overline{CS}$ pin transitions to a logic low state. All *open switches* are reported as logic [0], all *closed switches* are reported as logic [1]. The negative transition of $\overline{CS}$ will make status bit 15 available on SO. Each successive negative clock makes the next status bit available. The SI/SO shifting of the data follows a first-in-first-out protocol with both input and output words transferring the most significant bit (MSB) first.

MASTER/SLAVE (MASL)

The Master/Slave (MASL) pin is required when multiple 33884 devices are used in one module. The MASL identifies which device will be the master or slave. MASL identification is used during the Polling mode. In the Polling mode, the master device has it's internal oscillator running while the Slave device oscillator is shutdown. While polling, the master device wakes the slave via the Synchronization (SYNC) pin. This feature provides minimal quiescent from the voltage power (VPWR) and voltage digital drain (VDD) pins.

SYNCHRONIZATION (SYNC)

The Synchronization (SYNC) input is used by the slave IC during the Polling mode. The SYNC allows multiple 33884 ICs to poll the multiple inputs concurrently. The master controls the polling period. The slave is allowed to shut down it's oscillator, thereby conserving current. When the slave receives the SYNC signal from the master, the slave starts the internal oscillator and reads the switch inputs.

INTERRUPT ($\overline{\text{INT}}$)

The Interrupt ($\overline{\text{INT}}$) pin is an interrupt output from the 33884. The $\overline{\text{INT}}$ pin is an open drain output with an internal pull-up. In the Normal mode, a switch state change triggers the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin and $\overline{\text{INT}}$ bit (flag) are latched on the falling edge of $\overline{\text{CS}}$. This procedure determines the interrupt origin. The flag $\overline{\text{INT}}$ bit in the SPI word is the inverse of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin is cleared on the rising edge of $\overline{\text{CS}}$. The $\overline{\text{INT}}$ pin is active only during the ON time (when sink and source currents are active) in the Polling mode.

RESET ($\overline{\text{RST}}$)

The Reset ($\overline{\text{RST}}$) pin is active low reset input to the 33884. When asserted, the 33884 will reset all internal registers, timers, and enters a Sleep mode (with all switch inputs in a Tri-State condition). Only an MCU SPI command word will wake the 33884 from a Sleep state. The $\overline{\text{RST}}$ pin may be controlled directly from a general purpose input/output (GPIO) pin or from a system/MCU reset.

BANDGAP VOLTAGE (VBG)

The Bandgap Voltage (VBG) pin requires a 130 kΩ to ground for standard wetting and sustain currents. The device is tested with a 0.1 percent value, but a standard 1.0 percent could be used to function properly.

VOLTAGE POWER (VPWR)

The Voltage Power (VPWR) pin is battery/supply source pin for the 33884. The VPWR pin requires external reverse battery/supply and transient protection. Maximum input voltage on VPWR is 40 V. All wetting currents and sustain currents are derived from VPWR.

SWITCH PINS (SP1 : SP4)

The 33884 has four programmable switch sense inputs (SP1- P4) to read switch-to-ground or switch-to-battery/ supply contacts. Transient battery/supply voltages greater than 40 V must be clamped by an external device. Surface mount 0805 MOVs and transient voltage suppressors (TVS) are available in SOT-23 packages. The sensed input is compared with an internal 4.0 V reference. When programmed to sense switch-to-battery, *sensed voltages greater than 4.0 V are interpreted as a CLOSED switch, while sensed voltages less than 4.0 V are interpreted as an OPEN switch*. The opposite holds true when inputs are programmed to sense switch-to-ground. Further programming can set the wetting currents or make the inputs Tri-State. Programming methods are provided in the following section.

SWITCH-TO-BATTERY (SB1 AND SB2)

The two Switch-to-Battery (SB) pins sense inputs only. Transient battery/supply voltages greater than 40 V must be clamped by an external device. Surface mount 0805 MOVs and transient voltage suppressors (TVS) are available in SOT-23 packages.

The sensed input is compared with an internal 4.0 V reference. *Voltages greater than 4.0 V are interpreted as a CLOSED switch, while sensed voltages less than 4.0 V are interpreted as an OPEN switch.* Programming can set wetting currents or Tri-State the input. Programming methods are provided in the following section.

SWITCH-TO-GROUND (SG1 : SG6)

The six Switch-to-Ground (SG) pins are inputs only. The input is compared with the internal 4.0 V reference. *Voltages greater than 4.0 volts are interpreted as an OPEN switch. Voltages less than 4.0 V are interpreted as a CLOSED switch*. Programming can set the wetting currents or Tri-State the input. Programming methods are provided in the following section.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

POWER-UP

On initial power-up all 33884 registers are cleared and the device enters the Sleep mode. To exit the Sleep mode, a valid command word is required to be received from the microprocessor.

SLEEP COMMAND

Sleep mode can be entered by a SPI Sleep command or asserting the $\overline{RST}$ pin. In Sleep mode all inputs are Tri–State and all internal active pull up and pull down currents are disabled. Sleep mode reduces the current drain to a quiescent current level of 10 μA and disables the IC. Sleep mode provides lowest quiescent current for the IC. Exit from sleep mode requires a valid SPI RUN, TRI–STATE, or METALLIC command.

RUN COMMAND

The Run command places the IC in one of three operating modes:

1. This is the normal operating mode of the 33884. In Normal mode the status of the input switches are latched on falling edge of $\overline{CS}$ and data is returned to the MCU via SPI. All programmed combinations of source and sink currents, used for sensing purposes, are always active in this mode. While in the Normal mode, an interrupt is generated and sent to the microprocessor whenever an external switch changes its OPEN or CLOSED state. Prior to a switch closing, the 33884 sources 0.75 mA of sustain current. When the voltage at the input crosses the comparator threshold, 14 mA of current is allowed to flow. The 14 mA wetting current shuts off after a 20 ms timer expires.
2. The Polling mode reads a switch status periodically, interrupting the microprocessor only when an external switch is sensed as being CLOSED. When the 33884 senses all external switches to be OPEN, the Polling mode of operation continues. When a switch is sensed CLOSED, an interrupt is sent to the microprocessor, transferring it's operational mode to the Normal mode. The Polling mode provides a reduction in quiescent current by turning OFF all source and sink currents during sensed switch OFF periods. The Polling mode allows reduction of quiescent current by disabling sink

LOGIC COMMANDS AND REGISTERS

PROGRAMMING AND CONFIGURATION DESCRIPTION

SPI Commands from Microcontroller / Command Protocol
(Data into SI)

Table 5. SPI Command Protocol

Command	MSB															LSB
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Sleep (Default)	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
Run	0	0	0	1	MOD2	MOD1	ST3	ST2	ST1	—	WT2	WT1	CP4	CP3	CP2	CP1
Tri-State	0	0	1	1	TG6	TG5	TG4	TG3	TG2	TG1	TP4	TP3	TP2	TP1	TB2	TB1
Metallic	0	1	0	1	MG6	MG5	MG4	MG3	MG2	MG1	MP4	MP3	MP2	MP1	MB2	MB1
IC Test Mode	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Reset Values:																
Run Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U
Tri-State Register	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0
Metallic Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U =Unknown value coming out of Sleep mode. It be must configured with Run and Metallic commands. Note: the remaining combinations of bits [16;13] are *non-functional* (0010. 0100. 0110. 0111).

MOD[2:1] = Operating mode

CP[4:1] = Configure programmable switch

TG[6:1] = Tri-State switch-to-ground

TB[2:1] = Tri-State switch-to-battery

TP[4:1] = Tri-State programmable switch

ST[3:1] = Sample OFF time

WT[3:1] = Wake up time

MG[6:1] = Metallic switch-to-ground

MB[2:1] = Metallic switch-to-battery

MP[4:1] = Metallic programmable switch

SLEEP COMMAND

The Sleep command places the IC in Sleep mode and essentially turns the part OFF. By definition, a hardware reset sends/keeps the IC in Sleep mode. All inputs are Tri-Stated, disabling all input blocks and all internal pull-ups/pull downs. Only a SPI command can take the IC out of Sleep mode. Exiting this mode requires a valid Run, Tri-State, or Metallic command.

Table 6. Sleep Command

Command	MSB															LSB
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Sleep (Default)	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x

RUN COMMAND

The Run command gives access to all operating modes: Normal, Polling, and Polling + INT Timer. It allows selection of t_{WAIT} and t_{WAKE}, and configures the programmable input blocks. Bit 7 is currently unused. Note that the Run register values are unknown after exiting the Sleep mode.

Table 7. Run Command

	MSB															LSB
Command	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Run	0	0	0	1	MOD2	MOD1	ST3	ST2	ST1	—	WT2	WT1	CP4	CP3	CP2	CP1
Reset Values:																
Run Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U = Unknown value coming out of Sleep mode. It must be configured with Run command.

MOD[2:1] OPERATING MODE

In the Run command, the two MOD bits place the device in one of three operating modes: Normal, Polling, and Polling + INT Timer.

Table 8. Bit Definition for Run Command
Command: Run (0001) with bits [12:1]

Mode	MOD2	MOD1	ST[3:1]	WT[2:1]	CP[4:1]
Undefined	0	0	xxx	xx	CP[4:1]
Normal	0	1	xxx	xx	CP[4:1]
Polling	1	0	ST[3:1]	xx	CP[4:1]
Polling + INT Timer	1	1	ST[3:1]	WT[2:1]	CP[4:1]

ST[3:1] – OFF TIME BETWEEN SAMPLES (T_{WAIT})

During both Polling modes (with and without INT Timer wake up, MOD2=[1]), these bits select the interval of time (t_{WAIT}) the Input Blocks are turned OFF; switch transitions are not detected during the OFF interval.

Table 9. Sample OFF Time Prescales

ST[3:1]	Multiplier Selected	OFF Time, t_{WAIT} (ms) [t_{DETECT} (4.8ms typ) x Multiplier]	ON Time (ms)
000	5	15 - 25	5.1 - 6.3
001	9	30 - 55	5.1 - 6.3
010	17	60 - 90	5.1 - 6.3
011	25	100 - 140	5.1 - 6.3
100	33	145 - 185	5.1 - 6.3
101	41	195 - 215	5.1 - 6.3
110	49	220 - 245	5.1 - 6.3
111	57	250 - 320	5.1 - 6.3

WT[2:1] – WAKE UP TIME

These bits allow the device to assert an external interrupt (INT) at the following intervals during Polling mode (MOD2 = MOD1 = 1).

Table 10. Wake Up Delay Prescales

WT[2:1]	Multiplier Selected	Wake Up Interrupt, t_{WAIT} (ms) [t_{DETECT} (2.8ms typ) x Multiplier]
00	512 + 1	2400 - 3200
01	256 + 1	1200 - 1600
10	128 + 1	600 - 750
11	64 + 1	290 - 360

TRI-STATE COMMAND

This command places an external switch into a Tri-State condition, essentially disconnecting the wetting current (if the switch is metallic) and the sustain current. The internal input-threshold comparator is still internally connected to its external pin. This command does not change the mode of operation

CP[4:1] – CONFIGURE PROGRAMMABLE SWITCH

Configure the programmable inputs SP[4:1] to detect either an external switch-to-ground (internal current source) or an external switch-to-battery (internal current sink).

Note: This configuration may be entered in any of the three valid Operating Modes (see MOD[2:1]) within the Run command.

Table 11. Programmable Switch Bit Definition

CPx	External Switch to:
0	Ground
1	Battery

(e.g., a Tri-State command received while in the Polling mode leaves the part in that mode).

Note: The Tri-State register clears all bits to logic [0] (all inputs in Tri-State) in response to a hardware reset; all inputs also remain in Tri-State after existing the Sleep mode.

Table 12. Tri-State Command

	MSB															LSB
Command	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Tri-State	0	0	1	1	TG6	TG5	TG4	TG3	TG2	TG1	TP4	TP3	TP2	TP1	TB2	TB1
Reset Values:																
Run Register	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0

TG[6:1] = Tri-state switch-to-ground

TB[2:1] = Tri-state switch-to-battery

TP[4:1] = Tri-state programmable switch

Table 13. Programmable Switch Bit Definition

TGx, TBx, TPx	Input Configured to:
0	Input Disabled (Default)
1	Input Enabled

METALLIC COMMAND

This command enables the pulsed wetting current for an external metallic switch and disables it for an external non-metallic switch. This command does not change the mode of operation (e.g., a Metallic command received while in Polling mode leaves the part in that mode). Note that the Run register values are unknown after exiting the Sleep mode.

Table 14. Metallic Command

	MSB															LSB
Command	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Metallic	0	1	0	1	MG6	MG5	MG4	MG3	MG2	MG1	MP4	MP3	MP2	MP1	MB2	MB1
Reset Values:																
Run Register	—	—	—	—	U	U	U	U	U	U	U	U	U	U	U	U

U = Unknown value coming out of Sleep mode. It must be configured with Run command.

MG[6:1] = Metallic switch-to-ground

MB[2:1] = Metallic switch-to-battery

MP[4:1] = Metallic programmable switch

Table 15. Metallic Switch Bit Definition

MGx, MBx, MPx	Accept Switch Type:
0	Non-Metallic
1	Metallic (Enable Wetting Current Pulse)

TEST MODE

Bit 16 is reserved for placing the device into a special IC Test mode. It is used to confirm various internal functions.

Table 16. Test Mode

	MSB															LSB
Command	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IC Test Mode	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SPI RESPONSES

Response Protocol (Data out of SO).

Table 17. SPI Responses

	MSB															LSB
Mode	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Reset/Sleep	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Normal	0	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1
Polling	1	0	MASL	x	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1
Polling + INT Timer	1	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG1	SP4	SP3	SP2	SP1	SB2	SB1

SG[6:1] = Switch-to-ground flag

SB[2:1] = Switch-to-battery flag

SP[4:1] = Programmable switch flag

MASL = Master/Slave identification flag

INT = External Interrupt flag

RESET/SLEEP

When the Reset ($\overline{RST}$) input is active (logic [0]), all internal registers are cleared, thereby placing the device in Sleep mode and upon the $\overline{RST}$ input returning to the inactive state (logic [1]) the MC33884 remains in Sleep mode. A SPI command, received from the microprocessor, is necessary to command the device out of Sleep mode.

Table 18. Reset/Sleep

	MSB															LSB
Mode	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Reset/Sleep	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Note: The SPI response given while sending the command to exit Sleep mode should be ignored due to unknown power-up state.

NORMAL AND PERIODIC

Bits [16:15] identify one of the three operating modes: Normal, Polling, and Polling + INT Timer. The remaining bits identify the device as the Master or a Slave, whether the device has an interrupt that has not been cleared, and the state of all the inputs.

Table 19. Normal and Periodic

	MSB															LSB
Mode	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Normal	0	1	MASL	INT	SG6	SG5	SG4	SG3	SG2	SG2	SG1	SP3	SP2	SP1	SB2	SB1
Polling	1	0		x								—		—		
Polling + INT Timer	1	1		INT								—		—		

Note: The SPI response given while sending the command to exit Sleep mode should be ignored due to unknown power-up state.

MASL– MASTER/SLAVE IDENTIFICATION FLAG

This flag is the same as the state of the MASL pin. It provides software identification of the configuration of each IC.

Table 20. MASL Bit Definition

MASL	Device is a:
0	Slave
1	Master

INT – EXTERNAL INTERRUPT FLAG

This flag identifies this particular IC as the initiator of an external interrupt. It is the inverse of $\overline{\text{INT}}$.

Table 21. MASL Bit Definition

MASL	16	15	14	13	Type of Interrupt
Normal	0	1	x	0	Nothing Happened
	—	—	—	1	Switch Interrupt
Polling	1	0	x	x	—
	1	1	x	0	Nothing Happened
Polling + INT Timer	—	—	—	1	Wake up Interrupt

SG[6:1] = Switch-to-ground flag

SB[2:1] = Switch-to-battery flag

SP[4:1] = Programmable switch flag

These twelve flags indicate the state of all switch inputs:

Table 22. Switch State Bit Definition

SGx, SBx, SPx	External Switch is:	Mode	Input States Latched:
0	Open	Normal	At the moment CS transitions to logic 0
1	Closed	Polling	

TRI-STATE

All Tri-State inputs have their wetting and sustain currents disabled. By definition, all disabled inputs return the following value for the switch state whenever SPI data is exchanged:

Table 23. Tri-State Bit Definition

SGx, SBx, SPx	External Switch is:
0	Tri-State

TYPICAL APPLICATIONS

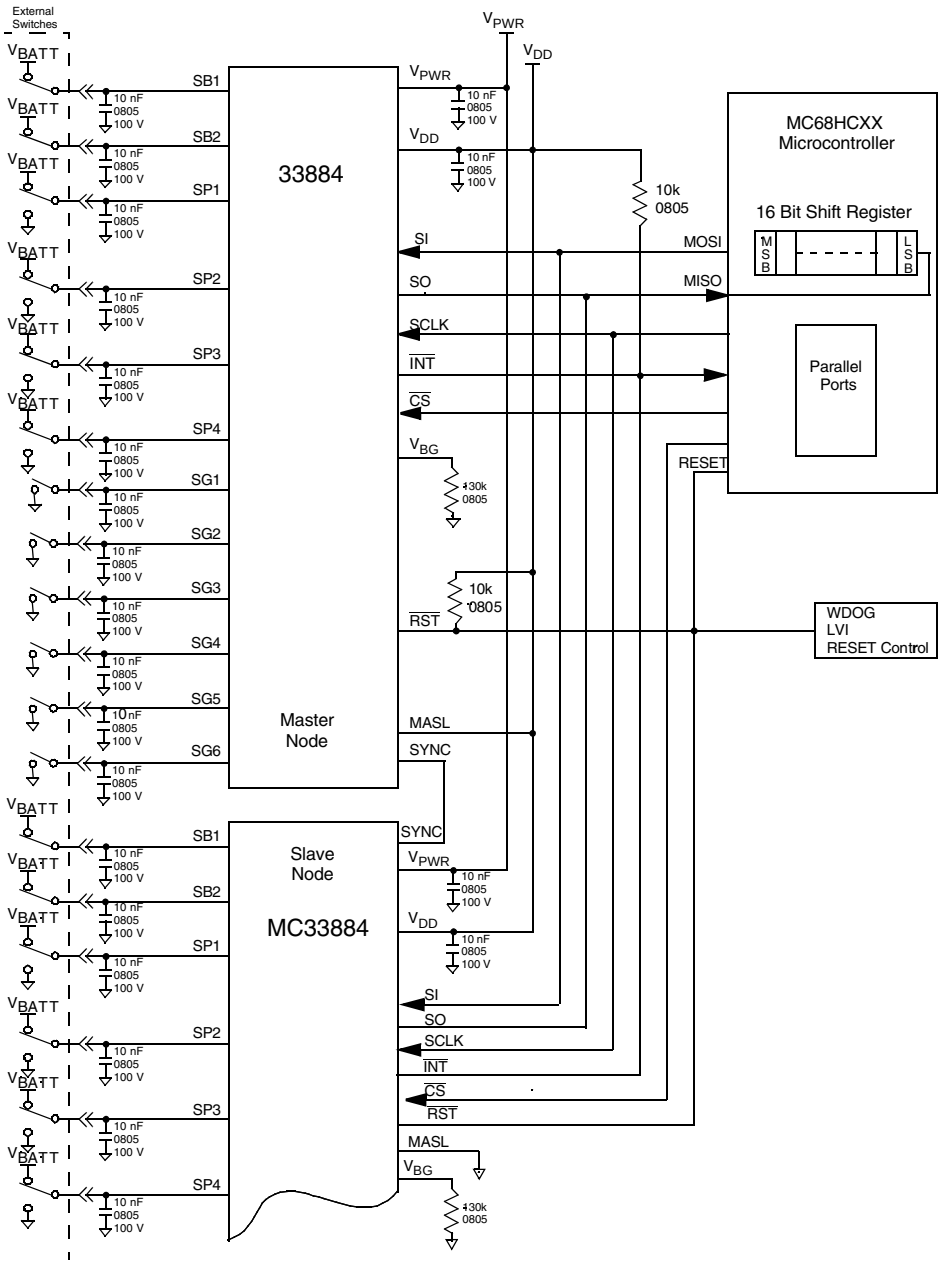
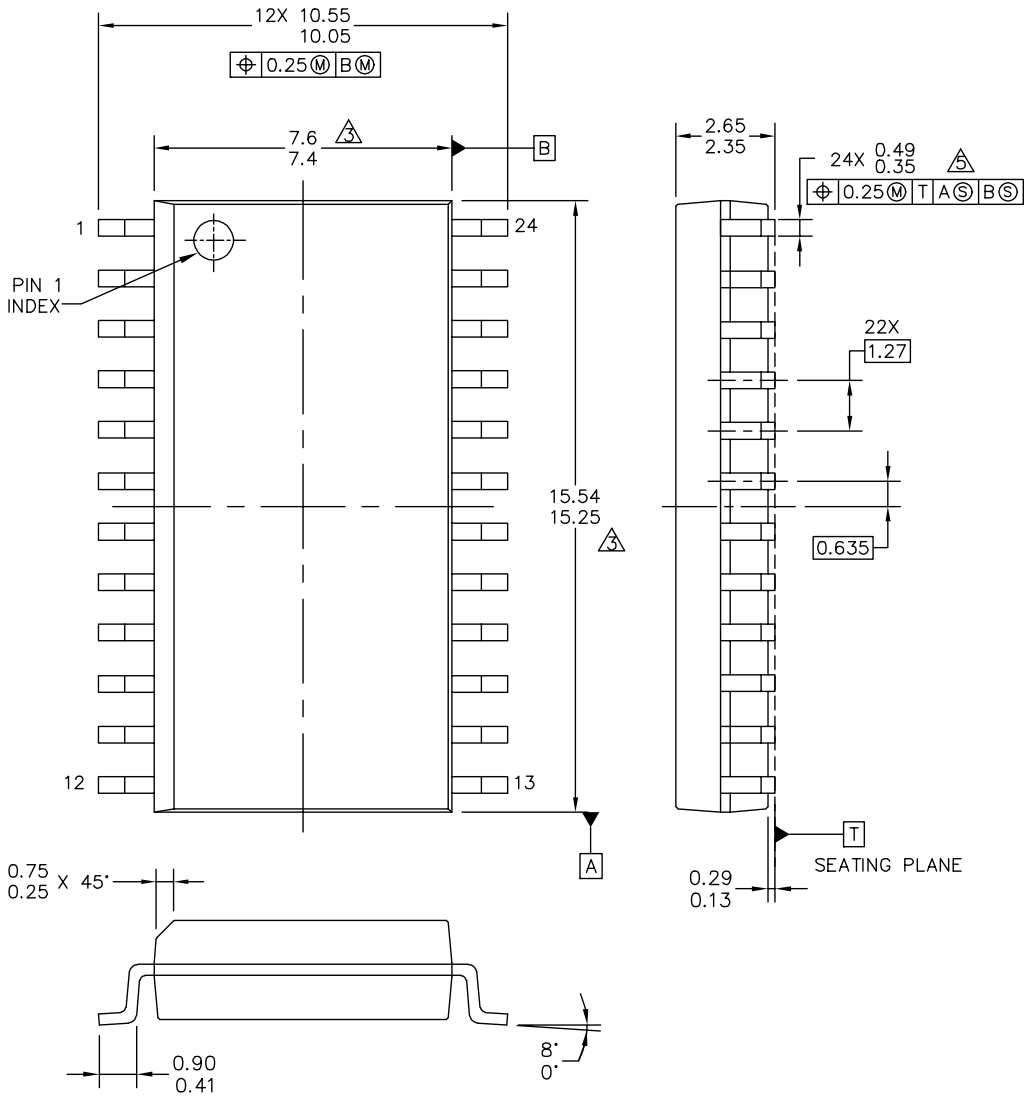


Figure 7. Typical Master/Slave Application

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 24LD SOIC W/B, 1.27 PITCH 7.5 X 15.4 CASE–OUTLINE	DOCUMENT NO: 98ASB42344B	REV: F
	CASE NUMBER: 751E–04	26 APR 2005
	STANDARD: JEDEC MS–013 AD	

DW SUFFIX
EG (Pb-FREE) SUFFIX
PLASTIC PACKAGE
98ASB42344B
ISSUE F

33884

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	6/2006	• Implemented Revision History page • Converted to Freescale format • Corrected content to the prevailing form and style • Removed MC33884EG/R2, and replaced with MCZ33884EG/R2 in the Ordering Information block
4.0	11/2006	• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum ratings on page 5. Added note with instructions from www.freescale.com.

TM