Product Change Notification / SYST-05QQMU831

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Product Category:

32-bit Microcontrollers

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Document Change

Notification Subject:

ERRATA - SAM L22 Family Silicon Errata and Data Sheet Clarificaiton

Affected CPNs:

SYST-05QQMU831_Affected_CPN_09072022.pdf
SYST-05QQMU831_Affected_CPN_09072022.csv

Notification Text:

SYST-05QQMU831

Microchip has released a new Errata for the SAM L22 Family Silicon Errata and Data Sheet Clarificaiton of devices. If you are using one of these devices please read the document located at SAM L22 Family Silicon Errata and Data Sheet Clarificaiton.

Notification Status: Final

Description of Change: Rev. E Document (09/2022) The following Errata were added in this revision: • PORT: 1.6.2 PA24 and PA25 Pull-down Functionality • ADC: 1.11.7 SEQSTATE • BOD33: 1.19.1 Hysteresis

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 06 Sep 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM L22 Family Silicon Errata and Data Sheet Clarificaiton

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Affected Catalog Part Numbers (CPN)

ATSAML22G16A-AUT
ATSAML22G16A-MUT
ATSAML22G17A-AUT
ATSAML22G17A-MUT
ATSAML22G17A-UUT
ATSAML22G17A-UUTA0
ATSAML22G17A-UUTA1
ATSAML22G17A-UUTA2
ATSAML22G18A-AUT
ATSAML22G18A-MUT
ATSAML22G18A-UUT
ATSAML22J16A-AU
ATSAML22J16A-AUT
ATSAML22J16A-MUT
ATSAML22J17A-AUT
ATSAML22J17A-MUT
ATSAML22J18A-AUT
ATSAML22J18A-MUT
ATSAML22N16A-AUT
ATSAML22N16A-CFUT
ATSAML22N17A-AUT
ATSAML22N17A-CFUT
ATSAML22N18A-AUT
ATSAML22N18A-CFUT

SAM L22 Family

SAM L22 Family Silicon Errata and Data Sheet Clarification

SAM L22 Family

The SAM L22 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001465B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the SAM L22 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 2. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L22 Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])	
		A	B
ATSAML22N18A	0x10820x00	0x0	0x1
ATSAML22N17A	0x10820x01		
ATSAML22N16A	0x10820x02		
ATSAML22J18A	0x10820x05		
ATSAML22J17A	0x10820x06		
ATSAML22J16A	0x10820x07		
ATSAML22G18A	0x10820x0A		
ATSAML22G17A	0x10820x0B		
ATSAML22G16A	0x10820x0C		

Note: Refer to the “Device Services Unit” chapter in the current Device Data Sheet (DS60001465B) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Errata Summary

Table 2. Silicon Errata Summary

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
AC	AC0 with PA02 Input	1.1.1	After a Power-on Reset (POR), the capacitance on PA02 is offset by an amount that slowly decays during 5 seconds, making any touch-related measurements on this pin is unreliable.	X	X

.....continued

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
PM	Low-Power Configuration	1.2.1	If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.	X	
PM	Regulator in Standby Mode	1.2.2	Writing PM.STDBYCFG.VREGSMOD to one does not set the main voltage regulator in Standby mode, the low-power regulator is still used in Standby mode.	X	X
DFLL48M	Write Access to DFLL Register	1.3.1	The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.	X	X
DFLL48M	Out of Bounds Interrupt	1.3.2	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X
DFLL48M	DFLL Status Bit in USB Clock Recovery Mode	1.3.3	The DFLL status bits in the STATUS register during the USB Clock Recovery mode can be wrong after a USB suspend state.	X	X
DMAC	Disable a Trigger From the Module	1.4.1	A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode.	X	
DMAC	Linked Descriptor	1.4.2	When using many DMA channel and if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.	X	X
DMAC	Linked Descriptors	1.4.3	When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR), or an incorrect descriptor fetch.	X	X
FDPLL	FDPLL Jitter	1.5.1	Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification.	X	
FDPLL	DPLLRATIO Register	1.5.2	When FDPLL ratio value in DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.	X	X
PORT	PORT Read/Write on Non-Implemented Register	1.6.1	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.	X	X
PORT	PA24 and PA25 Pull-down Functionality	1.6.2	Pull-down functionality is not available on GPIO pins, PA24 and PA25.	X	X
SUPC	Buck Converter Mode	1.7.1	Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode.	X	X
SUPC	Buck Converter as a Main Voltage Regulator	1.7.2	When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.	X	X
Device	VBAT in Battery Back Up Mode	1.8.1	When VBAT>VDDANA, in battery Backup mode or in battery Forced mode (SUPC.BBPS.CONF=FORCED) an over consumption appears due to high voltage on PC00, PC01, PB00, PB01, PB02 pins.	X	
Device	Excess Current Consumption and SLCD	1.8.2	When LCD feature is enable and (VLCD - VDD) > 0.7V, an extra consumption occurs.	X	
Device	Excess Current Consumption	1.8.3	When ABS (VLCD - VDD) < 50 mV, an extra consumption can occur on VLCD (if VLCD generated externally) or on VDD (if VLCD generated internally).	X	
Device	Standby entry	1.8.4	Potential hard fault upon standby entry when Systick interrupt is enabled.	X	X
PTC	PTC Lines Incorrect Mapping	1.9.1	Five PTC lines are mapped on PC00, PC01, PB00, PB01, PB02 instead of PC05, PC06, PA11, PA10, PA09.	X	

.....continued

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
ADC	ADC Result in Unipolar Mode	1.10.1	The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolutions.	X	X
ADC	Synchronized Event During ADC Conversion	1.10.2	If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event, causing a stall of the event channel.	X	X
ADC	Free Running Mode	1.10.3	In Standby Sleep mode, when the ADC is in Free-Running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.	X	X
ADC	SYNCBUSY.SWTRIG Bit	1.10.4	ADC SYNCBUSY.SWTRIG get stuck to one after wake up from Standby Sleep mode.	X	X
ADC	Effective Number of Bits	1.10.5	The ADC effective number of bits (ENOB) is 9.2 in this revision.	X	
ADC	Power Consumption	1.10.6	Power consumption for up to 1.6 seconds on VDDANA when the ADC is disabled manually or automatically.	X	
ADC	SEQSTATE	1.10.7	The SEQSTATUS synchronization is not managed properly when the system comes out of standby mode, leading to a wrong SEQSTATE value read in the first SEQSTATUS update of the sequence.	X	X
TC	SYNCBUSY Flag	1.11.1	When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	X	X
RTC	RTC Tamper Interrupt	1.12.1	When the tamper controller is configured for asynchronous detection, an RTC tamper interrupt can occur while the RTC is disabled.	X	
RTC	Tamper Interrupt and Timestamp	1.12.2	When the tamper controller is configured for time stamp capture, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.	X	
RTC	Active Layer Mode and DMA	1.12.3	When the tamper controller is configured for ACTL, the mismatch signal used to qualify the DMA and interrupt triggers produces different results.	X	
RTC	Active Layer Mode and Timestamp	1.12.4	When the tamper controller is configured for Active Layer mode, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.	X	
RTC	Active Layer Mode with Input 4 and Timestamp	1.12.5	When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the RTC tamper interrupt occurs before the TIMESTAMP register is updated.		X
RTC	Active Layer Mode with Input 4 and DMA	1.12.6	When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the mismatch signal used to qualify the DMA and interrupt triggers produces different results.		X
RTC	RTC with PB01 IO	1.12.7	If PB01 is multiplexed to RTC peripheral (RTC/IN2), the system will always see this input pin as logic '0' when Backup mode is entered. If the detection transition TAMPCTRL.TAMLVL2 = 0, it might falsely wake up the system.	X	X
RTC	Tamper Detection When RTC Disabled	1.12.8	When the tamper controller is configured for CAPTURE while the RTC is disabled, there is a noisy pin.	X	X
TCC	Advance Capture Mode	1.13.1	Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) does not work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX do not work.	X	X
TCC	SYNCBUSY Flag	1.13.2	When clearing the STATUS.xxBUFV flag, the SYNCBUSY is released before the register is restored to its appropriate value.	X	X

.....continued

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
TCC	MAX Capture Mode	1.13.3	In Capture mode using MAX Capture mode, timer set in up counting mode, if an input event occurred within 2 cycles before TOP, the value captured is zero instead of TOP.	X	X
TCC	Dithering Mode	1.13.4	Using TCC in Dithering mode with external retrigger events, can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses.	X	X
SERCOM	USART in Auto-baud Mode	1.14.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X
SERCOM	SERCOM Instances	1.14.2	SAML22G devices delivered before date code 1716 only have 3 SERCOMs available (0,1,2) instead of 4 (0,1,2,3).	X	X
SERCOM	Parity Error in ISO7816 T0 Mode	1.14.3	In ISO7816 T0 mode when start of frame detect is enabled (CTRLB.SFDE=1), if there is a parity error, receive start (INTFLAG.RXS) can be erroneously set.	X	X
SERCOM	SDA and SCL Fall Time	1.14.4	When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	X	X
SERCOM	SERCOM_USART: Overconsumption in Standby Mode	1.14.5	Unexpected over consumption in Standby mode	X	X
SERCOM	SERCOM_I^2C: Status Flag	1.14.6	The CLKHOLD Status bit is not read-only.	X	X
EIC	EIC_ASYNCH Register	1.15.1	Access to EIC_ASYNCH register in 8-bit or16-bit mode is not functional.	X	X
EIC	Low Level or Rising Edge or Both Edges	1.15.2	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.	X	X
EIC	NMI Configuration	1.15.3	Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.	X	X
EIC	Asynchronous Edge Detection	1.15.4	When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges won't generate events until the system wakes up.	X	X
TRNG	Power Consumption in Standby Mode	1.16.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	X	X
EVSYS	Synchronous Path	1.17.1	Using synchronous, spurious overrun can appear with generic clock for the channel always on.	X	X
EVSYS	Overrun Flag	1.17.2	The acknowledge between an event user and the EVSYS, clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later.	X	X
BOD33	Hysteresis	1.18.1	Hysteresis could not work properly if a reset occurs when the power supply is in the hysteresis phase.	X	X

Table of Contents

1. Silicon Errata Issues

The following issues apply to the SAM L22 family of devices.

Note: The silicon errata listed in this document supersedes the Errata Chapter 49 in SAM L22 product data sheet (DS60001465B).

1.1 Analog Comparator (AC)

1.1.1 AC0 with PA02 Input

After a Power-on Reset (POR), the capacitance on PA02 is offset by an amount that slowly decays during 5 seconds, making any touch-related measurements on this pin is unreliable.

Workaround
To get rid of this offset, reconfigure the AC0 input muxes to use internal inputs instead of AC0 pin 0 (default reset value) before starting any touch-related measurements (COMPCTRL0.MUXPOS = 4,COMPCTRL0.MUXNEG = 5).

Affected Silicon Revisions

A	B						
X	X						

1.2 Power Manager

1.2.1 Low-Power Configuration

If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.

Workaround
Before entering in Standby mode, switch the GCLK_MAIN to the OSCULP32K clock. After wake-up, switch back to the GCLK_MAIN clock.

Affected Silicon Revisions

A	B						
X							

1.2.2 Regulator in Standby Mode

Writing PM.STDBYCFG.VREGSMOD to one does not set the main voltage regulator in Standby mode, the low-power regulator is still used in Standby mode.

Workaround
Set SUPC.VREG.RUNSTDBY to one.

Affected Silicon Revisions

A	B						
X	X						

1.3 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.3.1 Write Access to DFLL Register

The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.

Workaround
Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

A	B						
X	X						

1.3.2 Out of Bounds Interrupt

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround
Check the lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

A	B						
X	X						

1.3.3 DFLL Status Bit in USB Clock Recovery Mode

The DFLL status bits in the STATUS register during the USB Clock Recovery mode can be wrong after a USB suspend state.

Workaround
Do not monitor the DFLL status bits in the STATUS register during the USB Clock Recovery mode.

Affected Silicon Revisions

A	B						
X	X						

1.4 Direct Memory Access Controller (DMAC)

1.4.1 Disable a Trigger From the Module

A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode, for example, DAC, LCD, and SERCOM in transmission mode.

Workaround
If the module generating the trigger also generates event, use event interface instead of triggers with DMAC, for example, SLCD.

Affected Silicon Revisions

A	B						
X							

1.4.2 Linked Descriptor

When using many DMA channel and if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.

Workaround
Do not use linked descriptors, instead make a software link.

1. Replace the channel which used linked descriptor by two channels DMA (with linked descriptor disabled) handled by two channels event system:
   - DMA channel 0 transfer completion can send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL= BLOCK for channel 0 and configuration CHCTRLB.EVACT = CBLOCK for channel 1)
   - On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
   - Then DMA channel 1 transfer completion can send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL= BLOCK for channel 1 and configuration CHCTRLB.EVACT = CBLOCK for channel 0)
   - On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
   - The mechanism can be launched by sending a software event on the DMA channel 0

Affected Silicon Revisions

A	B						
X	X						

1.4.3 Linked Descriptors

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR), or an incorrect descriptor fetch.

Workaround
This happens if the channel number of the channels being enabled is lower than the channels already active.

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

Affected Silicon Revisions

A	B						
X	X						

1.5 96 MHz Fractional Digital Phase Locked Loop (FDPLL)

1.5.1 FDPLL Jitter

Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification. The maximum supported input reference clock is 1 MHz.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

1.5.2 DPLLRATIO Register

When FDPLL ratio value in DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround
Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

Affected Silicon Revisions

A	B						
X	X						

1.6 PORT - I/O Pin Controller

1.6.1 PORT Read/Write on Non-Implemented Register

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB, PC), do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

A	B						
X	X						

1.6.2 PA24 and PA25 Pull-Down Functionality

The pull-down functionality is not available on these GPIO pins: PA24 and PA25.

Workaround
None.

Affected Silicon Revisions

A	B						
X	X						

1.7 Supply Controller (SUPC)

1.7.1 Buck Converter Mode

Buck Converter mode is not supported when using Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M). As a result, Table 45-7 “Active Current Consumption - Active Mode” data for Buck Converter mode with FDPLL96M configuration is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL and DFLL.

Affected Silicon Revisions

A	B						
X	X						

1.7.2 Buck Converter as a Main Voltage Regulator

When Buck converter is set as main voltage regulator (SUPC.VREG.SEL= 1), the microcontroller can freeze when leaving Standby mode.

Workaround
Enable the main voltage regulator in Standby mode (SUPC.VREG.RUNSTDBY = 1) and set the Standby in PL0 bit to one (SUPC.VREG.STDBYPL0 = 1).

Note: When SUPC.VREG.STDBYPL0 = 1, In Standby mode, the voltage regulator is used in PL0.

Affected Silicon Revisions

A	B						
X	X						

1.8 Device

1.8.1 VBAT in Battery Back Up Mode

When VBAT > VDDANA, in battery Backup mode or in battery Forced mode (SUPC.BBPS.CONF = FORCED) an over consumption appears due to high voltage on the PC00, PC01, PB00, PB01, and PB02 pins.

Workaround
The PC00, PC01, PB00, PB01, and PB02 pins should be tied to GND.

Affected Silicon Revisions

A	B						
X							

1.8.2 Excess Current Consumption and SLCD

When LCD feature is enable and (VLCD - VDD) > 0.7V, an extra consumption occurs. If VLCD internally generated, the VLCD voltage will be out of specification.

Workaround
The LCD feature must be used only when (VLCD - VDD) < 0.7V.

Affected Silicon Revisions

A	B						
X							

1.8.3 Excess Current Consumption

When ABS (VLCD - VDD) < 50 mV, an extra consumption can occur on VLCD (if VLCD generated externally) or on VDD (if VLCD generated internally).

Workaround
ABS (VLCD - VDD) should be greater than 50 mV.

Affected Silicon Revisions

A	B						
X							

1.8.4 Standby Entry

When the Systick interrupt is enabled and the standby back-bias option is set (STDBYCFG.BBIAS = 1), a hard fault can occur when the Systick interrupt coincides with the standby entry.

Workaround
Disable the Systick interrupt before entering standby and re-enable it after wake up.

Affected Silicon Revisions

A	B						
X	X						

1.9 Peripheral Touch Controller (PTC)

1.9.1 PTC Lines Incorrect Mapping

Five PTC lines are mapped on PC00, PC01, PB00, PB01, PB02 instead of PC05, PC06, PA11, PA10, and PA09.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

1.10 Analog-to-Digital Converter (ADC)

1.10.1 ADC Result in Unipolar Mode

The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolutions.

Workaround
Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

Affected Silicon Revisions

A	B						
X	X						

1.10.2 Synchronized Event During ADC Conversion

If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event, causing a stall of the event channel.

Workaround
When using events with the ADC, only the asynchronous path from the event system must be used.

Affected Silicon Revisions

A	B						
X	X						

1.10.3 Free Running Mode

In Standby mode, when the ADC is in Free-Running mode (CTRLC.FREERUN = 1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY = 0), the ADC keeps requesting its generic clock.

Workaround
Stop the free-running mode (CTRLC.FREERUN = 0) before entering Standby mode

Affected Silicon Revisions

A	B						
X	X						

1.10.4 SYNCBUSY.SWTRIG Bit

ADC SYNCBUSY.SWTRIG get stuck to one after wake up from Standby mode.

Workaround
Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby mode. ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a ‘1’ to SWTRIG.START.

Affected Silicon Revisions

A	B						
X	X						

1.10.5 Effective Number of Bits

The ADC effective number of bits (ENOB) is 9.2 in this revision.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

1.10.6 Power Consumption

Power consumption for up to 1.6 seconds on VDDANA when the ADC is disabled manually or automatically.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

1.10.7 SEQSTATE

In the ADC, the SEQSTATUS synchronization is not managed properly when the system comes out of Standby mode, leading to a wrong SEQSTATE value read in the first SEQSTATUS update of the sequence. This happens when the ADC is in SleepWalking mode and the conversion sequence is launched before a full wake up from Standby mode.

Workaround
Trigger the wake up of the chip before the conversion sequence is launched rather than when its result is ready.

Affected Silicon Revisions

A	B					
X	X					

1.11 Timer/Counter (TC)

1.11.1 SYNCBUSY Flag , TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround
Successively clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is restored before updating it.

Affected Silicon Revisions

A	B						
X	X						

1.12 Real-Time Counter (RTC)

1.12.1 RTC Tamper Interrupt

When the tamper controller is configured for asynchronous detection, an RTC tamper interrupt can occur while the RTC is disabled.

Workaround
Set the tamper interrupt enable only when the RTC is enabled.

- Program INTEN.TAMPER = 1 after setting the CTRLA.ENABLE register and clearing the INTFLAG.TAMPER register.
- Program INTEN.TAMPER = 0 before clearing the CTRLA.ENABLE register.

Affected Silicon Revisions

A	B						
X							

1.12.2 Tamper Interrupt and Timestamp

When the tamper controller is configured for time stamp capture, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

Two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update.
2. Implement a wait loop to create a delay when the tamper interrupt handler routine begins to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period. For example,
   - If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms.
   - If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us.

Affected Silicon Revisions

A	B						
X							

1.12.3 Active Layer Mode and DMA

When the tamper controller is configured for ACTL, the mismatch signal used to qualify the DMA and interrupt triggers produces different results. The DMA implements a level-detection whereas the interrupt implements an edge-detection. The result is that the DMA may trigger frequently from the same mismatch compared to the interrupt which will only trigger once.

Workaround

If no other tamper configurations are implemented (that is, other TAMPCTRL.INxACT! = WAKE/CAPTURE and EVCTRL.EVEI = 0), do not enable the DMA if possible to prevent performance degradation.

Affected Silicon Revisions

A	B						
X							

1.12.4 Active Layer Mode and Timestamp

When the tamper controller is configured for Active Layer mode, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

Two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update.
2. Implement a wait loop to create a delay when the tamper interrupt handler routine begins to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period. For example,
   - If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms.
   - If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us.

Affected Silicon Revisions

A	B						
X							

1.12.5 Active Layer Mode with Input 4 and Timestamp

When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT = 3), the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

The following two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update. Refer Errata 1.13.6.
2. Implement a wait loop to create a delay, when the tamper interrupt handler routine begins, to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period.

For example,

- If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms.
- If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us.

Affected Silicon Revisions

A	B							
	X							

1.12.6 Active Layer Mode with Input 4 and DMA

When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT = 3), the mismatch signal used to qualify the DMA and interrupt triggers produces different results. The DMA implements a level-detection whereas the interrupt implements an edge-detection. The result is that the DMA may trigger frequently from the same mismatch compared to the interrupt which will only trigger once.

Workaround

The following three workarounds are available:

1. Tamper inputs 0, 1, 2 and 3 can be configured for active layer with DMA.
2. Tamper input 4 can be configured with DMA for any mode other than active layer.
3. If Tamper input 4 is to be used in active layer, do not enable the DMA, to prevent performance degradation.

Affected Silicon Revisions

A	B							
	X							

1.12.7 RTC with PB01 IO

If PB01 is multiplexed to RTC peripheral (RTC/IN2), the system will always see this input pin as logic ‘0’ when Backup mode is entered. If the detection transition TAMPCTRL.TAMLVL2 = 0, it might falsely wake up the system.

Workaround

If the system is expected to enter Backup mode, use other tamper pins (IN0/IN1/IN3/IN4) for tamper detection.

Affected Silicon Revisions

A	B						
X	X						

1.12.8 Tamper Detection When RTC Disabled

When the tamper controller is configured for CAPTURE while the RTC is disabled, a noisy pin can trigger the following once the RTC is enabled:

- The timestamp capture
- The tamper interrupt if enabled
- The DMA trigger if enabled

Workaround

1. Set the tamper interrupt enable only when the RTC is enabled:
   – Clear the tamper interrupt flags and ID registers (INTFLAG.TAMPER & TAMPID.TAMPIDx registers).
   – Enable RTC (CTRLA.ENABLE = 1).
   – Enable the tamper interrupt (INTEN.TAMPER = 1).

   To disable the RTC, disable the Tamper interrupts before disabling the RTC.

   – Disable Tamper interrupts (INTEN.TAMPER = 0).
   – Disable the RTC (CTRLA.ENABLE = 0).
2. Issue a CPU read of the TIMESTAMP register immediately after the RTC is enabled. This releases the register lock allowing the capture of the next and valid tamper. This releases the DMA trigger of the erroneous capture tamper.

Affected Silicon Revisions

A	B						
X	X						

1.13 Timer/Counter for Control Applications (TCC)

1.13.1 Advance Capture Mode

Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) does not work if an upper channel is not in one of these modes, for example, when CC[0] = CAPTMIN, CC[1] = CAPTMAX, CC[2] = CAPTEN, and CC[3] = CAPTEN, CAPTMIN and CAPTMAX do not work.

Workaround

Basic Capture mode must be set in lower channel, and advance Capture mode in upper channel, for example, CC[0] = CAPTEN , CC[1] = CAPTEN , CC[2] = CAPTMIN, CC[3] = CAPTMAX.

All capture will be done as expected.

Affected Silicon Revisions

A	B						
X	X						

1.13.2 SYNCBUSY Flag

When clearing the STATUS.xxBUFV flag, the SYNCBUSY is released before the register is restored to its appropriate value.

Workaround
To ensure that the register value is restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared twice.

Affected Silicon Revisions

A	B						
X	X						

1.13.3 MAX Capture Mode

In Capture mode using MAX Capture mode, timer set in up counting mode, if an input event occurred within 2 cycles before TOP, the value captured is zero instead of TOP.

Workaround
Two possible options are as follows:

- If event is controllable, capture event should not occur when counter is within 2 cycles before TOP value.
- Use timer in down Counter mode and capture MIN value instead of MAX.

Affected Silicon Revisions

A	B						
X	X						

1.13.4 Dithering Mode

Using TCC in Dithering mode with external retrigger events, can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses.

Workaround
Do not use retrigger events or actions when TCC is configured in Dithering mode.

Affected Silicon Revisions

A	B						
X	X						

1.14 Serial Communication Interface (SERCOM)

1.14.1 USART in Auto-baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround
None.

Affected Silicon Revisions

A	B						
X	X						

1.14.2 SERCOM Instances

The SAML22G devices delivered before date code 1716 only have 3 sercoms available (0,1,2) instead of 4 (0,1,2,3).

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

1.14.3 Parity Error in ISO7816 T0 Mode

In ISO7816 T0 mode when start of frame detect is enabled (CTRLB.SFDE = 1), if there is a parity error, receive start (INTFLAG.RXS) can be erroneously set. This is because the transmitted parity low is also seen by the receiver and looks like a start of frame.

Workaround

Clear INTFLAG.RXS when received on parity error.

Affected Silicon Revisions

A	B						
X	X						

1.14.4 SDA and SCL Fall Time

When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.

Workaround

When reflection is observed a 100 ohms serial resistor can be added on the impacted line.

Affected Silicon Revisions

A	B						
X	X						

1.14.5 SERCOM-USART: Overconsumption in Standby Mode

When SERCOM USART CTRLA.RUNSTDBY = 0 and the Receiver is disabled (CTRLB.RXEN = 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected over consumption.

Workaround

Configure CTRLA.RXPO and CTRLA.TXPO to use the same SERCOM PAD for RX and TX, or add an external pull-up on the RX pin.

Affected Silicon Revisions

A	B						
X	X						

1.14.6 SERCOM I^2C: Status Flag

The STATUS.CLKHOLD bit in Host mode and Client mode can be written whereas it is a read-only status bit.

Workaround
Do not clear the STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A	B						
X	X						

1.15 External Interrupt Controller (EIC)

1.15.1 EIC_ASYNCH Register

Access to the EIC_ASYNCH register in 8-bit or16-bit mode is not functional.

- Writing in 8-bit mode will also write this byte in all bytes of the 32-bit word
- Writing higher 16-bits will also write the lower 16-bits
- Writing lower 16-bits will also write the higher 16-bits

Workaround

Two workarounds are available:

- Use 32-bit write mode
- Write only lower 16-bits (This will write upper 16-bits also, but does not impact the application)

Affected Silicon Revisions

A	B						
X	X						

1.15.2 Low Level or Rising Edge or Both Edges

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

Workaround
Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

A	B						
X	X						

1.15.3 NMI Configuration

Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.

Workaround
Clear the NMIFLAG bit once the NMI has been modified.

Affected Silicon Revisions

A	B						
X	X						

1.15.4 Asynchronous Edge Detection

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges won't generate events until the system wakes up.

Workaround
Asynchronous edge detection doesn't work, instead use the synchronous edge detection (ASYNCH.ASYNCH[x] = 0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL= 1).

Affected Silicon Revisions

A	B						
X	X						

1.16 True Random Number Generator (TRNG)

1.16.1 Power Consumption in Standby Mode , MATH100-7

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround
Disable the TRNG module twice:

- TRNG -> CTRLA.reg = 0;
- TRNG -> CTRLA.reg = 0;

Affected Silicon Revisions

A	B						
X	X						

1.17 Event System (EVSYS)

1.17.1 Synchronous Path

Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround

- Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to 1.
- No penalty is introduced.

Affected Silicon Revisions

A	B						
X	X						

1.17.2 Overrun Flag

The acknowledge between an event user and the EVSYS, clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround
For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.

Affected Silicon Revisions

A	B						
X	X						

1.18 BOD33

1.18.1 Hysteresis

The BOD33 hysteresis does not work if either an external reset or watchdog reset occurs when the supply voltage is between VBOD(min.) and VBOD(max.). If one of those resets occurs, the device will start operating if the supply voltage is below VBOD(max.) but above VBOD(min.) and the reset condition is lifted.

Workaround
Disable the BOD33/BODVDD hysteresis (BOD33.HYST = 0 or BODVDD.HYST = 0) and create a virtual hysteresis by configuring:

- The BOD33 threshold level at power-on (BOD_LEVEL) in the NVM User Row as the upper BOD threshold (VBOD(max.)).
- The SUPC BOD33.LEVEL/BODVDD.LEVEL bit field as the lower BOD threshold (VBOD(min.)).

Affected Silicon Revisions

A	B						
X	X						

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001465B).

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Maximum Clock Frequencies

The Table 44-6. Maximum Peripheral Clock Frequencies was updated with the following items, just the updated areas are shown:

Symbol	Description	Max		Units
		PL0	PL2	
FGCLK_DFLL48M_REF	DFLL48M Reference clock frequency	NA	33	**kHz**
$f_{GCLK\_FDPLL96M}$	FDPLL96M Reference clock frequency	2	2	MHz
$f_{GCLK\_FDPLL96M\_32K}$	FDPLL96M 32k Reference clock frequency	32	32	**kHz**

2.2 Power Consumption

Table 44-7. Active Current Consumption was updated with the following information:

Mode	Conditions	Regulator	PL	Clock	V_{DD}	Ta	Typ.	Max.	Units
ACTIVE	Coremark	LDO Mode	PL0	OSC 8MHz	1.8V	**Max. at 85°C Typ. at 25°C**	85	126	µA/MHz
					3.3V		90	131	
				OSC 4MHz	1.8V		94	181	
					3.3V		100	188	
			PL2	OSC 12MHz	1.8V		101	149	
					3.3V		106	151	
				FDPLL 32MHz	1.8V		87	100	
					3.3V		103	116	
		BUCK Mode	PL0	OSC 8MHz	1.8V		55	81	
					3.3V		41	57	
				OSC 4MHz	1.8V		62	116	
					3.3V		49	84	
			PL2	OSC 12MHz	1.8V		79	110	
					3.3V		52	76	
				FDPLL 32MHz	1.8V		63	75	
					3.3V		46	53	

.....continued

Mode	Conditions	Regulator	PL	Clock	V_{DD}	Ta	Typ.	Max.	Units
ACTIVE	FIBO	LDO Mode	PL0	OSC 8MHz	1.8V	**Max. at 85°C Typ. at 25°C**	69	111	µA/MHz
					3.3V		71	113	
				OSC 4MHz	1.8V		78	166	
					3.3V		81	170	
			PL2	OSC 12MHz	1.8V		85	130	
					3.3V		87	132	
				FDPLL 32MHz	1.8V		83	96	
					3.3V		83	96	
		BUCK Mode	PL0	OSC 8MHz	1.8V		44	71	
					3.3V		31	49	
				OSC 4MHz	1.8V		52	107	
					3.3V		39	76	
			PL2	OSC 12MHz	1.8V		66	103	
					3.3V		42	63	
				FDPLL 32MHz	1.8V		60	71	
					3.3V		35	42	
ACTIVE	While 1	LDO Mode	PL0	OSC 8MHz	1.8V	**Max. at 85°C Typ. at 25°C**	51	95	µA/MHz
					3.3V		53	97	
				OSC 4MHz	1.8V		60	151	
					3.3V		62	154	
			PL2	OSC 12MHz	1.8V		60	109	
					3.3V		62	111	
				FDPLL 32MHz	1.8V		56	75	
					3.3V		59	75	
		BUCK Mode	PL0	OSC 8MHz	1.8V		33	61	
					3.3V		25	43	
				OSC 4MHz	1.8V		41	97	
					3.3V		33	70	
			PL2	OSC 12MHz	1.8V		47	84	
					3.3V		31	54	
				FDPLL 32MHz	1.8V		43	55	
					3.3V		25	34	
IDLE2		BUCK	PL0	OSC 8MHz	1.8V	**Max. at 85°C Typ. at 25°C**	14	31	**µA/MHz**
					3.3V		12	23	

Table 44-9. Current Consumption – BACKUP and OFF Mode was updated:

Mode	conditions	V_{DD}	Ta	Typ.	Max.	Units
BACKUP	powered by V_{DDIO}, V_{DDANA}+V_{DDIO} consumption	1.8V	25°C	0.47	0.79	µA
			85°C	4.4	8.6	
		3.3V	25°C	0.55	0.9	
			85°C	5.7	9.9	
	powered by V_{DDIO}, V_{BAT} consumption	1.8V	25°C	0.000	0.00	
			85°C	0.013	0.009	
		3.3V	25°C	0.000	0.00	
			85°C	0.026	0.018	
	powered by V_{DDIO} with RTC running on OSCULP32K, V_{DDANA}+V_{DDIO} consumption	1.8V	25°C	0.55	0.88	
			85°C	4.4	8.7	
		3.3V	25°C	0.63	1.0	
			85°C	5.7	10.0	
	powered by V_{DDIO} with RTC running on OSCULP32K, V_{BAT} consumption	1.8V	25°C	0.000	0.00	
			85°C	0.008	0.009	
		3.3V	25°C	0.000	0.00	
			85°C	0.015	0.018	
BACKUP	powered by V_{BAT}, V_{DDANA}+V_{DDIO} consumption	1.8V	25°C	0.08	0.09	µA
			85°C	2.0	2.2	
		3.3V	25°C	0.14	0.2	
			85°C	3.2	3.5	
	powered by V_{BAT}, V_{BAT} consumption	1.8V	25°C	0.38	0.69	
			85°C	2.3	6.3	
		3.3V	25°C	0.41	0.73	
			85°C	2.4	6.4	
	powered by V_{BAT} with RTC running on OSCULP32K, V_{DDANA}+V_{DDIO} consumption	1.8V	25°C	0.08	0.09	
			85°C	2.1	2.3	
		3.3V	25°C	0.14	0.1	
			85°C	3.2	3.5	
	powered by V_{BAT} with RTC running on OSCULP32K, V_{BAT} consumption	1.8V	25°C	0.46	0.77	
			85°C	2.4	6.4	
		3.3V	25°C	0.49	0.81	
			85°C	2.5	6.6	
OFF	**V_{DDIN} + V_{DDANA} + V_{DDIO}**	1.8V	25°C	0.10	0.18	µA
			85°C	2.3	4.5	
		3.3V	25°C	0.18	0.39	
			85°C	3.6	7.5	

2.3 Analog Characteristics

2.3.1 Voltage Regulator Characteristics

Table 44-16. External Components requirements in switching mode was updated with the information shown in **bold**:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input regulator capacitor	**Tantalum or electrolytic dielectric**	**-**	**10**	**-**	µF
		Ceramic dielectric X7R	-	100	-	nF
C_{OUT}	Output regulator capacitor	**Tantalum or electrolytic dielectric**	**0.8**	**1**	**1.2**	µF
		Ceramic dielectric X7R	-	100	-	nF
L_{EXT}	External Inductance	Murata LQH3NPN100MJ0				
R_{SAT_LEXT}	ESR of L_{EXT}	-	-	-	0.7	Ω
I_{SAT_LEXT}	Saturation current	-	275	-	-	mA

Table 44-18. External Components requirements in linear mode was updated with the information shown in **bold**:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input regulator capacitor	**Tantalum or electrolytic dielectric**	**-**	**10**	**-**	µF
		Ceramic dielectric X7R	-	100	-	nF
C_{OUT}	Output regulator capacitor	**Tantalum or electrolytic dielectric**	**0.8**	**1**	**1.2**	µF
		Ceramic dielectric X7R	-	100	-	nF
ESR C_{OUT}	**External Series Resistance of C_{OUT}**	**-**	**-**	**-**	**0.5**	**Ω**

Table 44-19. Automatic Power Switch Characteristics was updated with the information shown in **bold**:

Symbol	Parameters	Typ.	Unit
CD	**Decoupling capacitor on VDDIN**	**10**	µF
THUP	VDD threshold	1.84	V
THDWN		1.75	V
THHYS	VDD hysteresis	90	mV

2.4 Analog-to-Digital (ADC) Characteristics

Table 44-25. Differential Mode was updated with the information shown in **bold**, just the updated areas are shown:

Symbol	Parameters	Conditions	Min	Typ.	Max	Unit
ENOB	Effective Number of bits (With gain compensation)	V_{DDANA}=3.0V / V_{ref} =2.0V	9.6	10.5	10.6	bits
		V_{DDANA}=1.6V/3.6V, V_{ref}=1.0V	8.9	9.7	9.9	
		V_{DDANA}=V_{ref}=1.6V	10	10.5	11.1	
		V_{DDANA}=V_{ref}=3.6V	10.5	10.9	11.0	
TUE	Total Unadjusted Error	V_{DDANA}=3.0V, V_{ref}=2.0V	-	7.5	11	LSB
INL	Integral Non Linearity	V_{DDANA}=3.0V, V_{ref}=2.0V	-	+/-1.5	+/-2.1	LSB
DNL	Differential Non Linearity	V_{DDANA}=3.0V, V_{ref}=2.0V	-	+/-0.8	+1.1/-1.0	LSB
GERR	Gain Error	External Reference voltage 1.0V	-	+/-0.7	+/-1.5	%
		External Reference voltage 3.0V		+/-0.2	0.5	
		Internal Reference INTREF=1.024V (SUPC.VREF.SEL=0x0)	-	+/-0.4	+/-4.4	
		V_{DDANA}		+/-0.1	0.4	
		V_{DDANA}/2	-	+/-0.4	+/-1.3	
		V_{DDANA}/1.6	-	+/-0.3	+/-0.9	
OERR	Offset Error	External Reference voltage 1.0V	-	+/-1.1	+/-2.4	mV
		External Reference voltage 3.0V		+/-1.1	3	
		Internal Reference INTREF=1.024V (SUPC.VREF.SEL=0x0)	-	+/-2.3	+/-7.5	
		V_{DDANA}		+/-0.9	2.9	
		V_{DDANA}/2	-	+/-1	+/-2.6	
		V_{DDANA}/1.6	-	+/-1	+/-2.9	
SFDR	Spurious Free Dynamic Range	F_s=1MHz / F_{in}=13 kHz / Full range Input signal V_{DDANA}=3.0V, V_{ref}=2.0V	68	75	77	dB
SINAD	Signal to Noise and Distortion ratio		60	65	66	
SNR	Signal to Noise ratio		61	66	67	
THD	Total Harmonic Distortion		-74	-73	-67	
	Noise RMS	External Reference voltage	-	1.0	2.5	mV

Table 44-26. Single-Ended Mode was updated with the information shown in **bold**, just the updated areas are shown:

Symbol	Parameters	Conditions	Min	Typ.	Max	Unit
ENOB	Effective Number of bits (With gain compensation)	V_{DDANA}=3.0V / V_{ref} =2.0V	8.5	9.5	9.8	bits
		V_{DDANA}=1.6V/3.6V, V_{ref}=1.0V	7.5	8.7	8.9	
		V_{DDANA}=V_{ref}=1.6V	9.0	9.5	9.8	
		V_{DDANA}=V_{ref}=3.6V	9.2	9.8	9.9	
TUE	Total Unadjusted Error	V_{DDANA}=3.0V, V_{ref}=2.0V	-	17.4	31	LSB
INL	Integral Non Linearity	V_{DDANA}=3.0V, V_{ref}=2.0V	-	+/-2.2	+/-10.1	LSB
DNL	Differential Non Linearity	V_{DDANA}=3.0V, V_{ref}=2.0V	-	+/-0.8	+/-0.9	LSB
GERR	Gain Error	External Reference voltage 1.0V	-	+/-1	+/-1.3	%
		External Reference voltage 3.0V		+/-0.3	+/-0.6	
		Internal Reference INTREF=1.024V (SUPC.VREF.SEL=0x0)	-	+/-0.4	+/-3.2	
		V_{DDANA}		+/-0.1	+/-0.3	
		V_{DDANA}/2	-	+/-0.6	+/-1.4	
		V_{DDANA}/1.6	-	+/-0.4	+/-1	
OERR	Offset Error	External Reference voltage 1.0V	-	+/-3.35	+/-13	mV
		External Reference voltage 3.0V		+/-3.6	+/-23.7	
		Internal Reference INTREF=1.024V (SUPC.VREF.SEL=0x0)	-	+/-1	+/-14.4	
		V_{DDANA}		+/-4.2	+/-24.8	
		V_{DDANA}/2	-	+/-5.7	+/-10.1	
		V_{DDANA}/1.6	-	+/-6.3	+/-13	
SFDR	Spurious Free Dynamic Range	F_s=1MHz / F_{in}=13 kHz / Full range Input signal V_{DDANA}=3.0V, V_{ref}=2.0V	65	71	78	dB
SINAD	Signal to Noise and Distortion ratio		53	59	61	
SNR	Signal to Noise ratio		53	59	61	
THD	Total Harmonic Distortion		-76	-70	64	
	Noise RMS	External Reference voltage	-	2.0	7.0	mV

The $t_{SAMPLEHOLD}$ equation at the end of the chapter 44.10.5 Analog-to-Digital (ADC) Characteristics was removed.

2.5 DETREF

The 44.10.7 Voltage Reference chapter name was updated to **44.10.7 DETREF.**

The Table 44-29. Reference Voltage Characteristics was updated with the information shown in **bold**, just the updated areas are shown:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ADC Ref	ADC internal reference	nom. 1.0V, V_{DDANA}=3.0V, T= 25°C	0.967	1.0	1.017	V
		nom. 1.1V, V_{DDANA}=3.0V, T= 25°C	1.069	1.1	1.120	V
		nom. 1.2V, V_{DDANA}=3.0V, T= 25°C	1.167	1.2	1.227	V
		nom. 1.25V, V_{DDANA}=3.0V, T= 25°C	1.214	1.3	1.280	V
		nom. 2.0V, V_{DDANA}=3.0V, T= 25°C	1.935	2.0	2.032	V
		nom. 2.2V, V_{DDANA}=3.0V, T= 25°C	2.134	2.2	2.242	V
		nom. 2.4V, V_{DDANA}=3.0V, T= 25°C	2.328	2.4	2.458	V
		nom. 2.5V, V_{DDANA}=3.0V, T= 25°C	2.420	2.5	2.565	V
	Ref Temperature coefficient	drift over [-40, +85]°C	-	[-0.01:+0.015]	-	%/°C
		drift over [25, +85]°C	-	[-0.01:+0.005]	-	%/°C
	Ref Supply coefficient	drift over [1.6, 3.6]V	-	[-0.35:+0.35]	-	%/V
AC Ref / Bandgap	AC Ref Accuracy	V_{DDANA}=3.0V, T= 25°C	1.073	1.1	1.123	V
	Ref Temperature coefficient	drift over [-40, +85]°C	-	[-0.01:+0.01]	-	%/°C
		drift over [25, +85]°C	-	[-0.005:+0.001]	-	
	Ref Supply coefficient	drift over[1.6, 3.6]V	-	[-0.35:+0.35]	-	%/V

3. Appendix A: Revision History

Rev. E Document (09/2022)
The following Errata were added in this revision:

- PORT: 1.6.2 PA24 and PA25 Pull-down Functionality
- ADC: 1.11.7 SEQSTATE
- BOD33: 1.19.1 Hysteresis

Rev. D Document (07/2021)
Terminology for “Master” and “Slave” was updated to “Host” and “Client” respectively. This change may not be reflected in all associated Microchip Documentation. For additional information, contact a Microchip support and sales representative.

The following Errata were added in this revision:

- SERCOM I2C: Status Flag

The following Data Sheet Clarifications were added:

- Maximum Clock Frequencies
- Power Consumption
- Analog Characteristics:
  - Voltage Regulator Characteristics
  - Analog-to-Digital (ADC) Characteristics
  - DETREF

Rev. C Document (01/2021)
The following errata were added in this revision:

- DEVICE: 1.8.4 Standby Entry
- SERCOM-USART: 1.15.5 Overconsumption in Standby mode

Rev. B Document (05/2019)
The following Errata have been updated:

- SUPC: Buck Converter Mode
- SYNCBUSY Flag
- Power Consumption in Standby Mode

ADC errata 1.16.1 and 1.16.2 were moved to 1.11.5 and 1.11.6 respectively for document clarity. This resulted in errata listed afterward to shift down by one in their number specification from the previous released document version.

Rev. A Document (08/2018)

- This is the initial released version of this document that lists the silicon errata issues which were documented in the SAM L22 product data sheet DS60001465A (Chapter 49)
- Added silicon errata: FDPLL Jitter
- Added silicon errata: Buck Converter Mode
- Added silicon errata: MAX Capture Mode

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