SiT9501

PRELIMINARY

Ultra-low Jitter Differential XO for Standard Networking Frequencies

Description

The SiT9501 is a differential MEMS oscillator that is engineered for low-jitter applications requiring standard frequencies from 25 MHz to 644.53125 MHz.

In addition to standard differential signaling types, a unique FlexSwing™ output-driver performs like LVPECL and provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9501 can be factory programmed for specific combinations of frequency, stability, output signaling, voltage, and output enable functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Standard frequencies from 25 MHz to 644.53125 MHz
- 70 fs RMS typical phase jitter, 12 kHz to 20 MHz
- 9 fs/mV typical PSNR
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ±20, ±25, ±30, and ±50 ppm frequency stabilities
- Wide temperature range (-40°C to 105°C)
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous power supply voltage range options
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package (Contact SiTime for 7 x 5, and 5 x 3.2 mm x mm packages)

Applications

- 400G/800G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment
- Test and measurement

Block Diagram

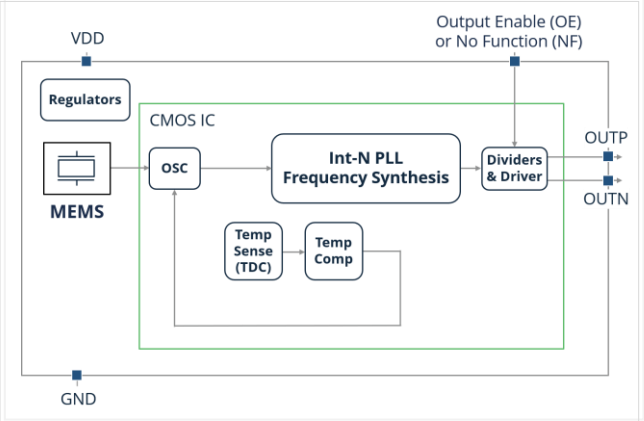


Figure 1. SiT9501 Block Diagram

Package Pinout

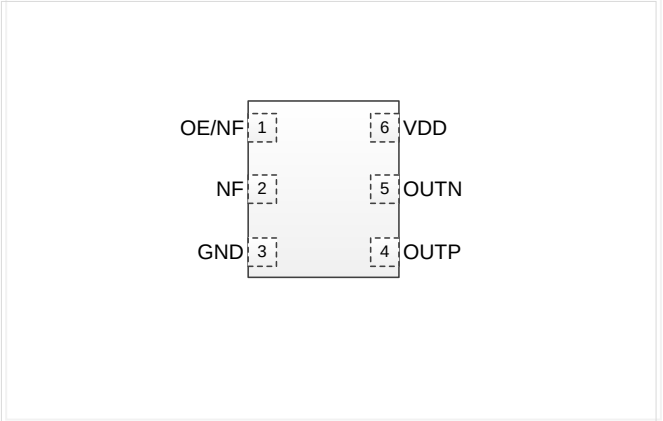


Figure 2. Pin Assignments (Top view)
(Refer to Table 15 for Pin Descriptions)

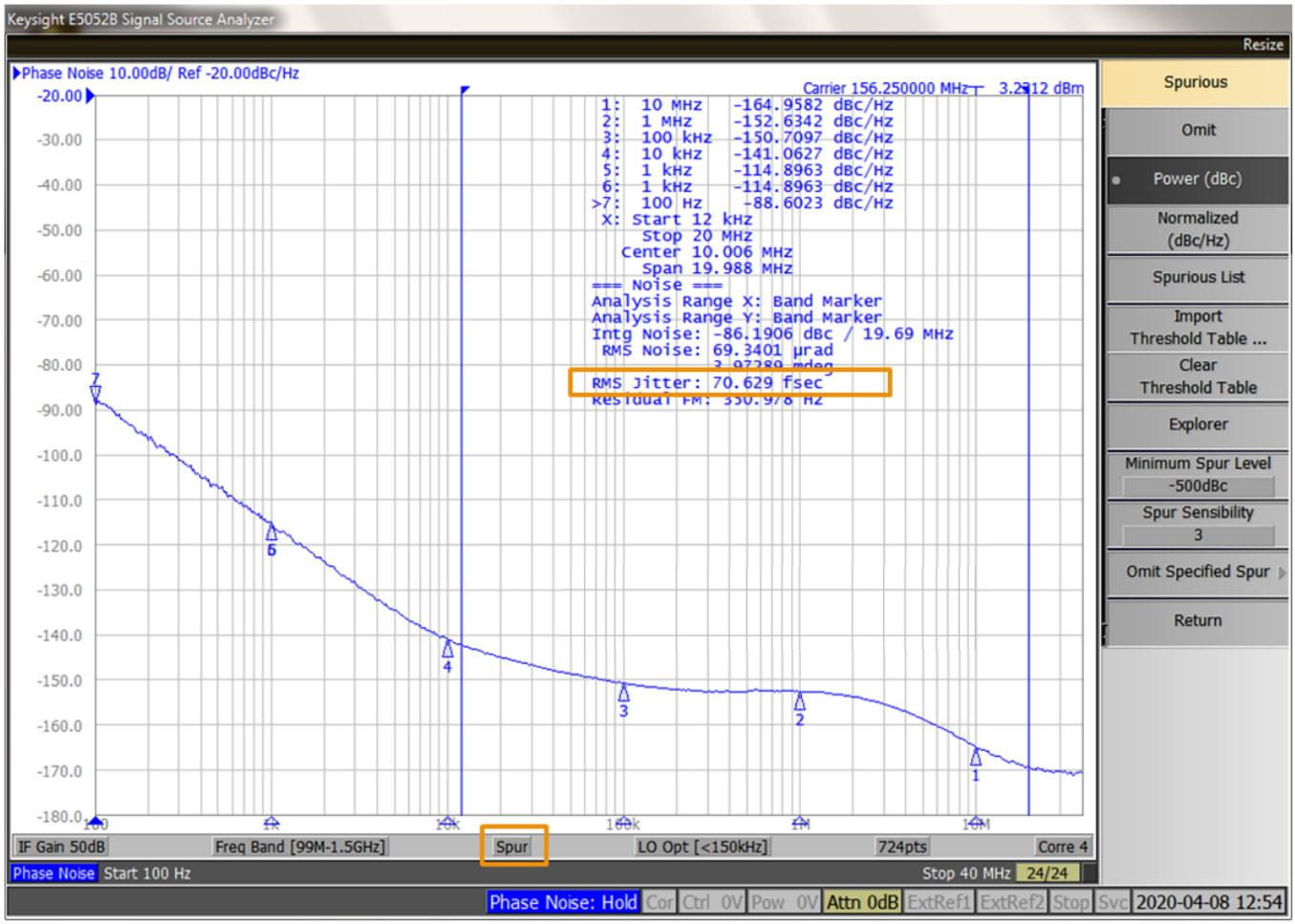
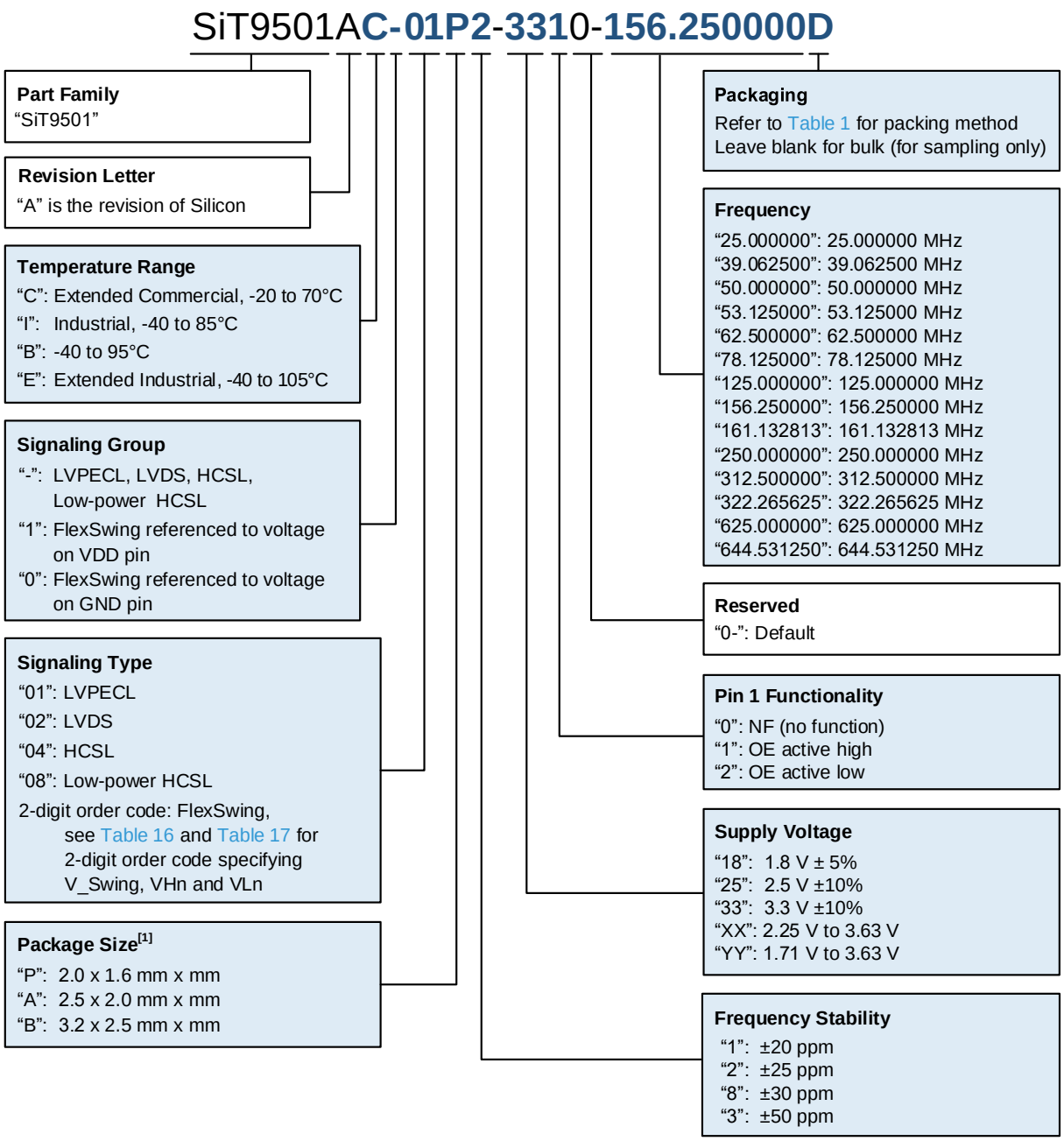


Figure 3. Typical Phase Noise Plot of 3.3 V 156.25 MHz LVPECL Device at 25°C, Spur turn on

Ordering Information



Note:

1. Contact SiTime for other package sizes.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See Test Circuit Diagrams for the test setups used with each signaling type.

Table 2. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 2 pF ± 10%, and 10 years aging at 85°C
		–	–	±25	ppm	
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±0.5	–	ppm	Ambient temperature of 85°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code “YY”
		2.25	–	3.63	V	Voltage-supply order code “XX”
		1.71	1.80	1.89	V	Voltage-supply order code “18”. Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code “25”
		2.97	3.30	3.63	V	Voltage-supply order code “33”
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Logic High function for Pin 1
Input Voltage Low	VIL	–	–	30%	Vdd	Logic High function for Pin 1
Input Pull-up/Pull-down Impedance	Z_in	112.9	120	133.4	kΩ	Pin 1 for OE function
Output Characteristics						
Duty Cycle	DC	48	–	52	%	See Figure 16 for waveform.
Startup, OE and SE Timing						
Startup Time	T_start	–	1.2	2	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time 1	T_oe	–	–	100+3 clock cycles	ns	For all signaling types except Low-Power HCSL. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 22 for waveform.
Output Enable Time 2	T_oe	–	–	500+3 clock cycles	ns	For Low-Power HCSL signaling type. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 22 for waveform.
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 23 for waveform.
Jitter and Phase Noise, measured at f = 156.25 MHz						
RMS Phase Jitter (random)	T_phj	–	70	100	fs	12 kHz to 20 MHz offset frequency integration bandwidth Contact SiTime for 85 fsec Max phase jitter option.
Spurious Phase Noise	T_spn	–	–	-112	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter[2]	T_jitt_per	–	0.5	0.6	ps	Measured based on 10K cycle.
Peak Cycle-to-cycle Jitter[2]	T_jitt_cc	–	3.5	6.2	ps	Measured based on 1K cycle

Note:

2. Measured according to JESD65B using Keysight DSAX91604A Oscilloscope.

Table 3. Electrical Characteristics – LVPECL | Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal supply voltage of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 5 and Figure 6 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	28.5	35.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	39	49	mA	Including load termination current as shown in Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms.
		–	39	45	mA	Including load termination current as shown in Figure 27 for Vdd=2.5 V ±10% and R3=220 Ohms.
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	55	61	mA	Including load termination current. See Figure 28 for termination.
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	46.5	58	mA	Including load termination current as shown in Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	46.5	53.5	mA	Including load termination current as shown in Figure 27 for Vdd=2.5 V ±10% and R3=220 Ohms. Driver output is at logic-high voltage levels.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	66	73	mA	Including load termination current. See Figure 28 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.075	Vdd-0.95	Vdd-0.86	V	See Figure 15 for waveform.
Output Low Voltage	VOL	Vdd-1.84	Vdd-1.7	Vdd-1.62	V	See Figure 15 for waveform.
Output Differential Voltage Swing	V_Swing	1.4	1.5	1.65	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	45	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	9	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2.0	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 5.
Power Supply-Induced Phase Noise	PSPN	–	-79	–	dBc	50 mV peak-peak ripple on VDD.
		–	-92	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 5.

Table 4. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to VDD only: 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 7 and Figure 8 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	29.5	38	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37	47.5	mA	Including load termination current, for FlexSwing order code "ER". See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms.
		–	37	43.5	mA	Including load termination current, for FlexSwing order code "ER". See Figure 27 for Vdd=2.5 V ±10%, and R3=220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	42.5	53	mA	Including load termination current, for FlexSwing order code "ER". See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	42.5	49.5	mA	Including load termination current, for FlexSwing order code "ER". See Figure 27 for Vdd=2.5 V ±10%, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn -0.13	VHn	VHn +0.1	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn -0.13	VLn	VLn +0.12	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. see Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER".
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER". Using RC power supply filter as shown in Figure 7.
Power Supply-Induced Phase Noise	PSPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "ER".
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "ER". Using R C power supply filter as shown in Figure 7.

Table 5. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to GND, only: 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 7 and Figure 8 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	31	37.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	38.5	44	mA	Including load termination current, for FlexSwing order code "3E". See Figure 27 for Vdd=1.8 V ±5% and R3=220 Ohms.
		–	38.5	45.5	mA	Including load termination current, for FlexSwing order code "3E". See Figure 27 for Vdd=1.71 V to 3.63 V and R3=220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	44.5	50	mA	Including load termination current, for FlexSwing order code "3E". See Figure 27 for Vdd=1.8 V ±5% and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	44.5	51.5	mA	Including load termination current, for FlexSwing order code "3E". See Figure 27 for Vdd=1.71 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.12	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.12	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	170	210	ps	20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	12	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "3E".
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "3E". Using RC power supply filter as shown in Figure 7.
Power Supply-Induced Phase Noise	PSPN	–	-76	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "3E".
		–	-95	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "3E". Using RC power supply filter as shown in Figure 7.

Table 6. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to GND, only: 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 7 and Figure 8 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	30	36	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37.5	44	mA	Including load termination current, for FlexSwing order code "VP". See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	46	53	mA	Including load termination current, for FlexSwing order code "VP". See Figure 27 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.11	VHn	VHn + 0.1	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 15 for waveform; Refer to Table 16 or Table 17 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "VP"
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "VP". Using RC power supply filter as shown in Figure 7.
Power Supply-Induced Phase Noise	PSPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "VP".
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "VP". Using RC power supply filter as shown in Figure 7.

Table 7. Electrical Characteristics – LVDS | Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 9 and Figure 10 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	25.5	32	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	29	35	mA	Including load termination current. See Figure 31 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	34.5	41	mA	Including load termination current. See Figure 31 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	360	450	mV	See Figure 17 for waveform.
Delta VOD	ΔVOD	–	–	50	mV	See Figure 17 for waveform.
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 17 for waveform.
Delta VOS	ΔVOS	–	–	50	mV	See Figure 17 for waveform.
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 31 for termination. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 21 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	18	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
	PSJS	–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 9
Power Supply-Induced Phase Noise	PSPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD.
	PSPN	–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 9.

Table 8. Electrical Characteristics – LVDS | Supply voltage ("order code"): 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 9 and Figure 10 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	25.5	32	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	29	35	mA	Including load termination current. See Figure 30 and Figure 31 termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	34.5	41	mA	Including load termination current. See Figure 30 and Figure 31 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	330	450	mV	See Figure 17 for waveform.
Delta VOD	ΔVOD	–	–	50	mV	See Figure 17 for waveform.
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 17 for waveform.
Delta VOS	ΔVOS	–	–	50	mV	See Figure 17 for waveform.
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 31 for termination. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 21 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	22.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 9.
Power Supply-Induced Phase Noise	PSPN	–	-71	–	dBc	50 mV peak-peak ripple on VDD.
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 9.

Table 9. Electrical Characteristics – HCSL | Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"), 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 11 and Figure 12 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	25	31	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	39.5	45	mA	Including load termination current. See Figure 32 for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	45	52	mA	Including load termination current. See Figure 32 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 15 for waveform.
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 15 for waveform.
Output Differential Voltage Swing	V_Swing	1.1	1.4	1.6	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	340	370	ps	Measured 20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±70	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	0	–	%	Measured as percent of V_Swing. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	27	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 11.
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 11.

Table 10. Electrical Characteristics – Low-Power HCSL | Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"), 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 13 and Figure 14 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	26	31.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	26.5	32	mA	Including load termination current. See Figure 33 for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	28.5	35	mA	Including load termination current. See Figure 33 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.92	1.15	V	See Figure 15 for waveform.
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 15 for waveform.
Output Differential Voltage Swing	V_Swing	1.6	1.83	2.0	V	See Figure 16 for waveform.
Rise/Fall Time	Tr, Tf	–	330	380	ps	Measured 20% to 80%. See Figure 16 for waveform.
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 18 for waveform.
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 19 for waveform.
Overshoot Voltage, peak	V_ov	–	1	–	%	Measured as percent of V_Swing. See Figure 20 for waveform.
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	18	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	6.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 13.
Power Supply-Induced Phase Noise	PSPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD.
		–	-82	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 13

Table 11. Absolute Maximum Ratings

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	135	°C

Table 12. Thermal Considerations[3]

Package	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	θ_{JB} (°C/W)	$\theta_{JC,Top}$ (°C/W)
3225, 6-pin	111	5.1	34	86
2520, 6-pin	126	4.8	39	118
2016 6-pin	149	3.9	40	163

Notes:

3. θ_{JA}, Ψ_{JT}, θ_{JB} and θ_{JC} are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25C ambient and 250 mW power consumption (typical of 1 GHz f_{out}). The conduction thermal resistances θ_{JB} and θ_{JC} are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads (θ_{JB}) or the top of the package ($\theta_{JC,Top}$). These may be used in a two-resistor compact model. The values of θ_{JA} and Ψ_{JT} are strongly application dependent, and we report values based on the JEDEC thermal environment. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. Ψ_{JT} can be used to estimate the junction temperature from measurements of the temperature at the top of the package if the thermal environment is similar to the JEDEC environment.

Table 13. Maximum Operating Junction Temperature[4]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80°C
85°C	95°C
95°C	105°C
105°C	115°C

Notes:

4. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 14. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	10,000	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)[5]	**MIL-STD-883F, Method 2003**	260	°C
Moisture Sensitivity Level	**MSL1 @ 260°C**		
Electrostatic Discharge (HBM)	**HBM, JESD22-A114**	2,000	V
Charge-Device Model ESD Protection	**JESD220C101**	750	V
Latch-up Tolerance	**JESD78 Compliant**		

Notes:

5. Please refer to SiTime Manufacturing Notes.

Pin Description

Table 15. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H[6]: Specified frequency output L[7]: OUT: Logic HIGH,
		No Function (NF)	Open, 120 kΩ internal pull-down resistor to GND
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions.[8]
3	GND	Power	Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[9]

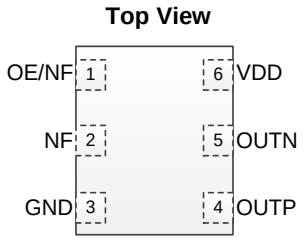


Figure 4. Pin Assignments

Notes:

6. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, the OE pin is recommended to include an external 10 kΩ resistor (Use 10kΩ pull-up if active high OE; use 10kΩ pull-down if active low OE) when the pin is not externally driven.
7. Differential Logic high means OUTP=VOH, OUTN=VOL
8. Can be left open. SiTime recommends grounding it for better thermal performance.
9. A capacitor of value 0.1 µF or higher between VDD and GND pins is required.

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL and additionally provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 16. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V)			VLn																					
			A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X
			Vdd-2.31V	Vdd-2.26V	Vdd-2.21V	Vdd-2.16V	Vdd-2.11V	Vdd-2.06V	Vdd-2.01V	Vdd-1.96V	Vdd-1.91V	Vdd-1.86V	Vdd-1.82V	Vdd-1.77V	Vdd-1.72V	Vdd-1.67V	Vdd-1.62V	Vdd-1.57V	Vdd-1.52V	Vdd-1.47V	Vdd-1.42V	Vdd-1.37V	Vdd-1.32V	Vdd-1.28V
VHn	A	VLn + V_Swing / 2									AJ 1.94	AK 1.86	AL 1.77	AM 1.69	AN 1.61	AP 1.52	AQ 1.44	AR 1.35	AS 1.27	AT 1.18	AU 1.10	AV 1.01	AW 0.93	AX 0.85
	B									1.94	BJ 1.86	BK 1.77	BL 1.69	BM 1.61	BN 1.52	BP 1.44	BQ 1.35	BR 1.27	BS 1.18	BT 1.10	BU 1.01	BV 0.93	BW 0.85	BX 0.76
	C								1.94	1.86	CJ 1.77	CK 1.69	CL 1.61	CM 1.52	CN 1.44	CP 1.35	CQ 1.27	CR 1.18	CS 1.10	CT 1.01	CU 0.93	CV 0.85	CW 0.76	CX 0.68
	D							1.94	1.86	1.77	DJ 1.69	DK 1.61	DL 1.52	DM 1.44	DN 1.35	DP 1.27	DQ 1.18	DR 1.10	DS 1.01	DT 0.93	DU 0.85	DV 0.76	DW 0.68	DX 0.59
	E						1.94	1.86	1.77	1.69	EJ 1.61	EK 1.52	EL 1.44	EM 1.35	EN 1.27	EP 1.18	EQ 1.10	ER 1.014	ES 0.93	ET 0.85	EU 0.76	EV 0.68	EW 0.59	EX 0.51
	F					1.94	1.86	1.77	1.69	1.61	FJ 1.52	FK 1.44	FL 1.35	FM 1.27	FN 1.18	FP 1.10	FQ 1.01	FR 0.93	FS 0.85	FT 0.76	FU 0.676	FV 0.59	FW 0.51	0.42
	G				1.94	1.86	1.77	1.69	1.61	GH 1.52	GJ 1.44	GK 1.35	GL 1.27	GM 1.18	GN 1.10	GP 1.01	GQ 0.93	GR 0.85	GS 0.76	GT 0.68	GU 0.59	GV 0.51	0.42	0.34
	H			1.94	1.86	1.77	1.69	1.61	HG 1.52	HH 1.44	HJ 1.35	HK 1.27	HL 1.18	HM 1.10	HN 1.01	HP 0.93	HQ 0.85	HR 0.76	HS 0.68	HT 0.59	HU 0.51	0.42	0.34	0.25
	J		1.94	1.86	1.77	1.69	1.61	JF 1.52	JG 1.44	JH 1.35	JJ 1.27	JK 1.18	JL 1.10	JM 1.01	JN 0.93	JP 0.85	JQ 0.76	JR 0.68	JS 0.59	JT 0.51	0.42	0.34	0.25	
	K		1.86	1.77	1.69	1.61	KE 1.52	KF 1.44	KG 1.35	KH 1.27	KJ 1.18	KK 1.10	KL 1.01	KM 0.93	KN 0.85	KP 0.76	KQ 0.68	KR 0.59	KS 0.51	0.42	0.34	0.25		
	L		1.77	1.69	1.61	LD 1.52	LE 1.44	LF 1.35	LG 1.27	LH 1.18	LJ 1.10	LK 1.01	LL 0.93	LM 0.85	LN 0.76	LP 0.68	LQ 0.59	LR 0.51	0.42	0.34	0.25			
	M		1.69	1.61	MC 1.52	MD 1.44	ME 1.35	MF 1.27	MG 1.18	MH 1.10	MJ 1.01	MK 0.93	ML 0.85	MM 0.76	MN 0.68	MP 0.59	MQ 0.51	0.42	0.34	0.25				
	N		1.61	NB 1.52	NC 1.44	ND 1.35	NE 1.27	NF 1.18	NG 1.10	NH 1.01	NJ 0.93	NK 0.85	NL 0.76	NM 0.68	NN 0.59	NP 0.51	0.42	0.34	0.25					
	P		PA 1.52	PB 1.44	PC 1.35	PD 1.27	PE 1.18	PF 1.10	PG 1.01	PH 0.93	PJ 0.85	PK 0.76	PL 0.68	PM 0.59	PN 0.51	0.42	0.34	0.25						
	Q		QA 1.44	QB 1.35	QC 1.27	QD 1.18	QE 1.10	QF 1.01	QG 0.93	QH 0.85	QJ 0.76	QK 0.68	QL 0.59	QM 0.51	0.42	0.34	0.25							
	R		RA 1.35	RB 1.27	RC 1.18	RD 1.10	RE 1.01	RF 0.93	RG 0.85	RH 0.76	RJ 0.68	RK 0.59	RL 0.51	0.42	0.34	0.25								
	S		SA 1.27	SB 1.18	SC 1.10	SD 1.01	SE 0.93	SF 0.85	SG 0.76	SH 0.68	SJ 0.59	SK 0.51	0.42	0.34	0.25									
	T		TA 1.18	TB 1.10	TC 1.01	TD 0.93	TE 0.85	TF 0.76	TG 0.68	TH 0.59	TJ 0.51	0.42	0.34	0.25										
	U		UA 1.10	UB 1.01	UC 0.93	UD 0.85	UE 0.76	UF 0.68	UG 0.59	UH 0.51	0.42	0.34	0.25											
	V		VA 1.01	VB 0.93	VC 0.85	VD 0.76	VE 0.68	VF 0.59	VG 0.51	0.42	0.34	0.25												
	W		WA 0.93	WB 0.85	WC 0.76	WD 0.68	WE 0.59	WF 0.51	0.42	0.34	0.25													

Supply Voltage	Available Colors
1.8V±5%	Not Supported
1.71V to 3.63V	Not Supported
2.5V±10%	Blue
3.3V±10%	Blue / Red
2.25V to 3.63V	Blue
Note 10	Gray

Note:

10. Please contact SiTime.

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing (i.e. VHn – VLn).

For example, order code “FS” selects VHn code “F” (i.e. Vdd-1.144 V) and VLn code “S” (i.e. Vdd-1.530 V) corresponding to a V_Swing of 0.845 V peak-peak, which may be used for supply voltages of 2.5 V ±10%, 3.3 V ±10% or (2.25 V to 3.63 V). Alternatively, an order code of “GS” corresponds to a VHn code “G” (i.e. Vdd-1.193 V) and a VLn order code “S” (e.g. Vdd-1.530 V) corresponding to a V_Swing of 0.760 V peak-peak, which may be used for a supply voltage of 3.3 V ±10%.

Table 17. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on GND pin

Order Code V_Swing (V)			C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y
			0.45V	0.49V	0.54V	0.59V	0.64V	0.69V	0.74V	0.79V	0.84V	0.89V	0.94V	0.99V	1.03V	1.08V	1.16V	1.23V	1.3V	1.38V	1.45V	1.53V	1.6V
VHn	A	VLn + V_Swing / 2																		AV 1.94	AW 1.86	AX 1.69	AY 1.61
	B																			BV 1.86	BW 1.77	BX 1.61	BY 1.52
	C																		CU 1.94	CV 1.77	CW 1.69	CX 1.52	CY 1.44
	D																	DT 1.94	DU 1.86	DV 1.69	DW 1.61	DX 1.44	DY 1.35
	E																	ET 1.86	EU 1.77	EV 1.61	EW 1.52	EX 1.35	EY 1.27
	F																FS 1.94	FT 1.77	FU 1.69	FV 1.52	FW 1.44	FX 1.27	FY 1.18
	G															1.94	GS 1.86	GT 1.69	GU 1.61	GV 1.44	GW 1.35	GX 1.18	GY 1.10
	H														1.94	1.86	HS 1.77	HT 1.61	HU 1.52	HV 1.35	HW 1.27	HX 1.10	HY 1.01
	J													1.94	1.86	1.77	JS 1.69	JT 1.52	JU 1.44	JV 1.27	JW 1.18	JX 1.01	JY 0.93
	K												1.94	1.86	1.77	1.69	KS 1.61	KT 1.44	KU 1.35	KV 1.18	KW 1.10	KX 0.93	KY 0.85
	L											1.94	1.86	1.77	1.69	1.61	LS 1.52	LT 1.35	LU 1.27	LV 1.10	LW 1.01	LX 0.85	LY 0.76
	M										1.94	1.86	1.77	1.69	1.61	MR 1.52	MS 1.44	MT 1.27	MU 1.18	MV 1.01	MW 0.93	MX 0.76	MY 0.68
	N									1.94	1.86	1.77	1.69	1.61	NQ 1.52	NR 1.44	NS 1.35	NT 1.18	NU 1.10	NV 0.93	NW 0.85	NX 0.68	NY 0.59
	P								1.94	1.86	1.77	1.69	1.61	PP 1.52	PQ 1.44	PR 1.35	PS 1.27	PT 1.10	PU 1.01	PV 0.85	PW 0.76	PX 0.59	PY 0.51
	Q							1.94	1.86	1.77	1.69	1.61	QN 1.52	QP 1.44	QQ 1.35	QR 1.27	QS 1.18	QT 1.01	QU 0.93	QV 0.76	QW 0.68	QX 0.51	0.42
	R						1.94	1.86	1.77	1.69	1.61	RM 1.52	RN 1.44	RP 1.35	RQ 1.27	RR 1.18	RS 1.10	RT 0.93	RU 0.85	RV 0.68	RW 0.59	0.42	0.34
	S					1.94	1.86	1.77	1.69	1.61	SL 1.52	SM 1.44	SN 1.35	SP 1.27	SQ 1.18	SR 1.10	SS 1.01	ST 0.85	SU 0.76	SV 0.59	SW 0.51	0.34	0.25
	T				1.94	1.86	1.77	1.69	1.61	TK 1.52	TL 1.44	TM 1.35	TN 1.27	TP 1.18	TQ 1.10	TR 1.01	TS 0.93	TT 0.76	TU 0.68	TV 0.51	0.42	0.25	
	U			1.94	1.86	1.77	1.69	1.61	UJ 1.52	UK 1.44	UL 1.35	UM 1.27	UN 1.18	UP 1.10	UQ 1.01	UR 0.93	US 0.85	UT 0.68	UU 0.59	0.42	0.34		
	V		1.94	1.86	1.77	1.69	1.61	VH 1.52	VJ 1.44	VK 1.35	VL 1.27	VM 1.18	VN 1.10	VP 1.01	VQ 0.93	VR 0.85	VS 0.76	VT 0.59	VU 0.51	0.34	0.25		
	W		1.86	1.77	1.69	1.61	WG 1.52	WH 1.44	WJ 1.35	WK 1.27	WL 1.18	WM 1.10	WN 1.01	WP 0.93	WQ 0.85	WR 0.76	WS 0.68	WT 0.51	0.42	0.25			
	X		1.77	1.69	1.61	XF 1.52	XG 1.44	XH 1.35	XJ 1.27	XK 1.18	XL 1.10	XM 1.01	XN 0.93	XP 0.85	XQ 0.76	XR 0.68	XS 0.59	0.42	0.34				
	Y		1.69	1.61	YE 1.52	YF 1.44	YG 1.35	YH 1.27	YJ 1.18	YK 1.10	YL 1.01	YM 0.93	YN 0.85	YP 0.76	YQ 0.68	YR 0.59	YS 0.51	0.34	0.25				
	Z		1.61	ZD 1.52	ZE 1.44	ZF 1.35	ZG 1.27	ZH 1.18	ZJ 1.10	ZK 1.01	ZL 0.93	ZM 0.85	ZN 0.76	ZP 0.68	ZQ 0.59	ZR 0.51	0.42	0.25					
	1		1C 1.52	1D 1.44	1E 1.35	1F 1.27	1G 1.18	1H 1.10	1J 1.01	1K 0.93	1L 0.85	1M 0.76	1N 0.68	1P 0.59	1Q 0.51	0.42	0.34						
	2		2C 1.44	2D 1.35	2E 1.27	2F 1.18	2G 1.10	2H 1.01	2J 0.93	2K 0.85	2L 0.76	2M 0.68	2N 0.59	2P 0.51	0.42	0.34	0.25						
	3		3C 1.35	3D 1.27	3E 1.18	3F 1.10	3G 1.01	3H 0.93	3J 0.85	3K 0.76	3L 0.68	3M 0.59	3N 0.51	0.42	0.34	0.25							

Supply Voltage	Available Colors
1.8V±5%	Orange, Green
1.71V to 3.63V	Green
2.5V±10%	Orange, Green, Blue, Purple
3.3V±10%	Green, Blue, Red
2.25V to 3.63V	Green, Blue
Note 11	Gray

Note:

11. Please contact SiTime.

Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

Test Setups for LVPECL Measurements

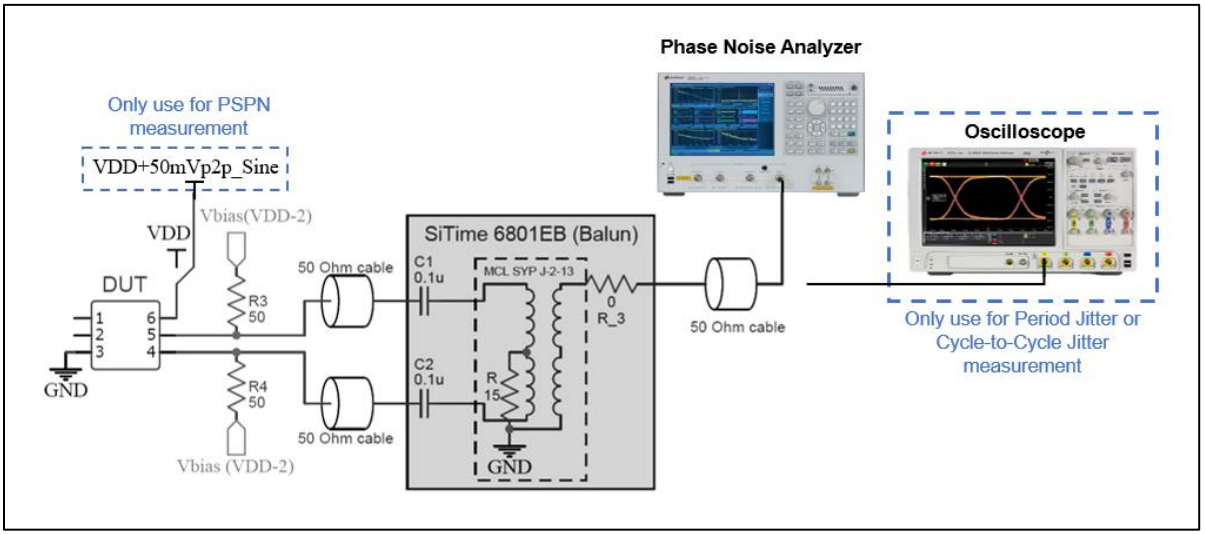


Figure 5. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) without filter added[12]

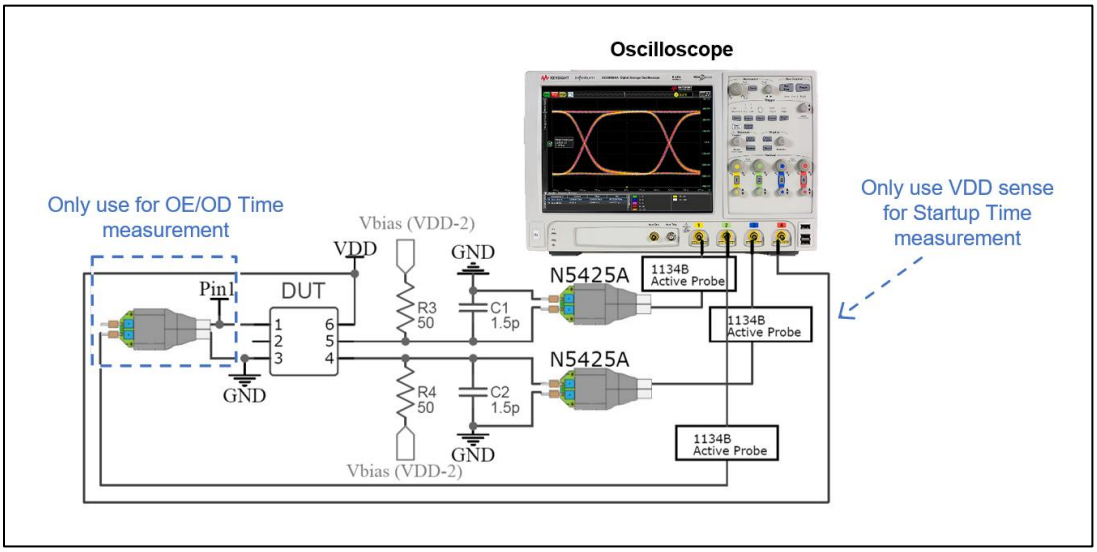


Figure 6. Test setup to measure LVPECL Waveform Characteristics, Current Consumption (with Termination 2)[13], Output Enable/Disable Time, and Startup Time

Notes:

12. See Figure 7 for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
13. See Figure 8 for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for FlexSwing Measurements[14]

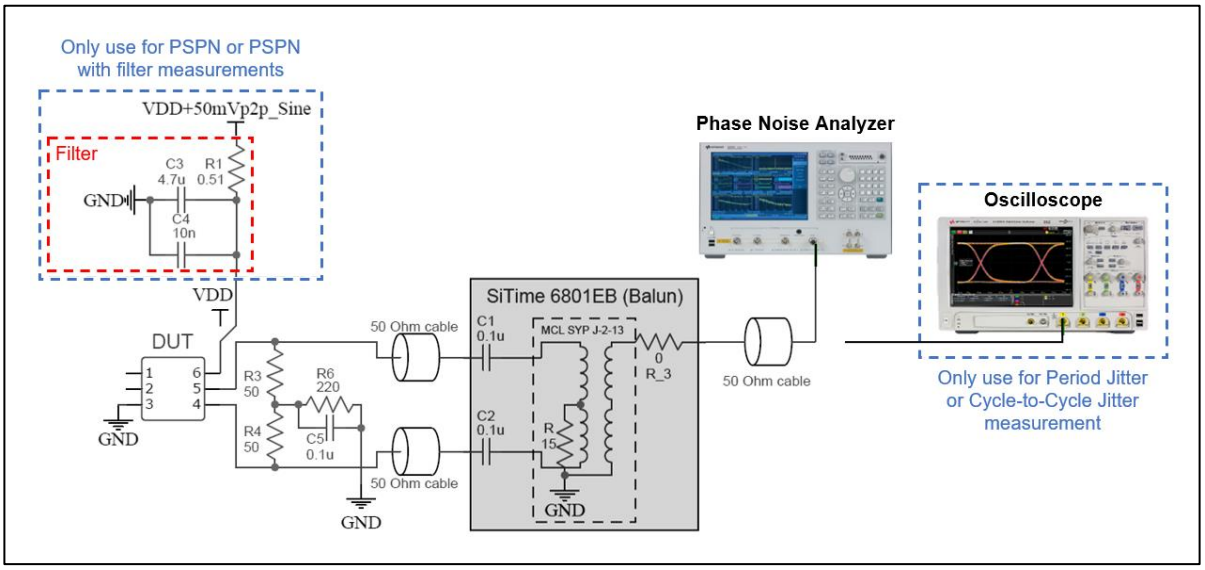


Figure 7. Test setup to measure FlexSwing Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added[15]

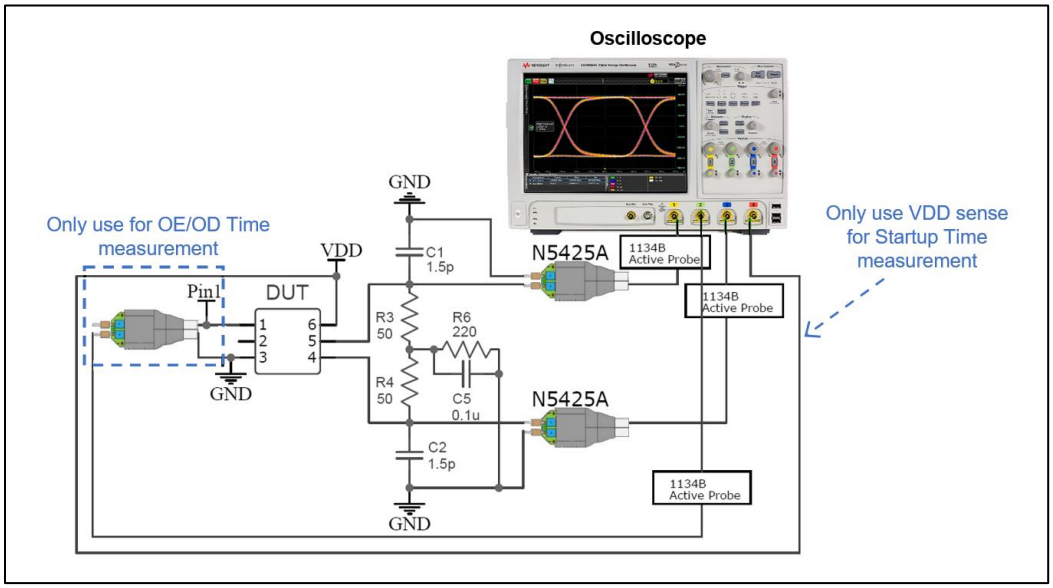


Figure 8. Test setup to measure FlexSwing Waveform Characteristics, Current Consumption[16], Output Enable/Disable Time, and Startup Time

Note:

14. The same test circuits are used for FlexSwing referenced to VDD and FlexSwing referenced to GND.
15. Test setup is also used to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
16. Test setup is also used to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for LVDS Measurements

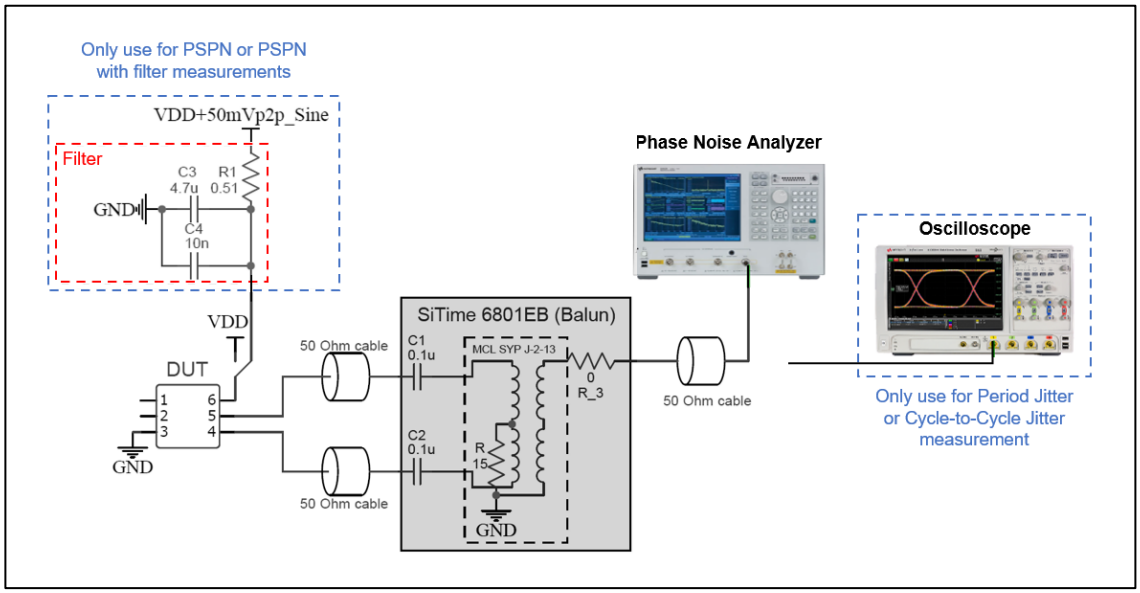


Figure 9. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

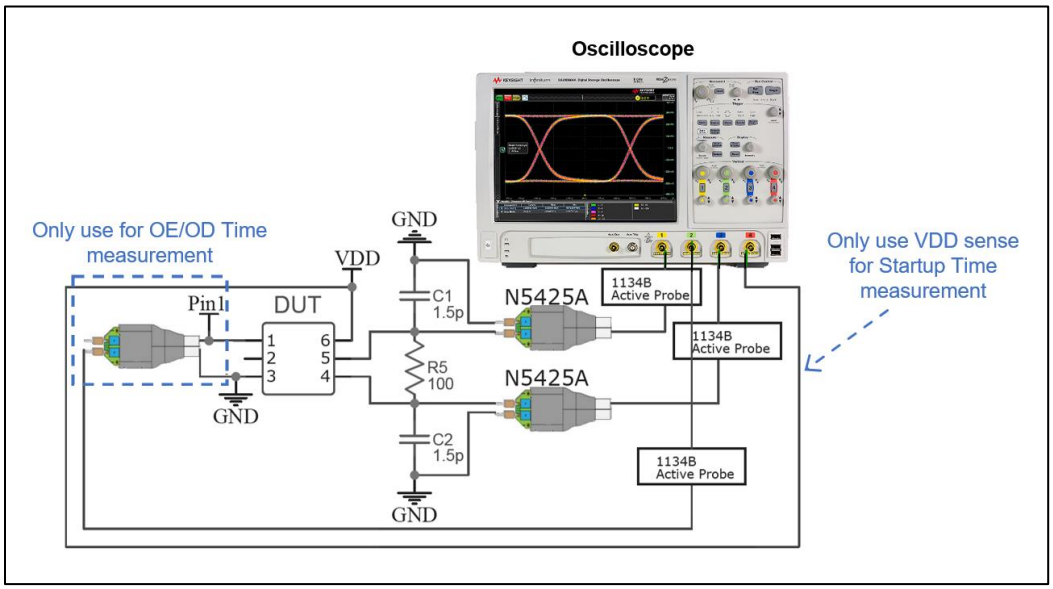


Figure 10. Test setup to measure LVDS Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for HCSL Measurements

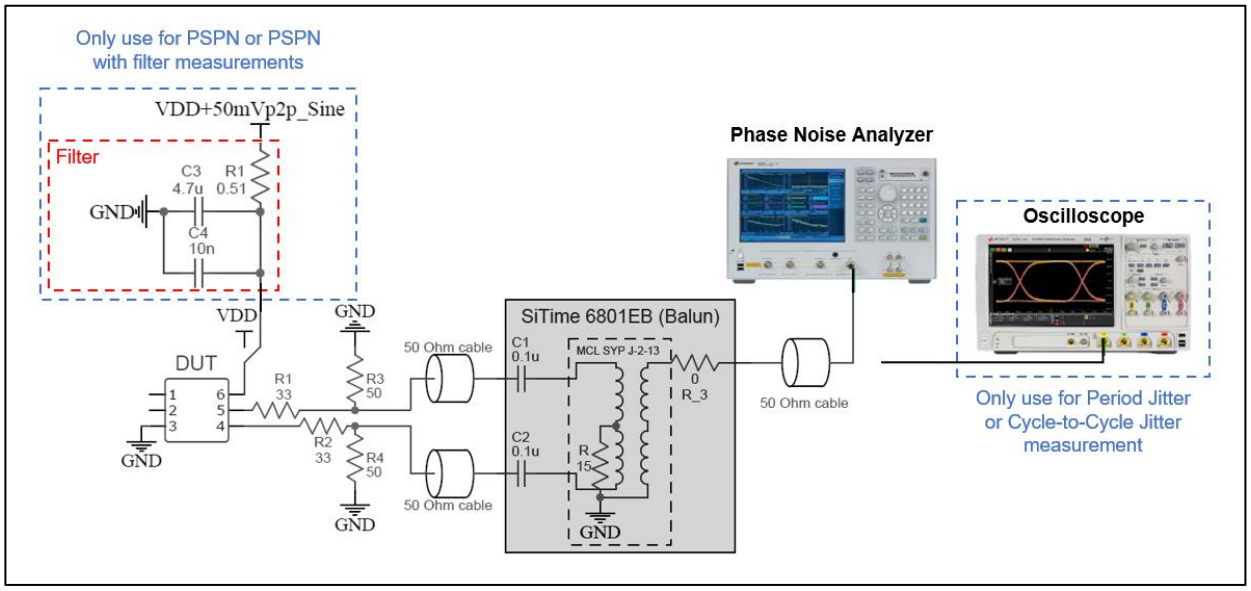


Figure 11. Test setup to measure HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

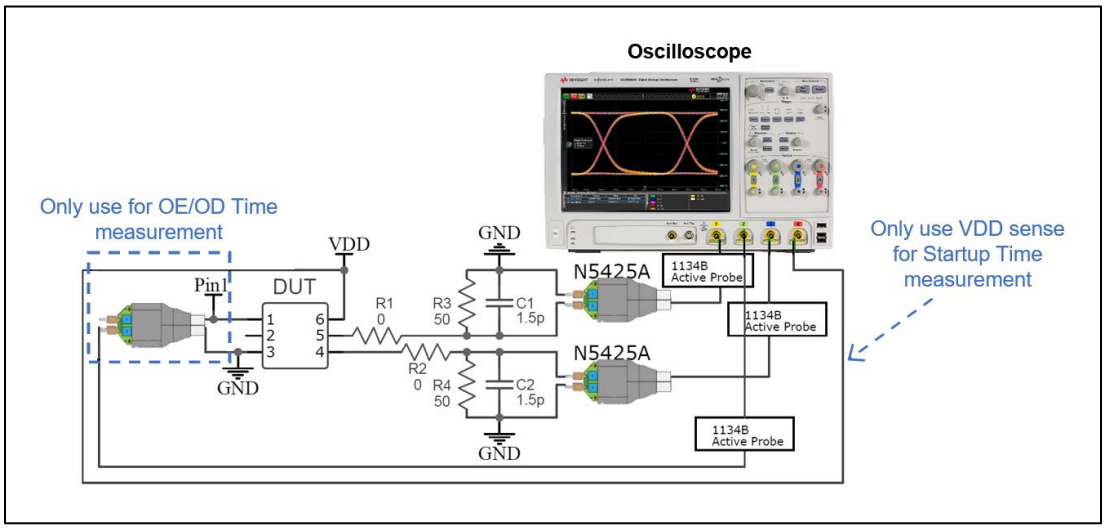


Figure 12. Test setup to measure HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for Low-Power HCSL Measurements

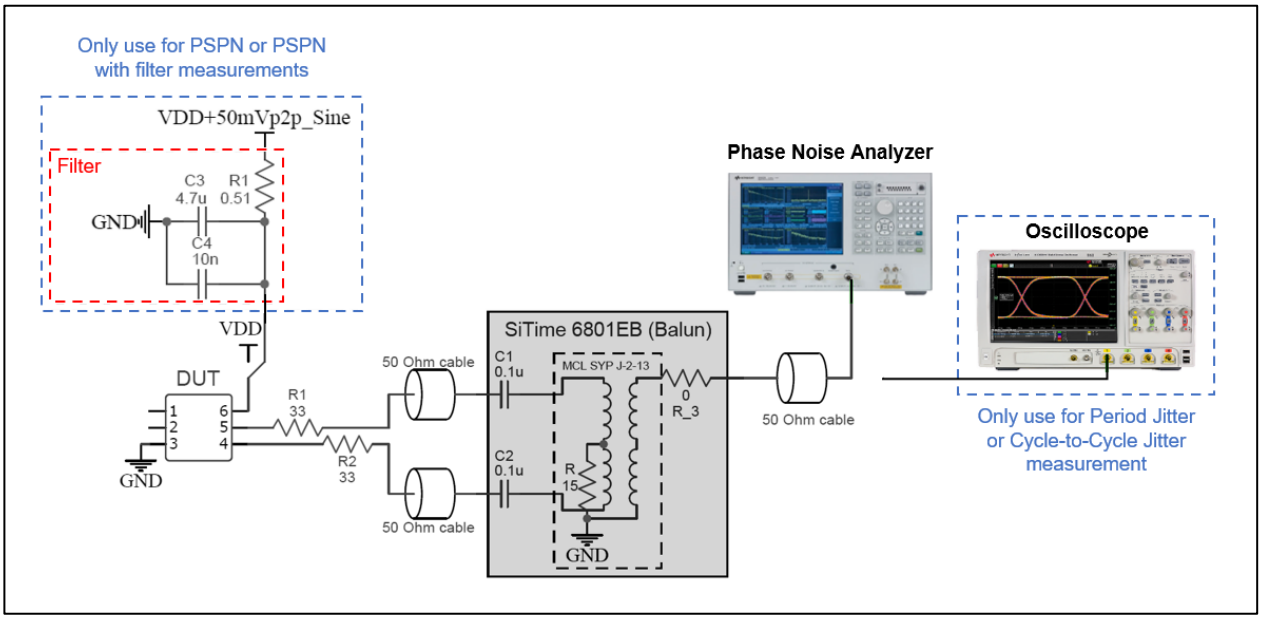


Figure 13. Test setup to measure Low-Power HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

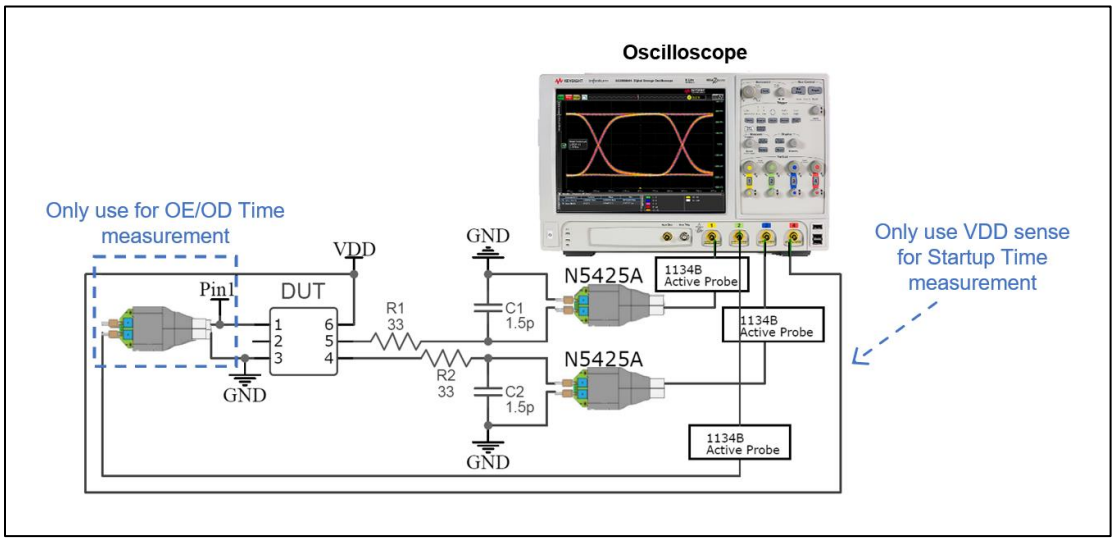


Figure 14. Test setup to measure Low-Power HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Waveform Diagrams

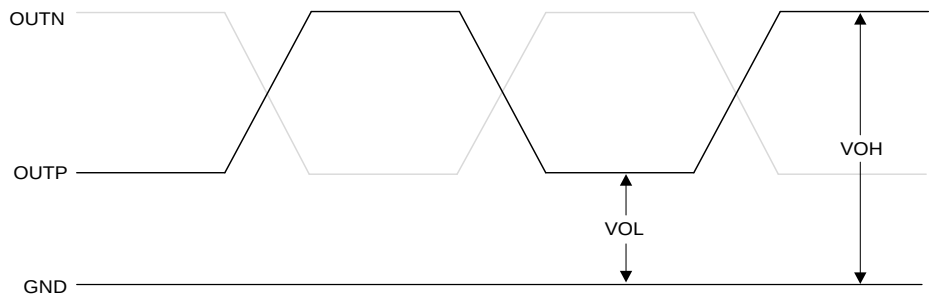


Figure 15. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

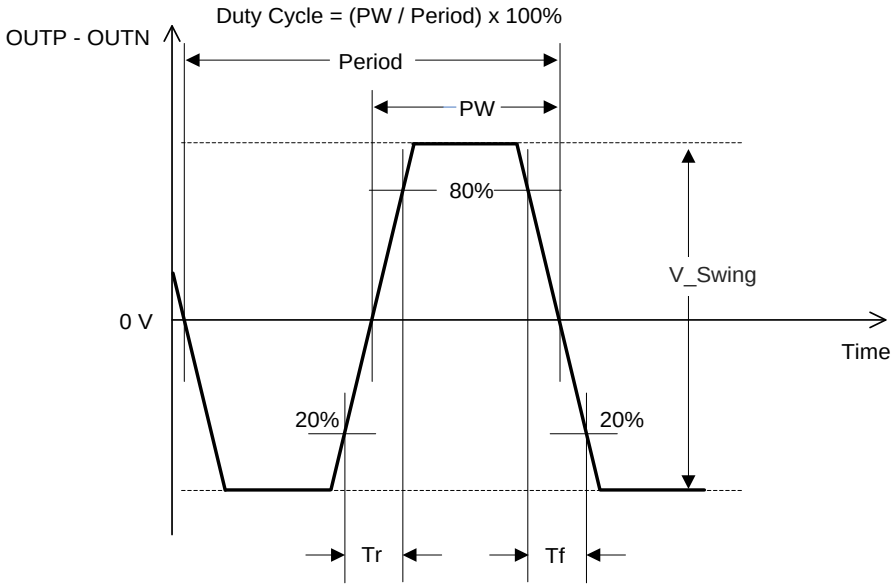


Figure 16. LVPECL, LVDS, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

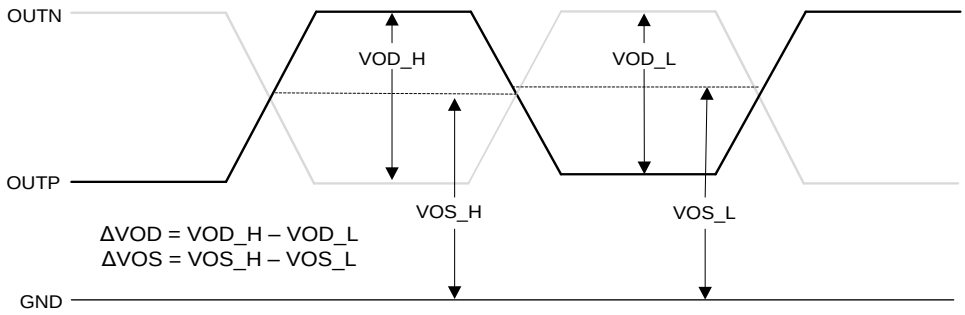


Figure 17. LVDS Voltage Levels per Differential Pin

Waveform Diagrams (continued)

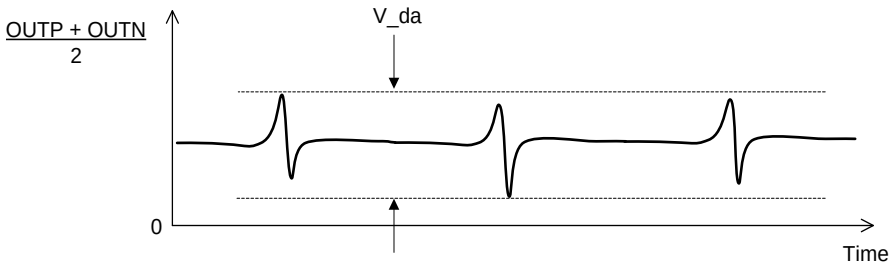


Figure 18. Differential Asymmetry (V_da)

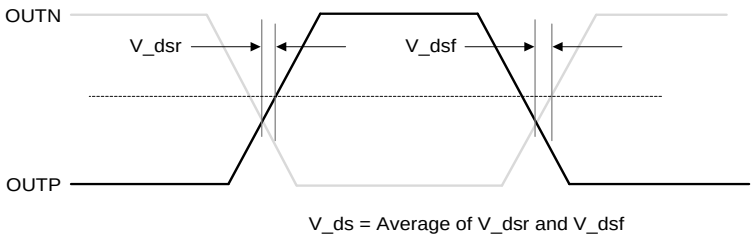


Figure 19. Differential Skew (V_ds) is measured as the Time between the Average Voltage Level and Crossing Voltage

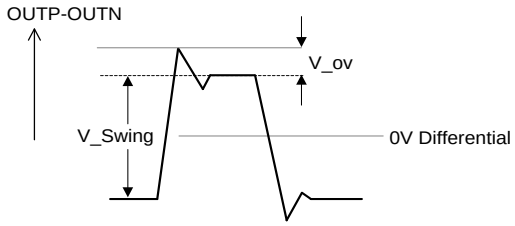


Figure 20. Overshoot Voltage (V_ov) for LVPECL, FlexSwing, HCSL, Low-power HCSL

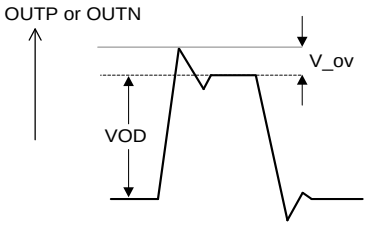


Figure 21. Overshoot Voltage (V_ov) for LVDS Output

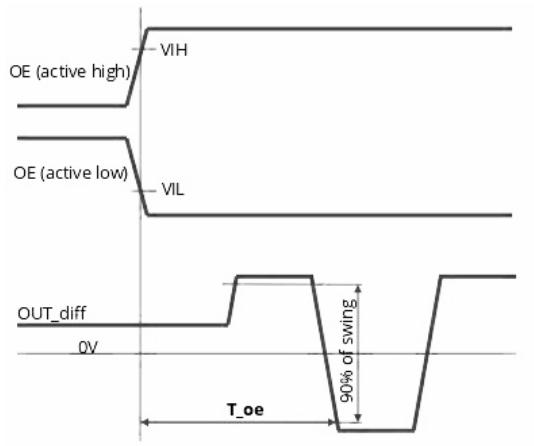


Figure 22. OE Pin Enable Timing (T_oe)

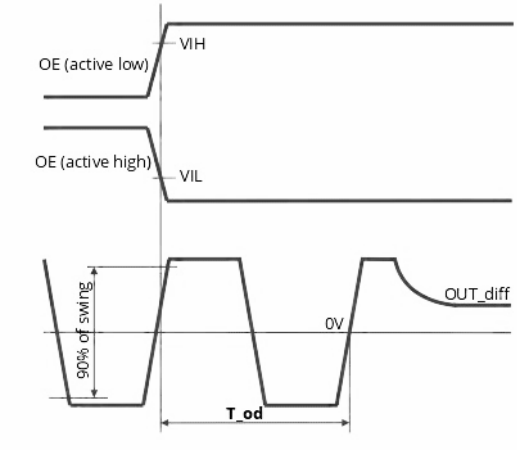


Figure 23. OE Pin Disable Timing (T_od)

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9501 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 25 and Figure 27, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_load) into the load termination.

Table 18. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 24	Figure 25	Figure 26	Figure 27	Figure 28	Figure 29
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use I_load = 40 mA with 100 Ω near-end bias resistor	**Do Not Use**	OK to use I_load = 28 mA	OK to use	OK to use I_load = 28 mA	**Do Not Use**
FlexSwing referenced to Vdd		OK to use[17]	OK to use (see Figure 25 for frequency ranges and voltage swings)	OK to use[18]	OK to use	OK to use	**Do Not Use**
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"			**Do Not Use**	OK to use	**Do Not Use**	**Do Not Use**
	"18"			**Do Not Use**	OK to use	**Do Not Use**	OK to use

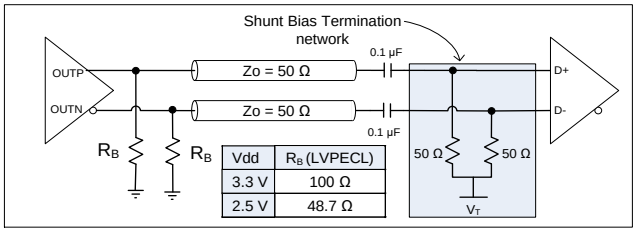


Figure 24. Recommended LVPECL and FlexSwing[17] Termination when AC-coupled

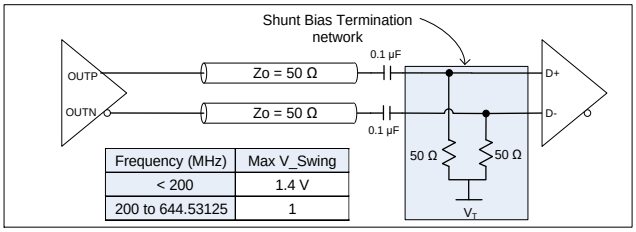


Figure 25. Recommended FlexSwing Termination when AC-coupled

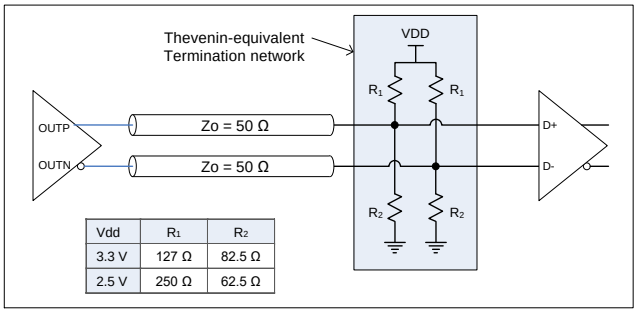


Figure 26. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network[18]

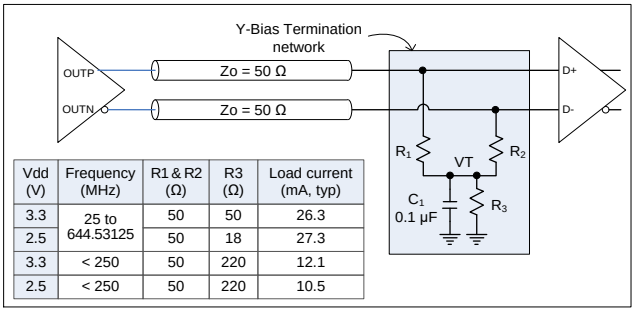


Figure 27. LVPECL and FlexSwing with Y-Bias Termination

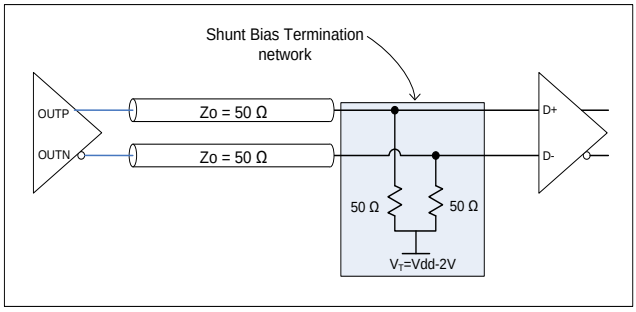


Figure 28. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

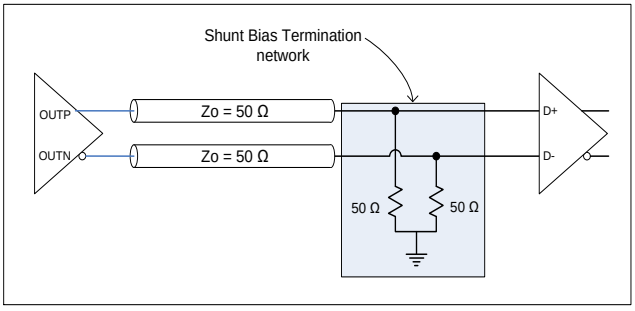


Figure 29. FlexSwing Termination – Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

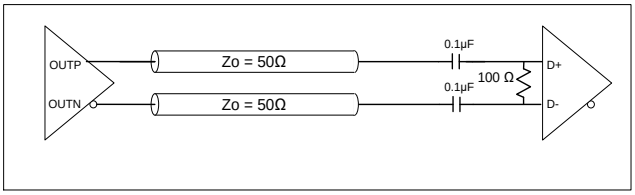


Figure 30. LVDS AC Termination

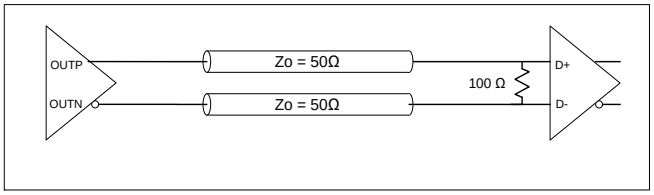


Figure 31. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

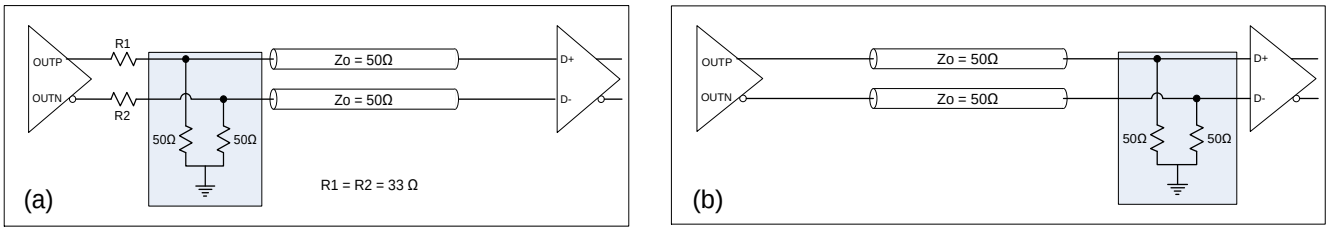


Figure 32. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

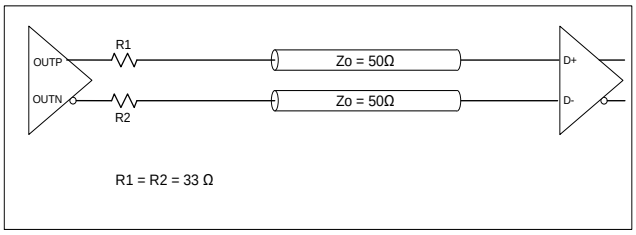


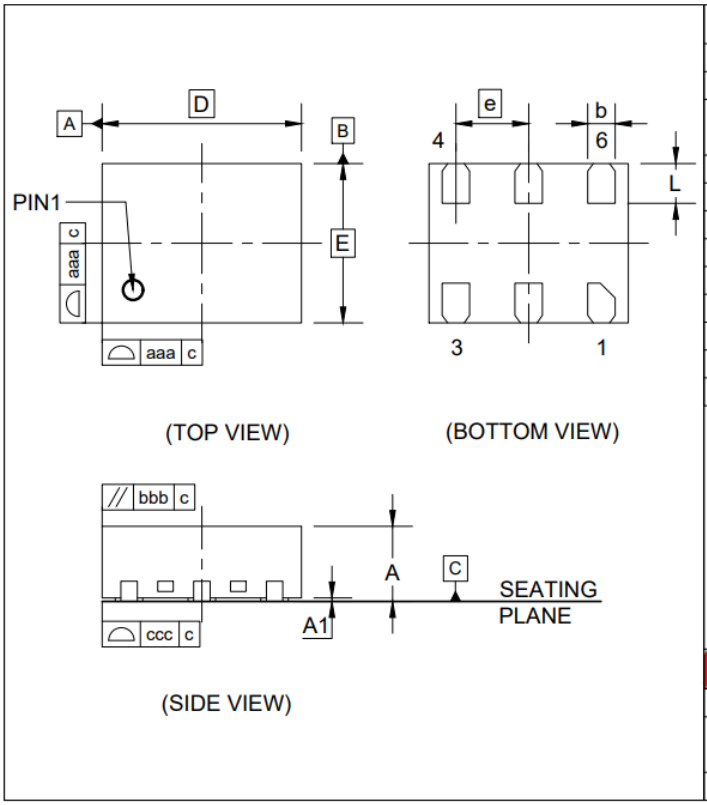
Figure 33. Low-power HCSL Termination

Notes:

17. Contact SiTime for optimum R_B values for FlexSwing options.
18. Contact SiTime for optimum R1 and R2 values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

Package Size – Dimensions (Unit: mm)[19]



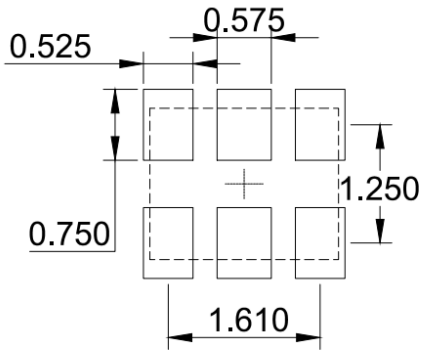
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		2.000 BSC	
	Y	E		1.600 BSC	
LEAD WIDTH		b	0.225	0.275	0.325
LEAD LENGTH		L	0.300	0.400	0.500
LEAD PITCH		e		0.730 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTE

1. ALL DIMENSION IN MM

SiTime		
PKG INFO		DRAWING NO.
6L PQFN 2.000x1.600x0.750 mm		POD-077-PQFN-006-C02016
		REV / SHEET
DATE	12/6/2021	B02 / 01

Recommended Land Pattern (Unit: mm)[20]



Note : All units in mm.

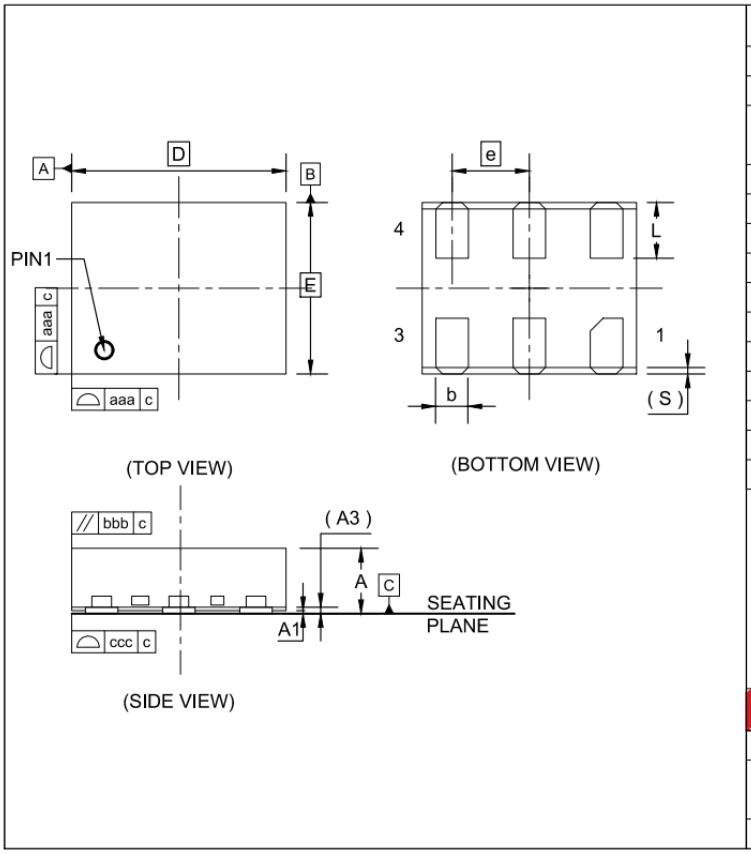
SiTime	PKG INFO	SPL DRAWING NO.	
	6L QFN 2.000x1.600 mm	SPL-077-QFN-006-C02016	
DATE		REV	SHEET
2020/04/20		B00	01

Notes:

19. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
20. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

Dimensions and Patterns — 2.5 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)[19]



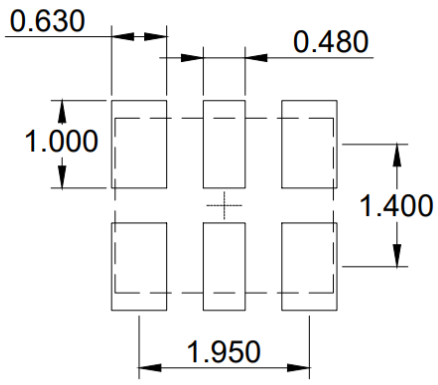
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.350	0.050
BODY SIZE	X	D	2.500 BSC		
	Y	E	2.000 BSC		
LEAD WIDTH		b	0.330	0.380	0.430
LEAD LENGTH		L	0.550	0.650	0.750
LEAD PITCH		e	0.900 BSC		
PACKAGE TOLERNCE		aaa	0.100		
MOLD FLATNESS		bbb	0.100		
COPLANARITY		ccc	0.080		
HALF CUT WIDTH		S	0.075 REF		
HALF CUT DPETH		A3	0.075 REF		

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
6L PQFW 2.500x2.000x0.850 mm		POD-078-PQFW-006-C02520	
		REV	SHEET
DATE	2020/9/23	B00	01

Recommended Land Pattern (Unit: mm)[20]

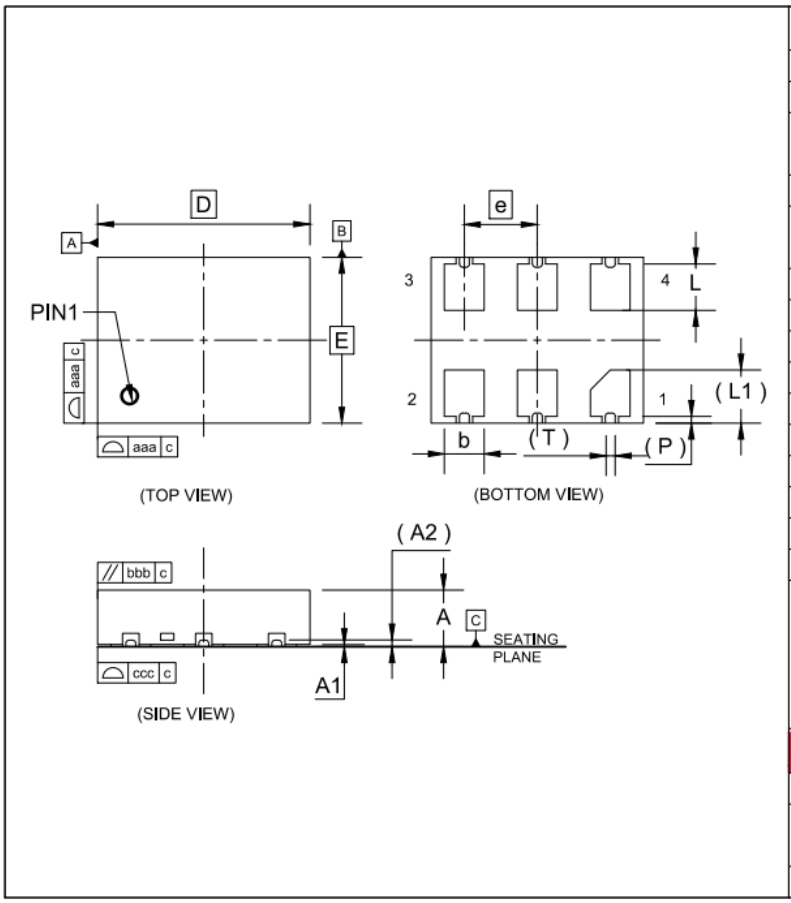


Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	6L PQFW 2.500x2.000 mm	SPL-078-QFN-006-C02520	
DATE		REV	SHEET
2021/12/06		B00	01

Dimensions and Patterns — 3.2 x 2.5 mm x mm

Package Size – Dimensions (Unit: mm)[19]



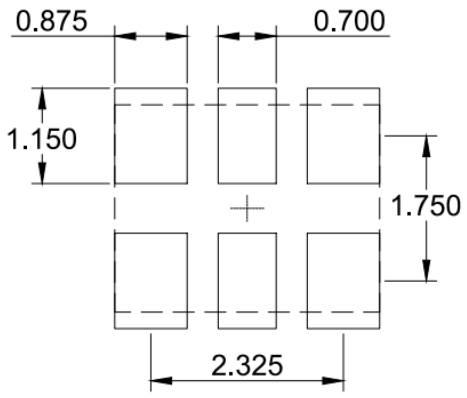
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		3.200 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.550	0.600	0.650
LEAD LENGTH		L	0.650	0.700	0.750
		L1		0.800 REF	
LEAD PITCH		e		1.100 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	
DIMPLE WIDTH		T		0.150 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
6L PQFD 3.200x2.500x0.850 mm		POD-076-PQFD-006-C03225	
		REV	SHEET
DATE	2020/9/23	B00	01

Recommended Land Pattern (Unit: mm)[20]



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	6L QFN 3.200x2.500 mm	SPL-076-QFN-006-C03225	
DATE		REV	SHEET
2020/04/20		B00	01

Additional Information

Table 19. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	TBD

Revision History

Table 20. Revision History

Revision	Release Date	Change Summary
0.5	27-Apr-2020	Advanced datasheet
0.51	18-May-2020	Formatting changes Fixed typos Added 2016 and 2520 packages
0.52	1-Jun-2020	Formatting changes Updated package drawings
0.53	2-Aug-2020	Modified Termination Diagrams section
0.54	23-Sep-2020	Modified LVPECL, FlexSwing, LVDS current consumption specifications Modified phase jitter specification Added FlexSwing order codes Added 250u T&R order code Changed rev table date format
0.55	23-Oct-2020	Trademarks update Modified termination for HCSL and low-power HCSL rise/fall time specs
0.56	15-Dec-2020	Updated current consumption
0.57	5-Jan-2021	Updated FlexSwing Electrical Characteristics tables and description Formatting updates
0.58	20-Jan-2022	General Updates
0.59	21-Mar-2022	General Updates
0.9	29-Jul-2022	Added Test Diagrams section Updated Electrical Characteristics tables and descriptions
0.91	1-Aug-2022	Preliminary datasheet
0.92	12-Aug-2022	Updated Test Diagrams General wording and formatting updates

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