MPQ4323M

42V Load Dump Tolerant, 3A, Ultra-Compact, Low-I_Q, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4323M is a configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching regulator with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). The device provides 3A of highly efficient output current (I_{OUT}) with peak current mode control.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown mode quiescent current (I_Q) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open-drain power good (PG) signal indicates that the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4323M is available in a QFN-12L (3.5mmx3.5mm) package.

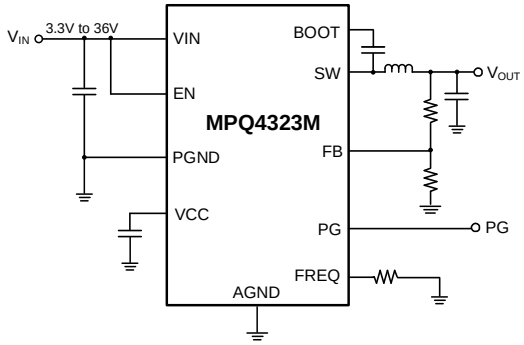
FEATURES

- Designed for Automotive Applications:
  - Survives 42V Load Dump
  - Supports 3.1V Cold Crank
  - 3A Continuous Output Current (I_{OUT})
  - Continuous Operation Up to 36V
  - Junction Temperature Operation from -40°C to +150°C (Absolute Maximum)
- Increases Battery Life:
  - 1µA Shutdown Supply Current
  - 20µA Sleep Mode Quiescent Current
  - Advanced Asynchronous Mode (AAM) Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Integrated 70mΩ High-Side MOSFET (HS-FET) and 50mΩ Low-Side MOSFET (LS-FET)
  - 65ns Minimum On Time and 50ns Minimum Off Time
- Optimized for EMC and EMI:
  - Frequency Spread Spectrum (FSS) Modulation
  - Symmetric VIN Pinout
  - Integrated Input Capacitors
  - CISPR25 Class 5 Compliant
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good (PG) Output
  - Low-Dropout (LDO) Mode
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-12L (3.5mmx3.5mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

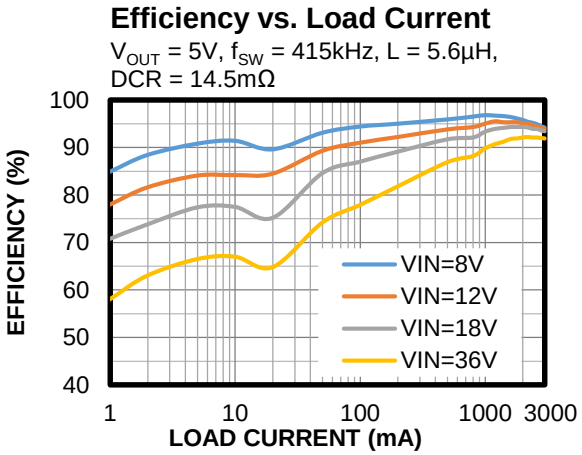
APPLICATIONS

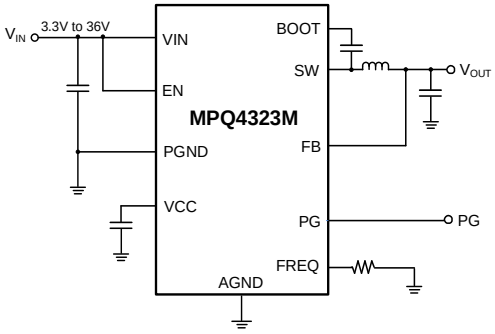
- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

TYPICAL APPLICATION



Typical Application (Adjustable Output)





Typical Application (Fixed Output)

ORDERING INFORMATION

Part Number [1] *	Package	Top Marking	MSL Rating**
MPQ4323MGQCE-AEC1***	QFN-12L (3.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4323MGQCE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Note:

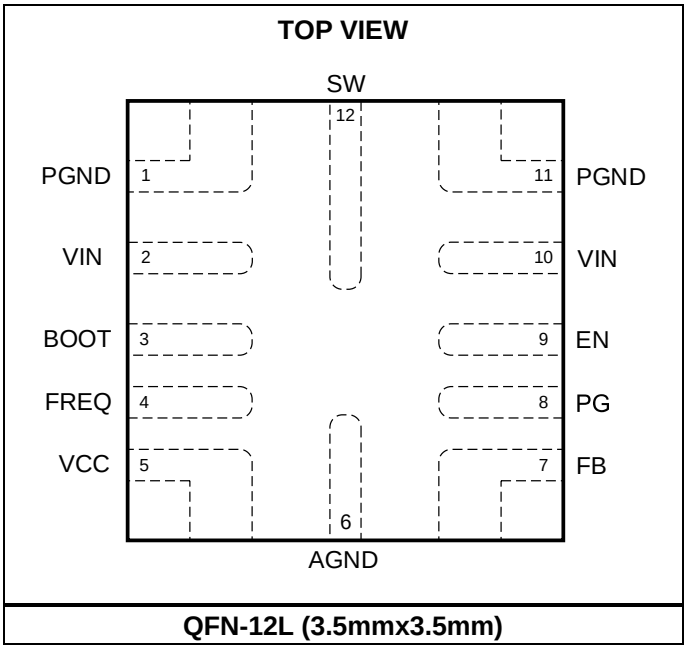
1) Contact MPS for more details regarding the fixed-output versions.

TOP MARKING

BQRYW
LLLLL
E

BQR: Production code of MPQ4323MGQCE-AEC1
Y: Year code
W: Week code
LLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-12L (3.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 11	PGND	**Power ground.**
2, 10	VIN	**Input supply.** The VIN pin supplies power to all of the internal control circuitry and the power MOSFET connected to SW. The two VIN pins are connected internally. Connect a decoupling capacitor from VIN to ground, close to each VIN pin, to minimize switching spikes. For the MPQ4323M, two 0.1µF capacitors are integrated between VIN and PGND inside the chip.
3	BOOT	**Bootstrap.** The BOOT pin is the high-side MOSFET (HS-FET) driver's positive power supply connected to SW. Connect a bypass capacitor between BOOT and SW.
4	FREQ	**Switching frequency configuration.** Connect a resistor from the FREQ pin to ground to set the switching frequency (f_{SW}).
5	VCC	**Bias supply.** The VCC pin is the internal regulator's output, and supplies power to the internal control circuit and gate drivers. Connect a minimum 1µF decoupling capacitor from VCC to ground, and place it as close as possible to VCC.
6	AGND	**Analog ground.**
7	FB	**Feedback input.** The FB pin is the error amplifier's (EA's) negative input, and its typical value is 0.8V. For a fixed output, connect FB directly to the output voltage (V_{OUT}). For an adjustable output, connect this pin to the external feedback divider's middle point between the output and AGND to set V_{OUT}.
8	PG	**Power good output.** The PG pin's output is an open drain. If PG is used, it must be connected to a power source via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high; if V_{OUT} is above 107% or below 93% of the nominal voltage, PG goes low. Float this pin if it is not used.
9	EN	**Enable.** Pull the EN pin below the specified threshold (about 0.85V) to shut down the chip. Pull EN above the specified threshold (about 1.02V) to enable the chip. The EN pin does not require an internal pull-up or pull-down resistor. Do not float the EN pin.
12	SW	**Switch node.** The SW pin is the HS-FET source and the low-side MOSFET (LS-FET) drain.

ABSOLUTE MAXIMUM RATINGS (2)

VIN, EN……..42V for automotive load dump (3)
VIN, EN……..-0.3V to +40V
SW…… -0.3V to $V_{IN(MAX)}$ + 0.3V
BOOT……..... V_{SW} + 5.5V
FREQ, VCC……..….5.5V
All other pins……. .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (4)
QFN-12L (3.5mmx3.5mm)…….... 3.8W (8)
Operating junction temperature .....150°C
Lead temperature…….....260°C
Storage temperature……...-65°C to +150°C

ESD Ratings

Human body model (HBM)……..…….Class 2 (5)
Charged device model (CDM).....Class C2b (6)

Recommended Operating Conditions

Supply voltage (V_{IN})…….3.3V to 36V
Minimum V_{IN} for start-up.……3.8V
Minimum V_{IN} after start-up.……..…….....3.1V
Output voltage (V_{OUT})…….....0.8V to 0.95 x V_{IN}
Operating junction temp (T_J)….-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-12L (3.5mmx3.5mm)
JESD51-7 (7)…...…..……47.9…....6…….°C/W
EVQ4323M-G-00A (8)……..32.5.....2.6.....°C/W

Notes:

2) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
3) Refer to ISO16750.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
8) Measured on a standard EVB: 4-layer, 2 oz, copper PCB (8.3cmx8.3cm).

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.4	3.65	3.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.6	2.9	3.1	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			750		mV
V_{IN} quiescent current	I_Q	V_{FB} = 0.85V, no load, T_J = 25°C		20	28	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +125°C (9)			34	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +150°C			80	µA
V_{IN} switching quiescent current (9)	$I_{Q\_SWITCHING}$	Switching, R_{FB1} = 1MΩ, R_{FB2} = 191kΩ, no load		25		µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN\_OVP\_RISING}$		35.5	37.5	40	V
V_{IN} OVP falling threshold	$V_{IN\_OVP\_FALLING}$		34.5	36.5	39	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
Switches and Frequency						
Switching frequency without frequency spread spectrum (FSS)	f_{SW}	R_{FREQ} = 86.6kΩ	332	415	498	kHz
		R_{FREQ} = 34.8kΩ	900	1000	1100	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
FSS span				±10		%
FSS modulation frequency				15		kHz
Minimum on time (9)	t_{ON_MIN}			65	80	ns
Minimum off time (9)	t_{OFF_MIN}			50	70	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = 25°C)		0.01	1	µA
		V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = -40°C to +150°C)		0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BOOT} - V_{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		50	90	mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB voltage (adjustable-output version)	V_{FB}	T_J = 25°C	0.794	0.8	0.806	V
		T_J = -40°C to +150°C	0.790	0.8	0.810	V
FB input current	I_{FB}	Adjustable output version		0	100	nA
Output voltage (V_{OUT}) discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V	2	4		mA
BOOT						
BOOT - SW refresh rising threshold	V_{BOOT_RISING}			2.5	2.9	V
BOOT - SW refresh falling threshold	$V_{BOOT\_FALLING}$			2.3	2.7	V
BOOT - SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
EN						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	EN high to SS finishes	3	5	7	ms
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5	5.3	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	70		mA
PG						
PG rising threshold (V_{FB} / V_{REF})	PG_{VTH_RISING}	V_{OUT} rising	93%	94.5%	96%	V_{REF}
		V_{OUT} falling	104%	105.5%	107%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{VTH\_FALLING}$	V_{OUT} falling	91.5%	93%	94.5%	
		V_{OUT} rising	105.5%	107%	108.5%	
PG threshold hysteresis (V_{FB} / V_{REF})	PG_{VTH_HYS}			1.5%		
PG low V_{OUT}	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_R}			70		µs
PG falling deglitch time	t_{PG_F}			60		µs
Protections						
High-side (HS) peak current limit	I_{LIMIT_HS}	Duty cycle = 30%	4.3	5.8	7.3	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		3	4.4	5.7	A
Zero-current detection (ZCD) current	I_{ZCD}		-0.05	0.05	+0.15	A
Thermal shutdown (9)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C

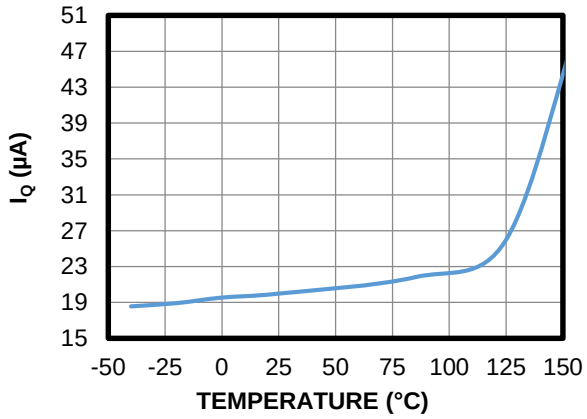
Note:

9) Not tested in production. Guaranteed by design and characterization.

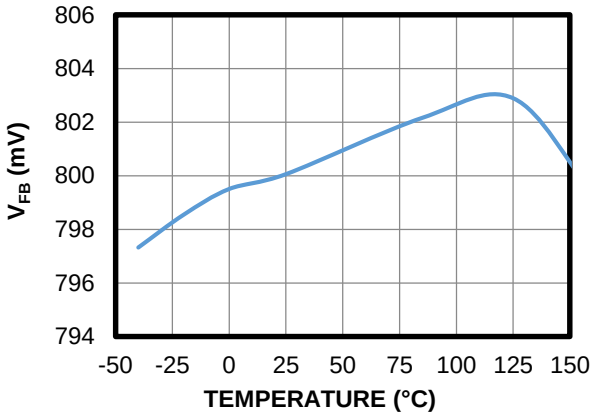
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

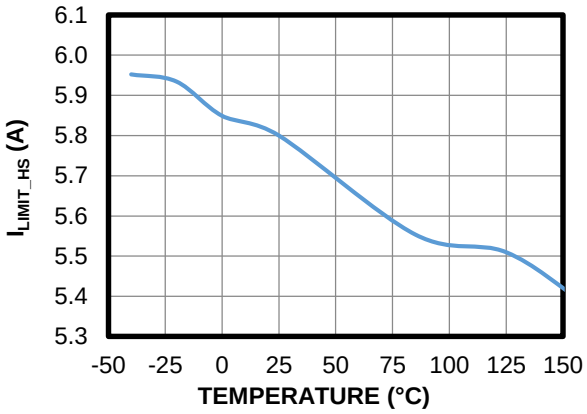
V_{IN} Quiescent Current vs. Temperature



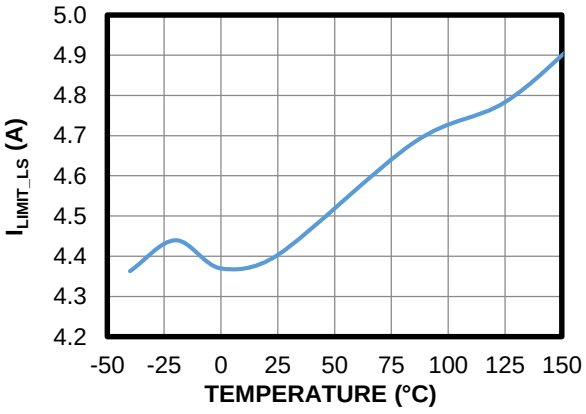
FB Voltage vs. Temperature



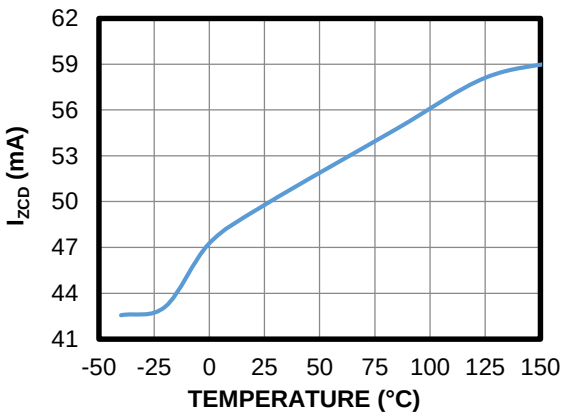
HS Peak Current Limit vs. Temperature



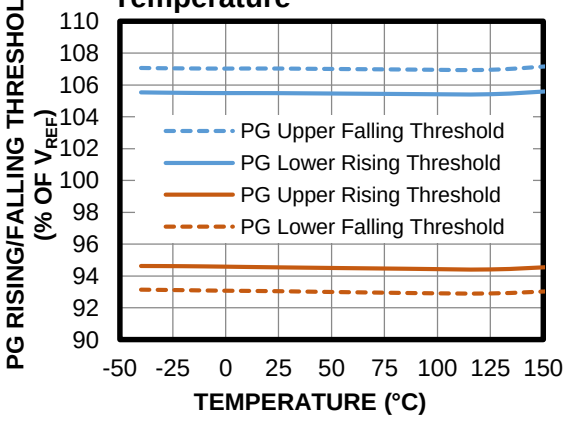
LS Valley Current Limit vs. Temperature



ZCD Current vs. Temperature



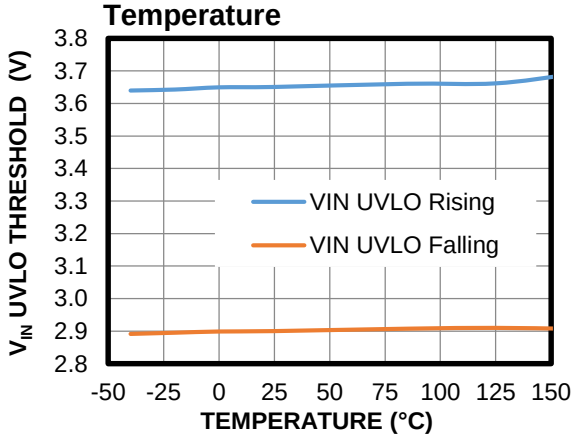
PG Rising/Falling Threshold vs. Temperature



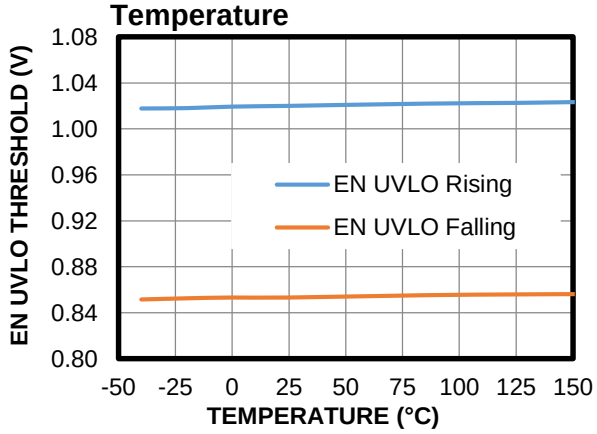
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

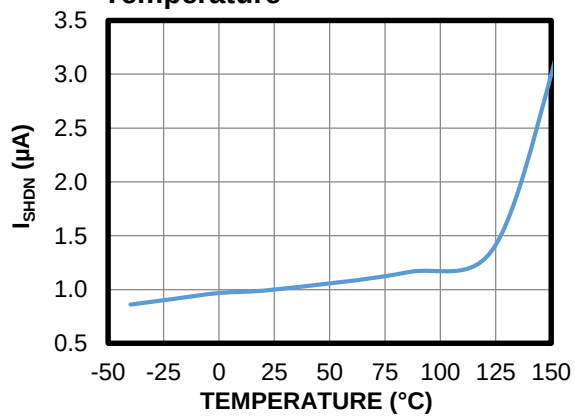
V_{IN} UVLO Threshold vs. Temperature



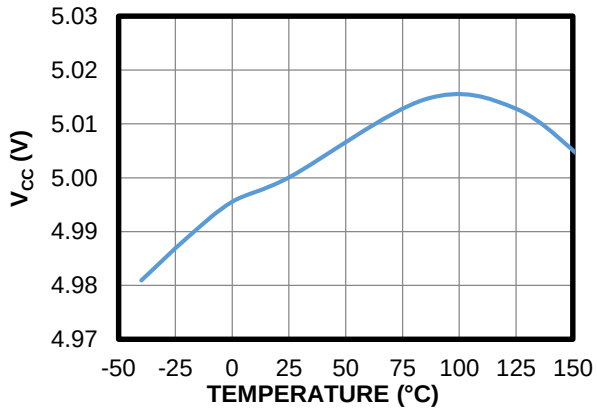
EN UVLO Threshold vs. Temperature



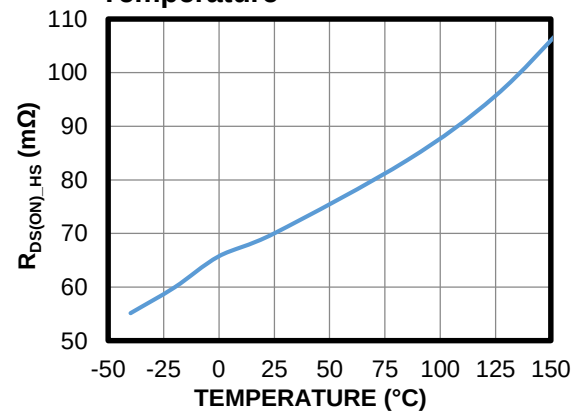
V_{IN} Shutdown Current vs. Temperature



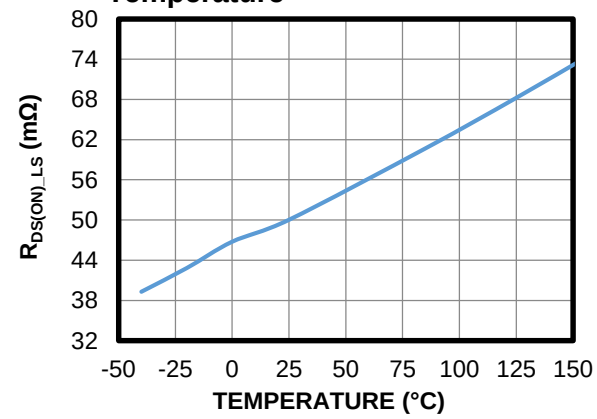
V_{CC} vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

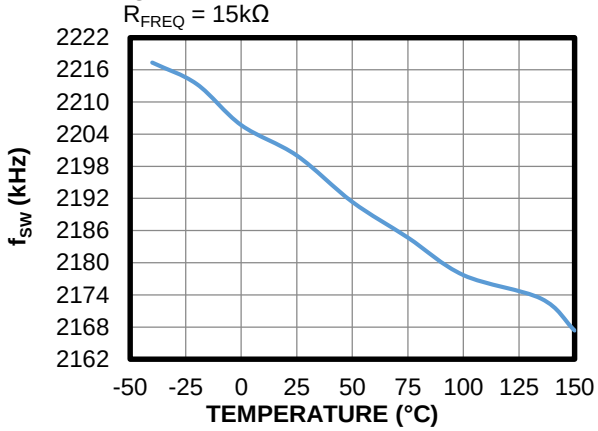


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

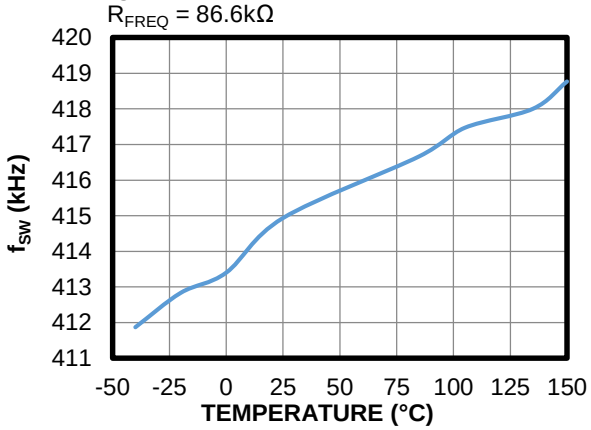
f_{SW} vs. Temperature

R_{FREQ} = 15kΩ



f_{SW} vs. Temperature

R_{FREQ} = 86.6kΩ

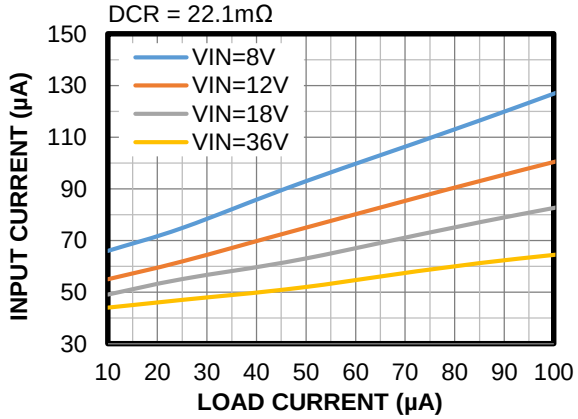


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

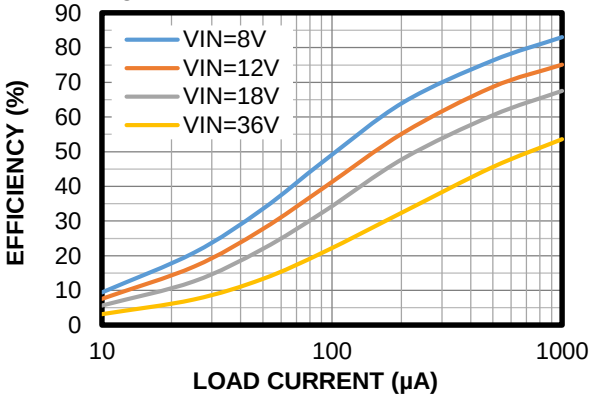
Input Current vs. Load Current

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 22.1mΩ



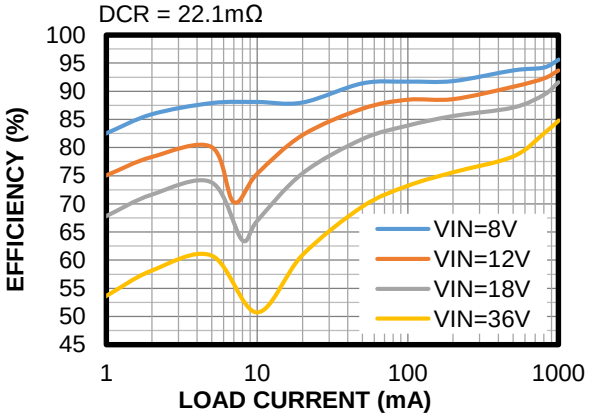
Efficiency vs. Load Current

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ,
DCR = 22.1mΩ



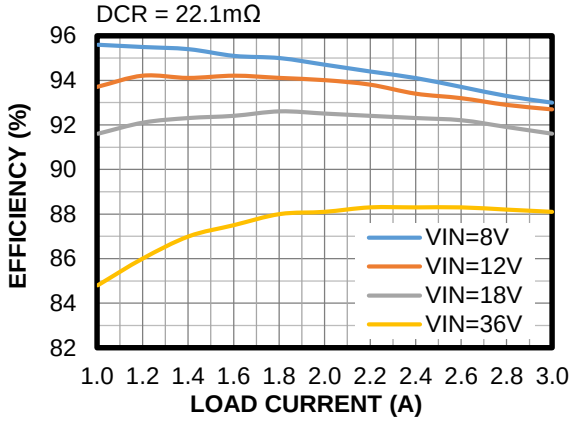
Efficiency vs. Load Current

DCR = 22.1mΩ



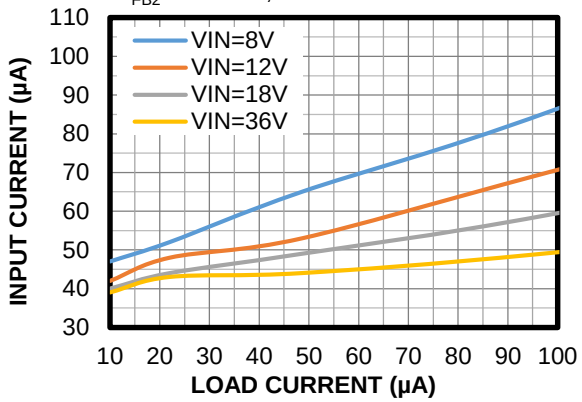
Efficiency vs. Load Current

DCR = 22.1mΩ



Input Current vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
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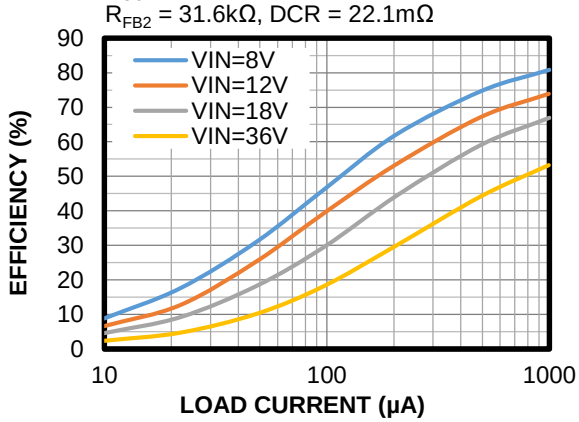
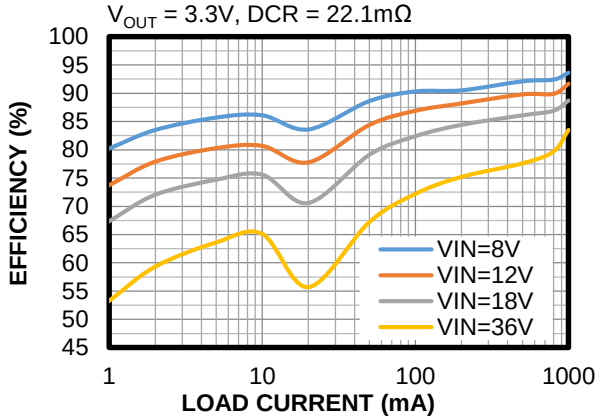


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

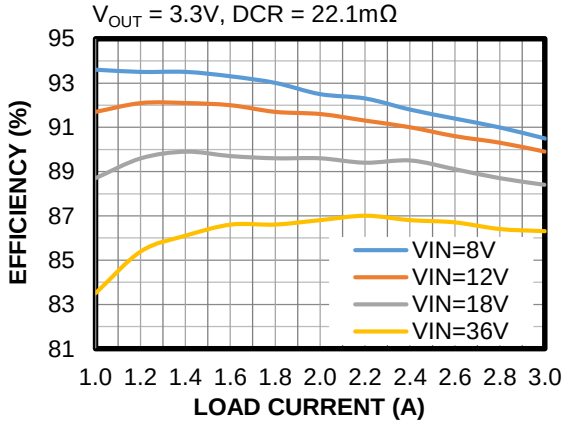
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



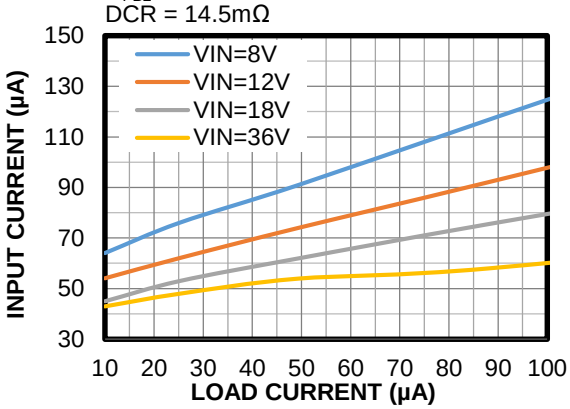
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



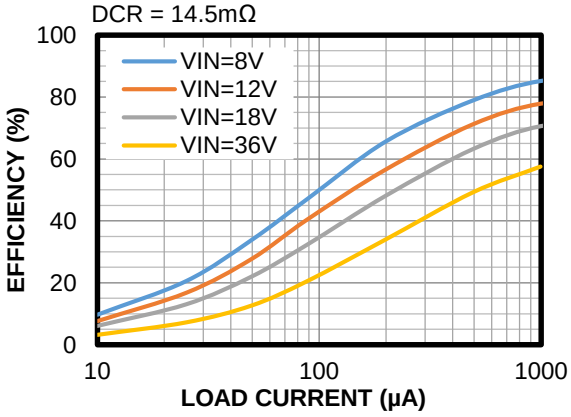
Input Current vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ,
R_{FB2} = 19.1kΩ, L = 5.6µH,
DCR = 14.5mΩ



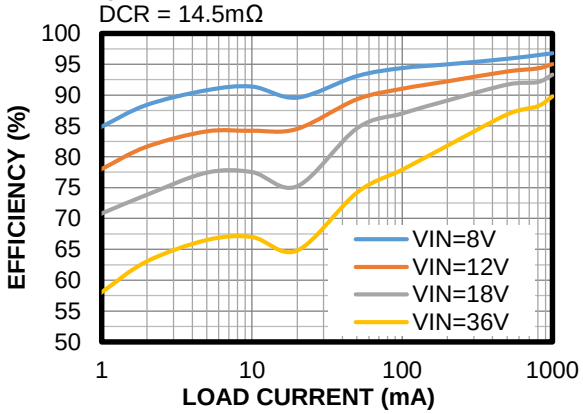
Efficiency vs. Load Current

f_{SW} = 415kHz, R_{FB1} = 100kΩ,
R_{FB2} = 19.1kΩ, L = 5.6µH,
DCR = 14.5mΩ



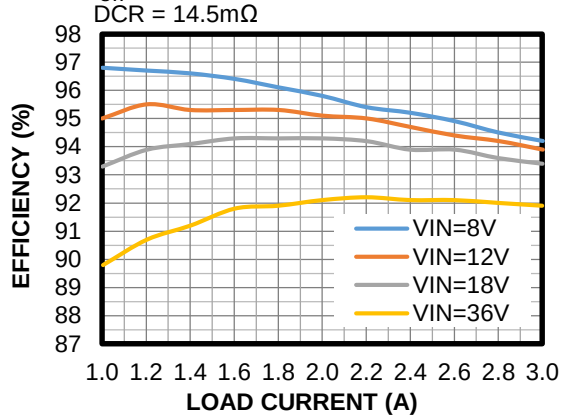
Efficiency vs. Load Current

f_{SW} = 415kHz, L = 5.6µH,
DCR = 14.5mΩ



Efficiency vs. Load Current

f_{SW} = 415kHz, L = 5.6µH,
DCR = 14.5mΩ

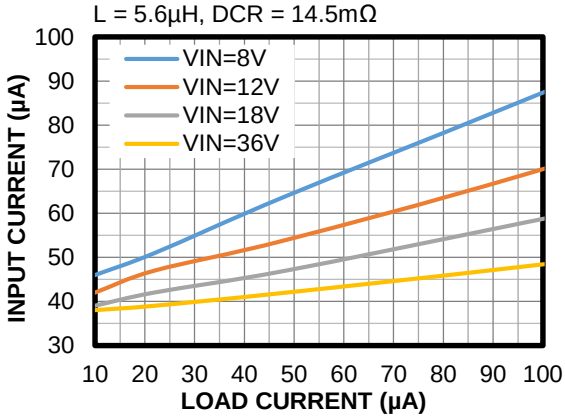


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

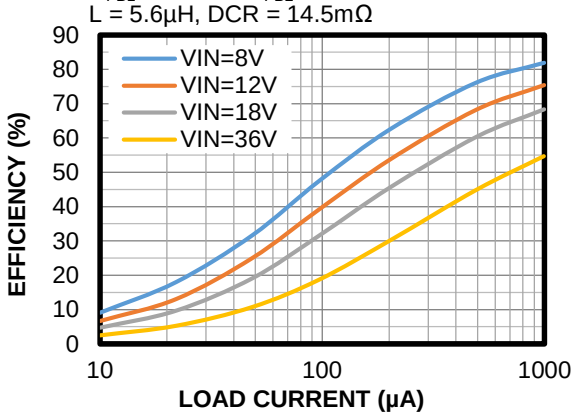
I_{IN} vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz,
R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ,
L = 5.6µH, DCR = 14.5mΩ



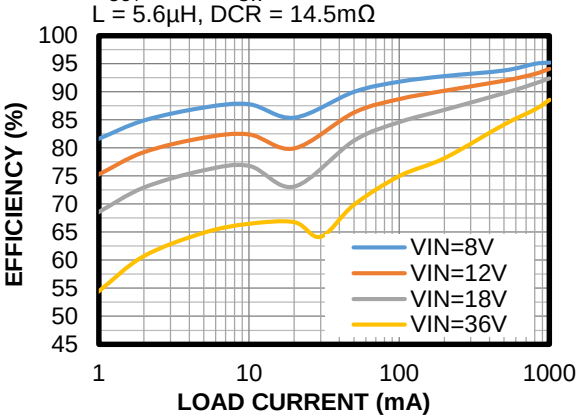
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz,
R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ,
L = 5.6µH, DCR = 14.5mΩ



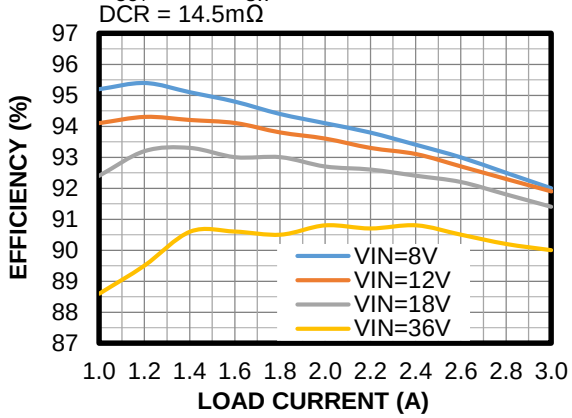
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz,
L = 5.6µH, DCR = 14.5mΩ



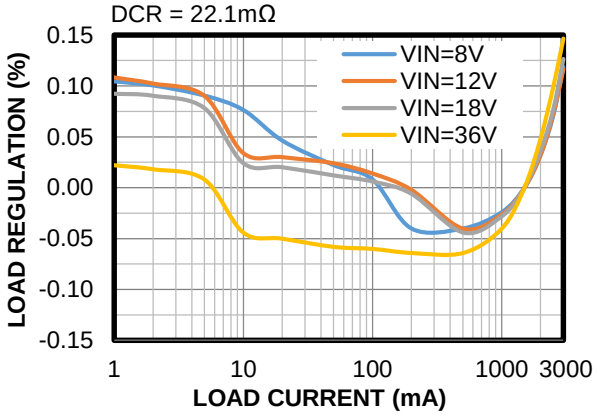
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH,
DCR = 14.5mΩ



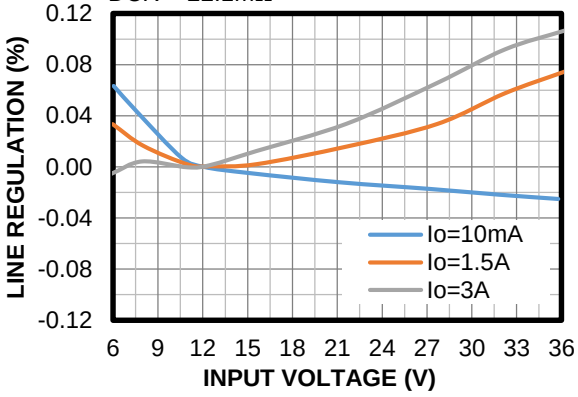
Load Regulation

DCR = 22.1mΩ



Line Regulation

DCR = 22.1mΩ

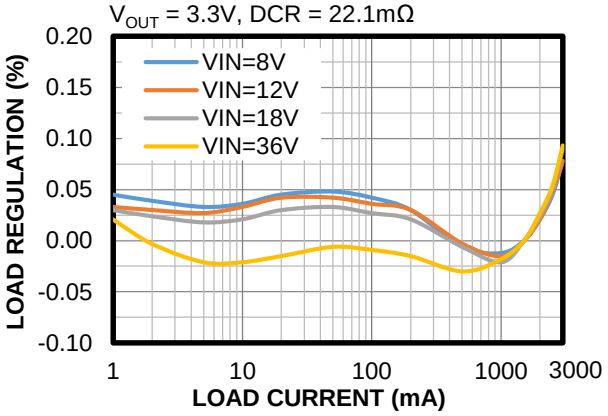


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

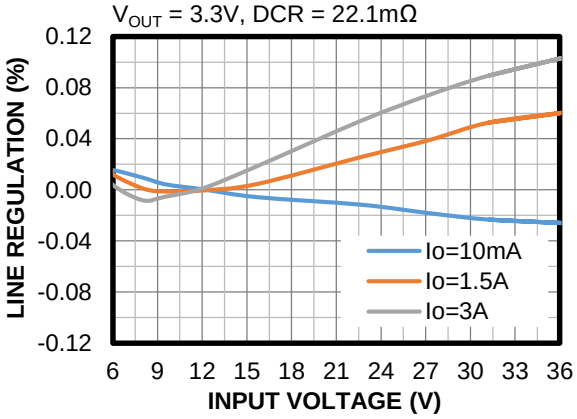
Load Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ



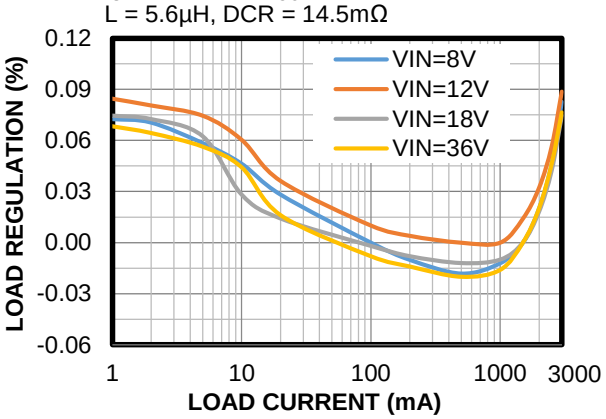
Line Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ



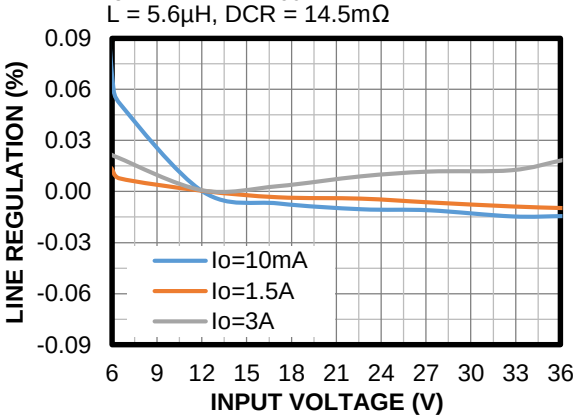
Load Regulation

f_{SW} = 415kHz, C_{OUT} = 47µF x 2,
L = 5.6µH, DCR = 14.5mΩ



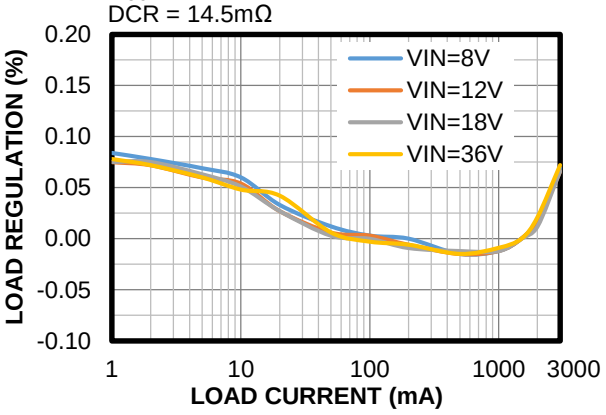
Line Regulation

f_{SW} = 415kHz, C_{OUT} = 47µF x 2,
L = 5.6µH, DCR = 14.5mΩ



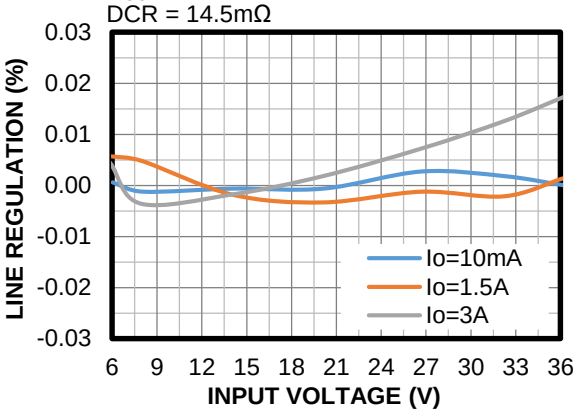
Load Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 47µFx 2, L = 5.6µH,
DCR = 14.5mΩ



Line Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 47µF x 2, L = 5.6µH,
DCR = 14.5mΩ

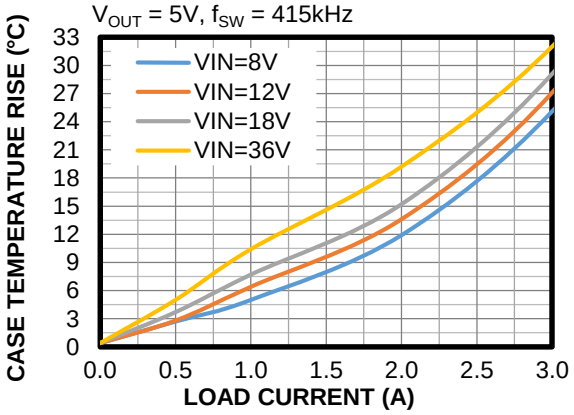


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

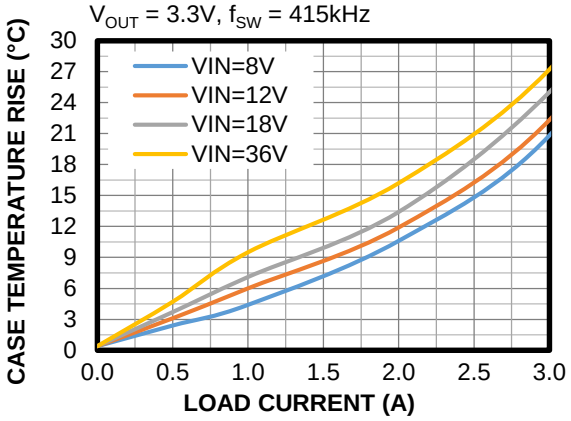
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 415kHz



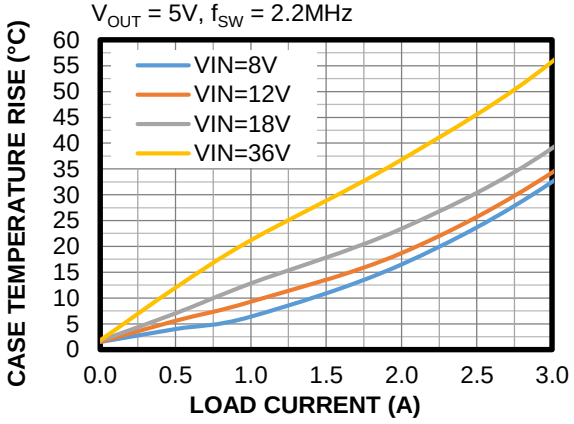
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 415kHz



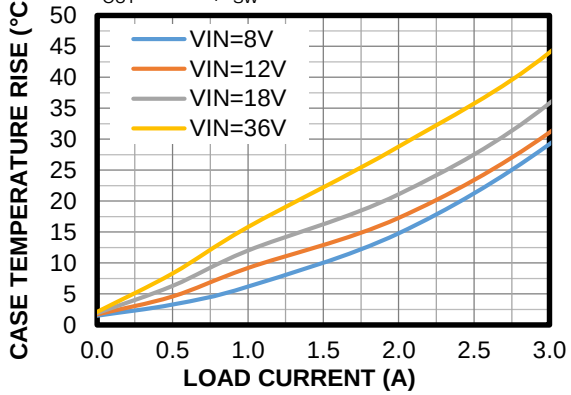
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz



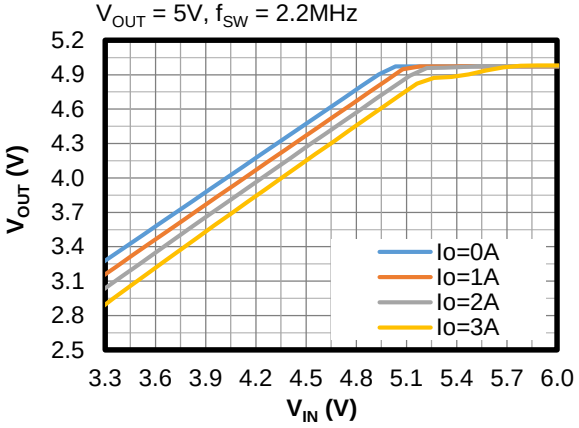
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz



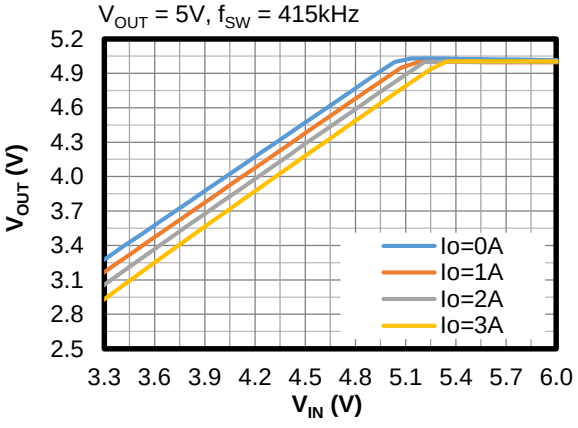
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz



Low-Dropout Mode

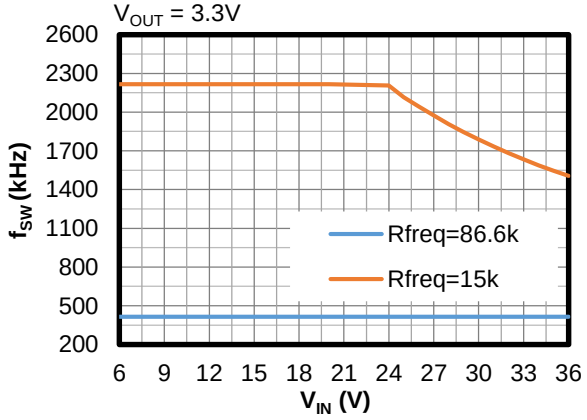
V_{OUT} = 5V, f_{SW} = 415kHz



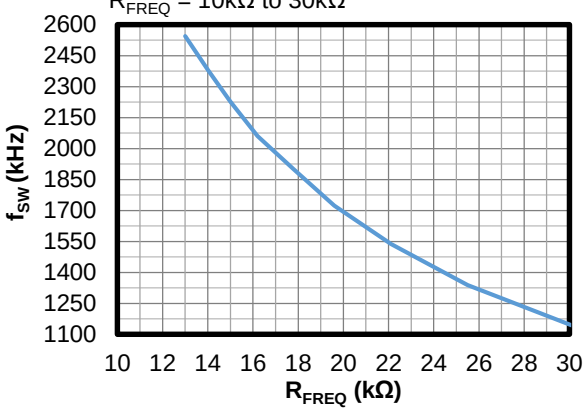
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

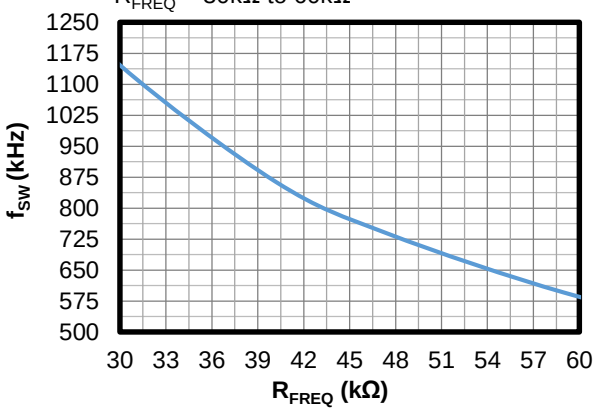
f_{SW} vs. V_{IN}
V_{OUT} = 3.3V



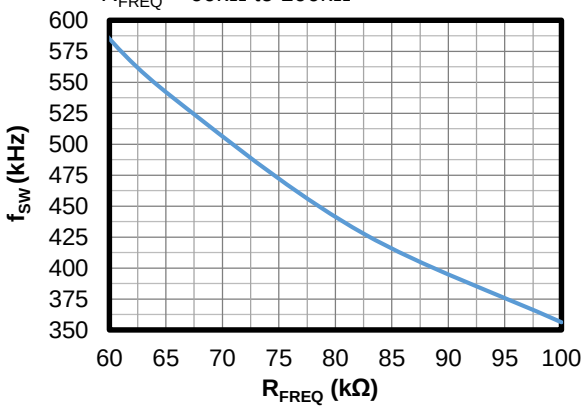
f_{SW} vs. R_{FREQ}
R_{FREQ} = 10kΩ to 30kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ} = 30kΩ to 60kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ} = 60kΩ to 100kΩ

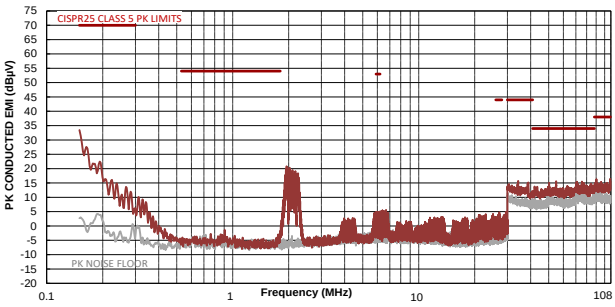


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (10)

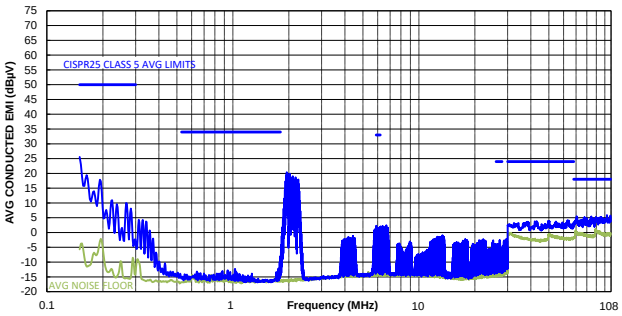
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



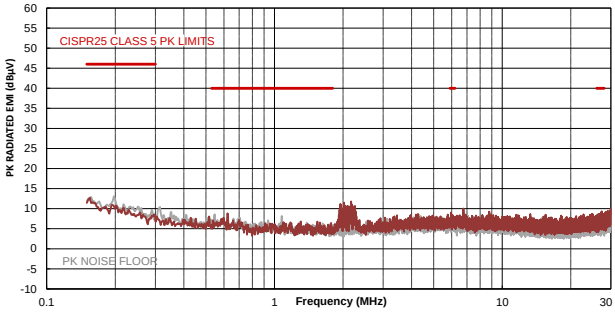
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



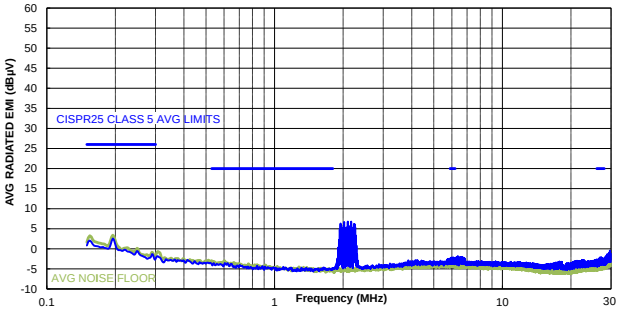
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



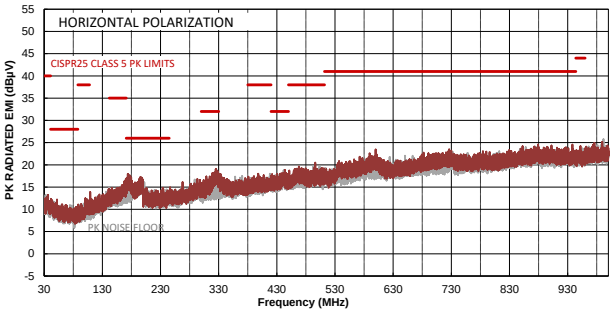
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



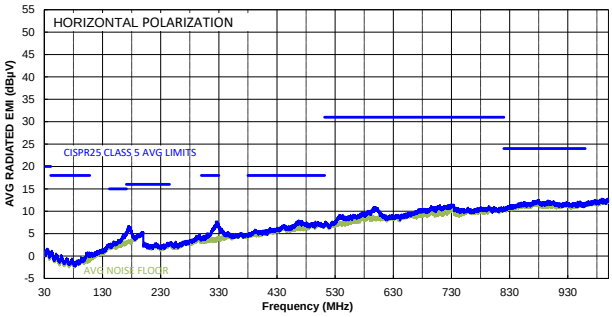
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

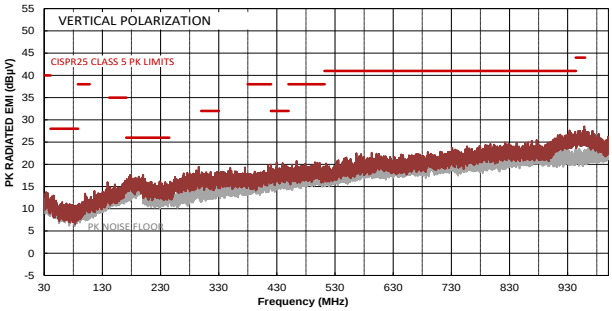


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (10)

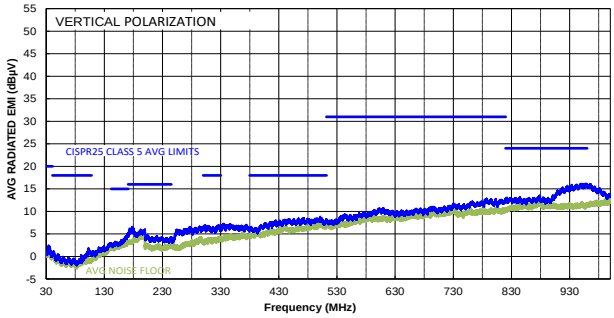
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

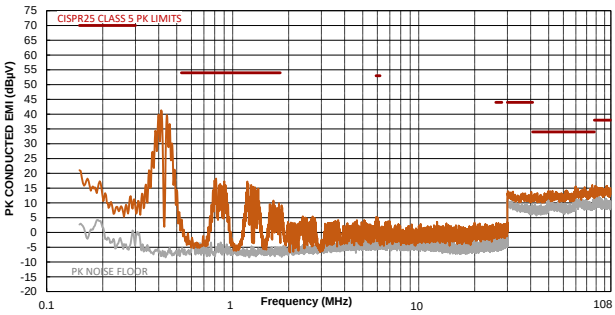
10) The EMC test results are based on the application circuit with EMI filters (see Figure 14 on page 38).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted. (11)

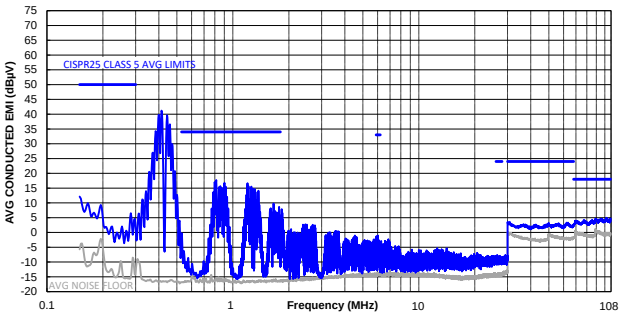
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



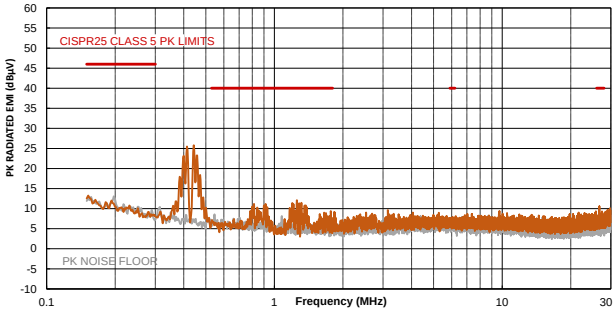
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



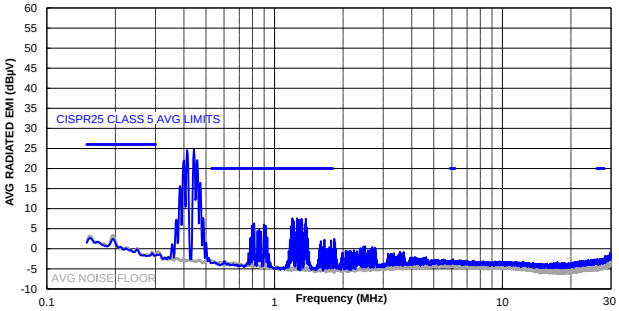
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



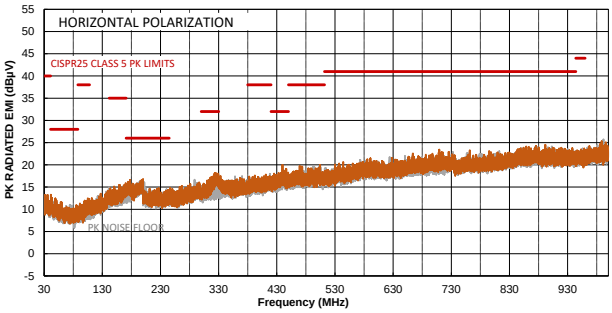
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



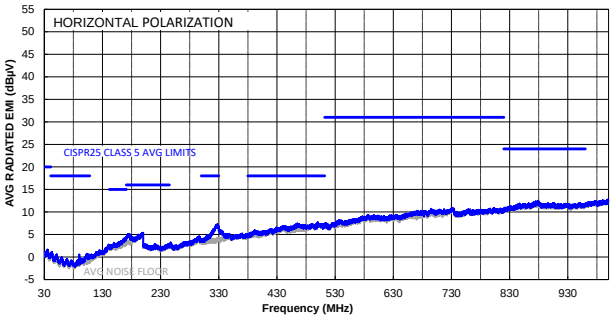
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

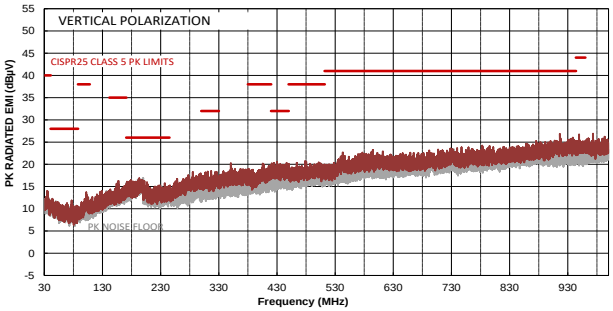


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted. (11)

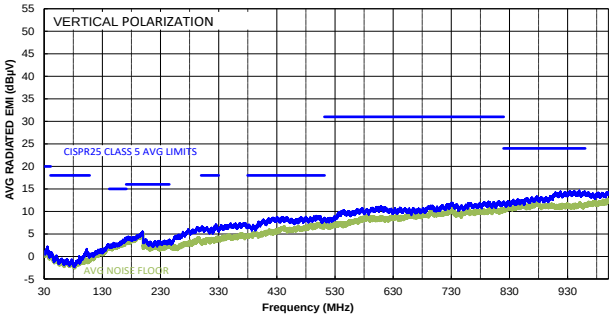
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



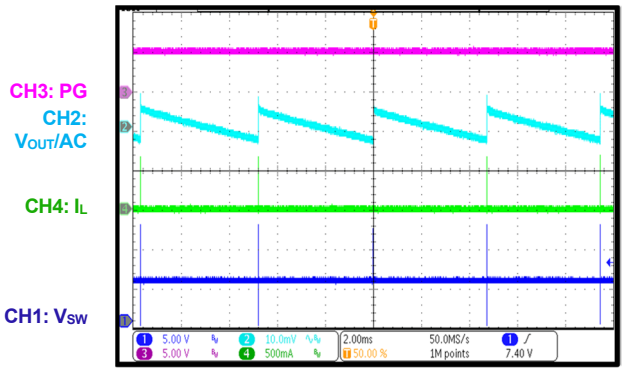
Note:

11) The EMC test results are based on the application circuit with EMI filters (see Figure 15 on page 39).

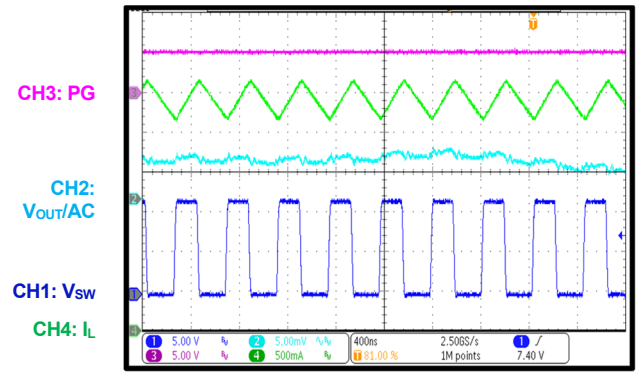
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

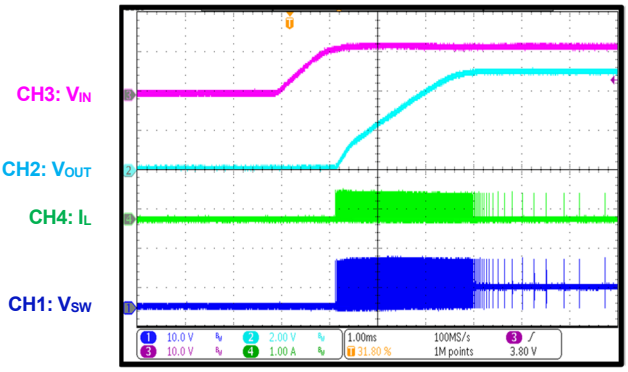
Steady State
I_{OUT} = 0A



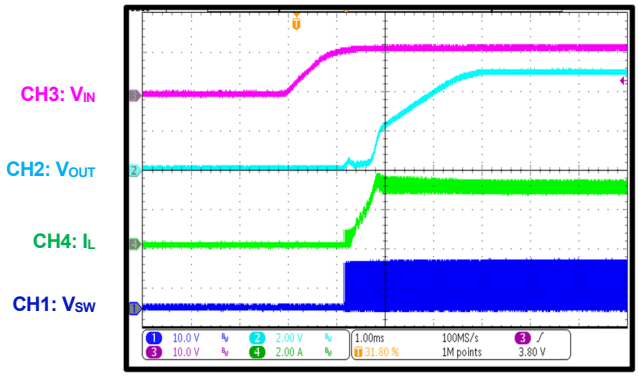
Steady State
I_{OUT} = 3A



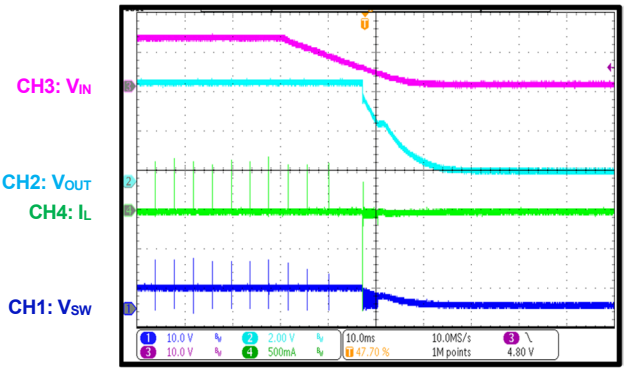
Start-Up through VIN
I_{OUT} = 0A



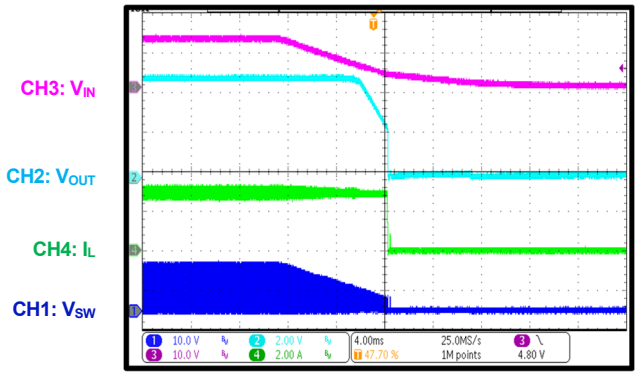
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A



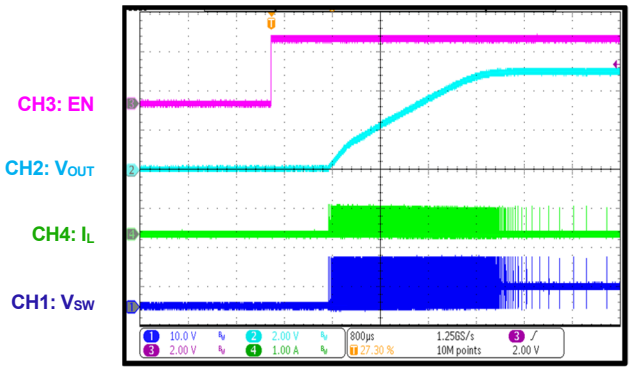
Shutdown through VIN
I_{OUT} = 3A



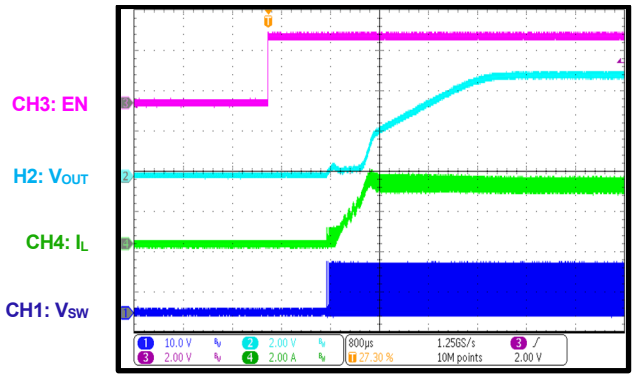
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

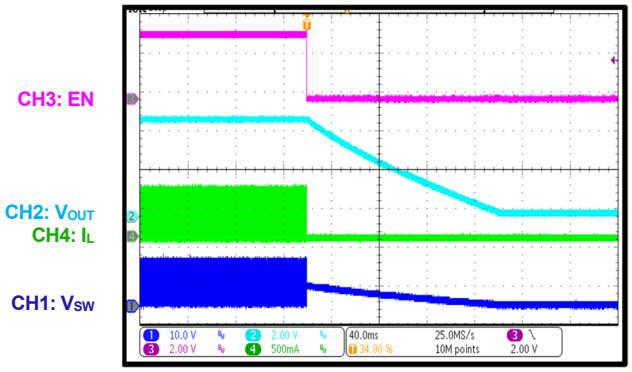
Start-Up through EN
I_{OUT} = 0A



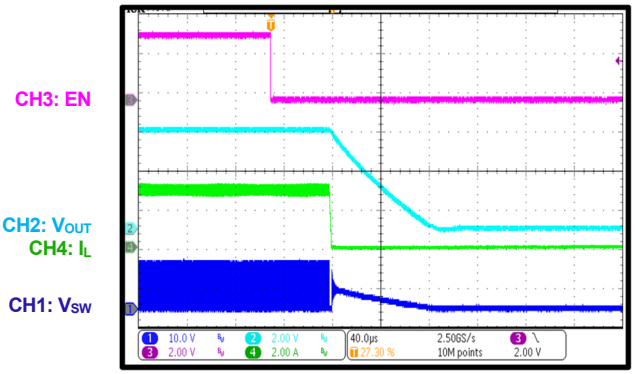
Start-Up through EN
I_{OUT} = 3A



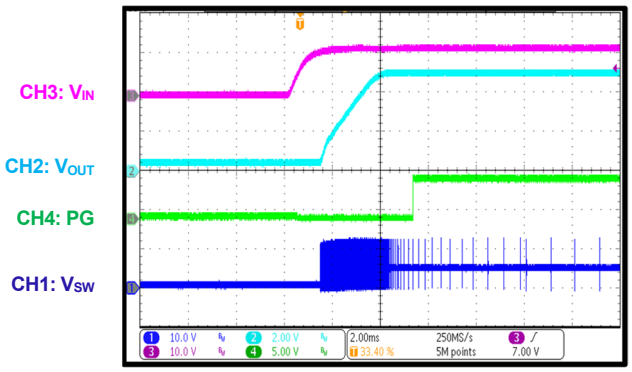
Shutdown through EN
I_{OUT} = 0A



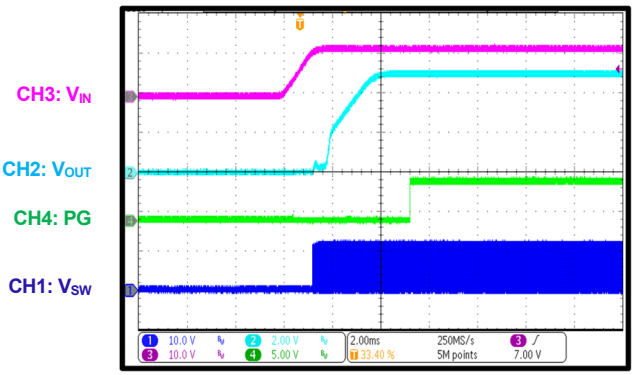
Shutdown through EN
I_{OUT} = 3A



PG Start-Up through VIN
I_{OUT} = 0A



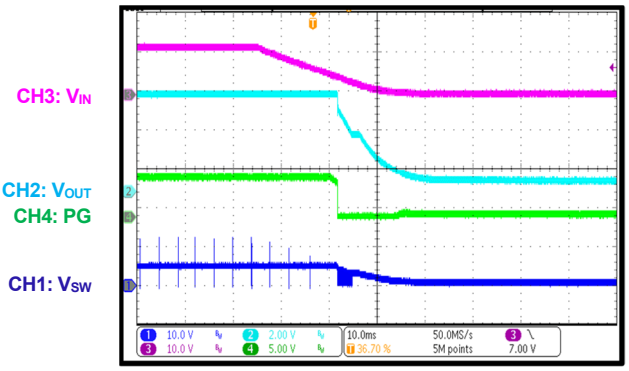
PG Start-Up through VIN
I_{OUT} = 3A



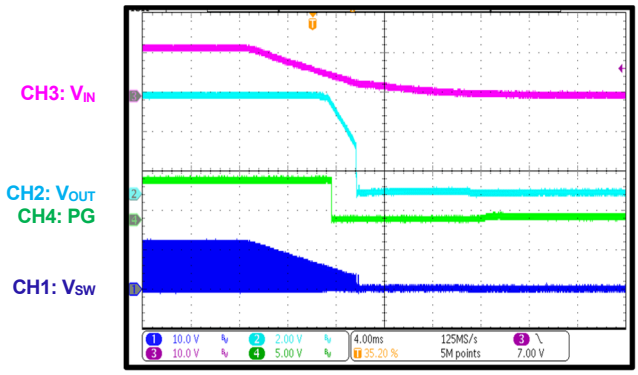
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

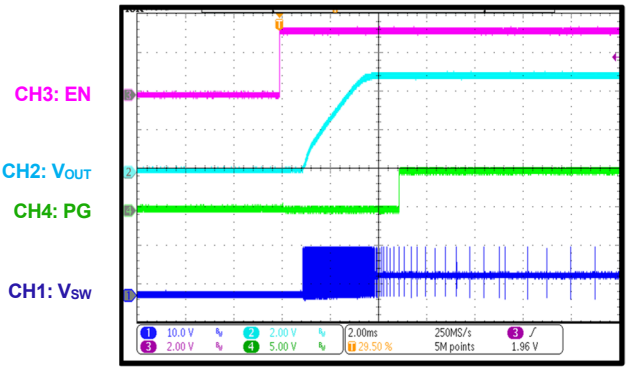
PG Shutdown through VIN
I_{OUT} = 0A



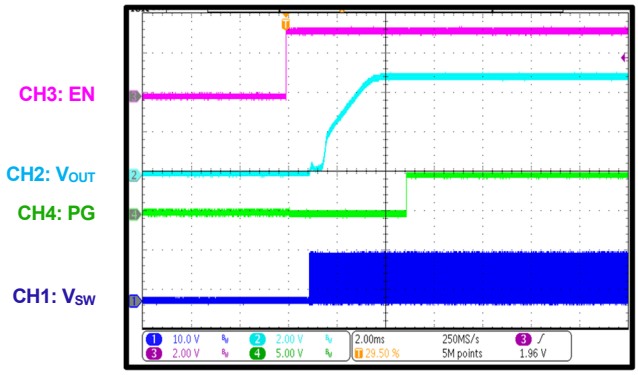
PG Shutdown through VIN
I_{OUT} = 3A



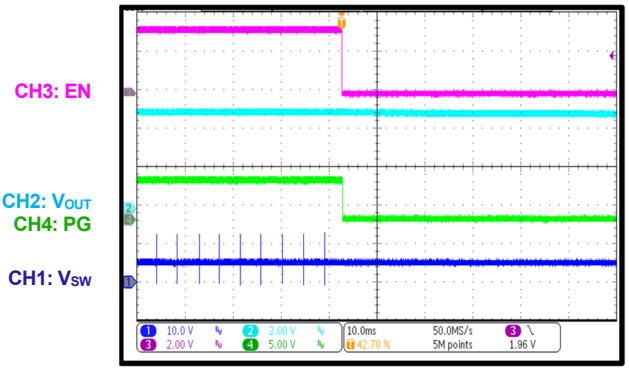
PG Start-Up through EN
I_{OUT} = 0A



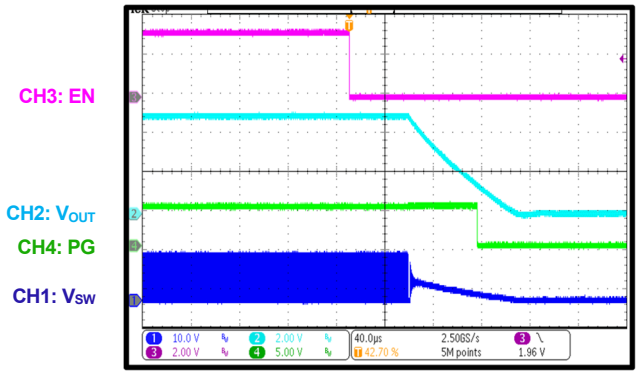
PG Start-Up through EN
I_{OUT} = 3A



PG Shutdown through EN
I_{OUT} = 0A



PG Shutdown through EN
I_{OUT} = 3A

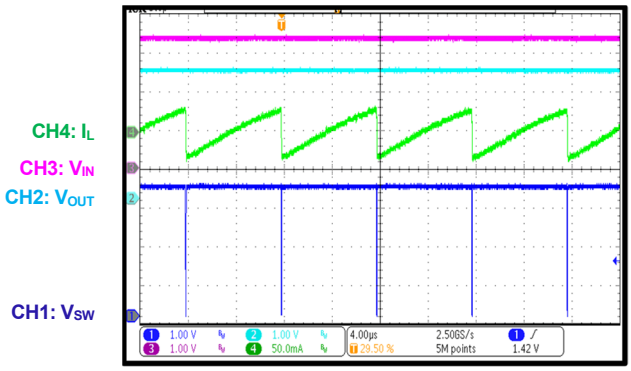


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

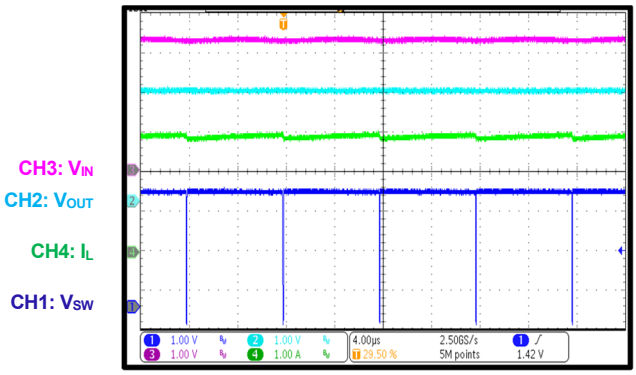
Low-Dropout Mode

I_{OUT} = 0A, V_{IN} = 3.3V



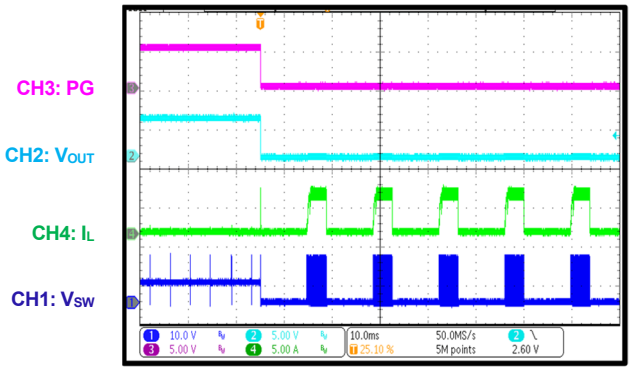
Low-Dropout Mode

I_{OUT} = 3A, V_{IN} = 3.3V



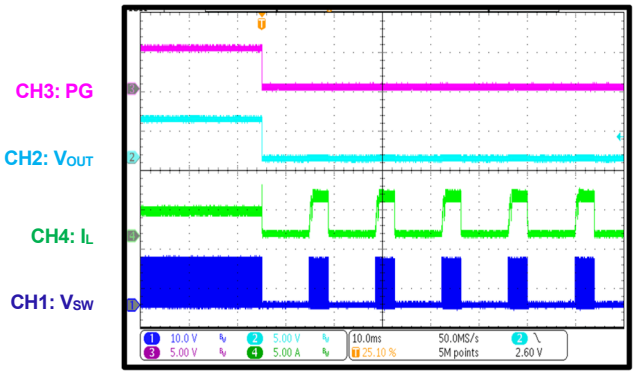
SCP Entry

I_{OUT} = 0A



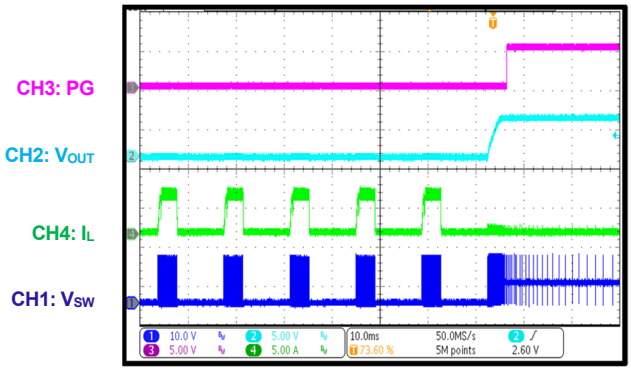
SCP Entry

I_{OUT} = 3A



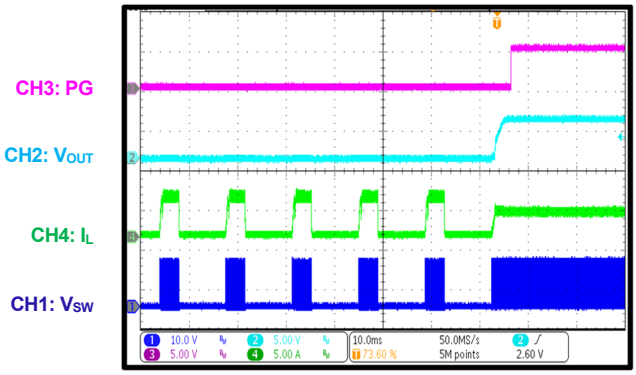
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 3A

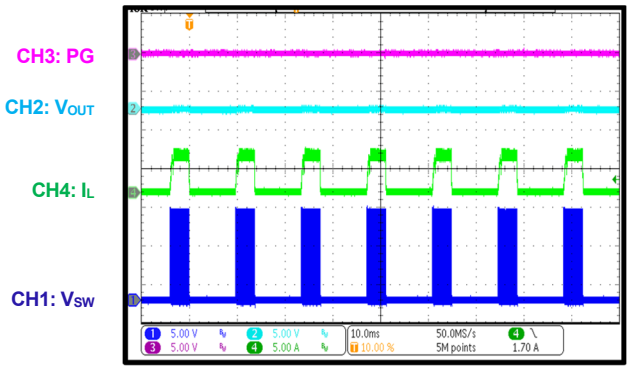


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

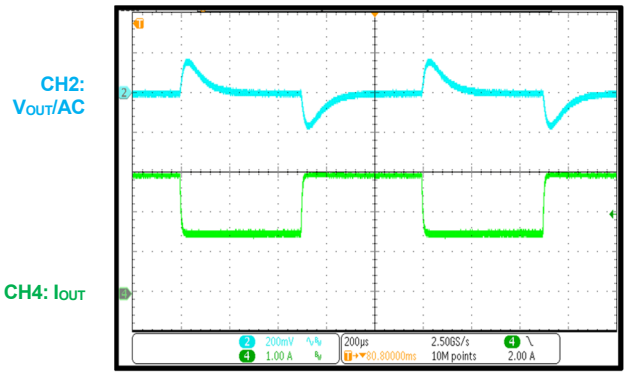
SCP Steady State

I_{OUT} = 0A



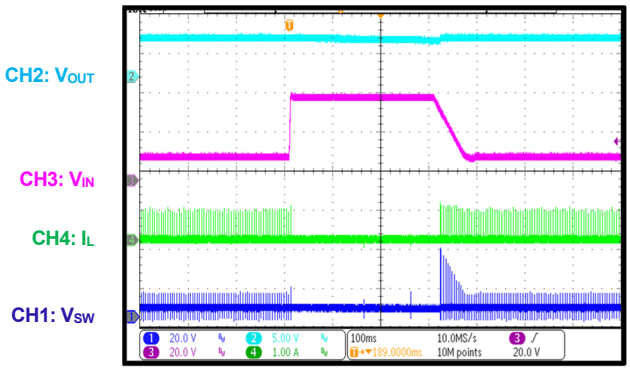
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



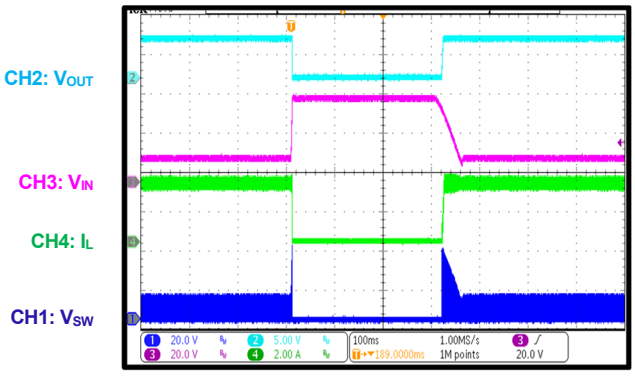
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 0A



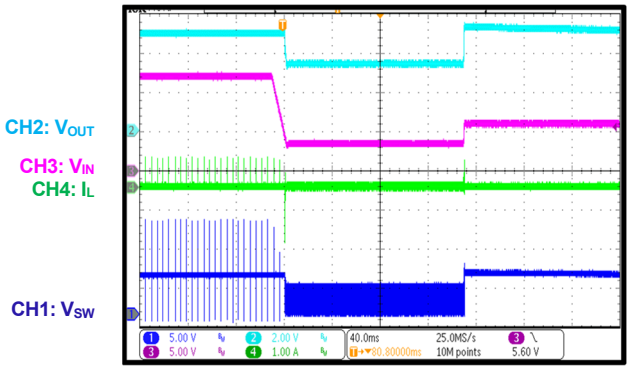
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 3A



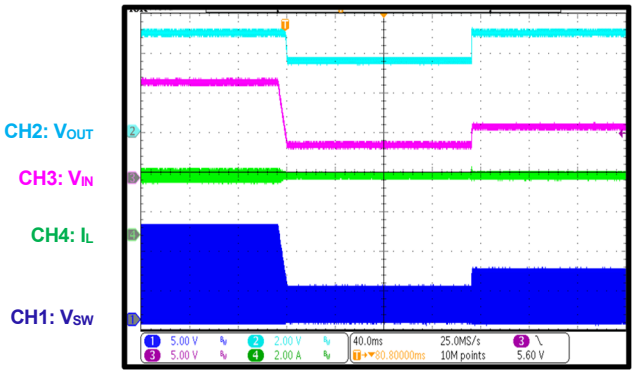
Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 0A



Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 3A

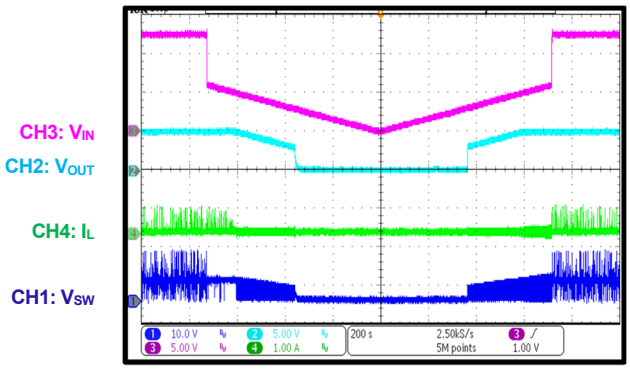


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

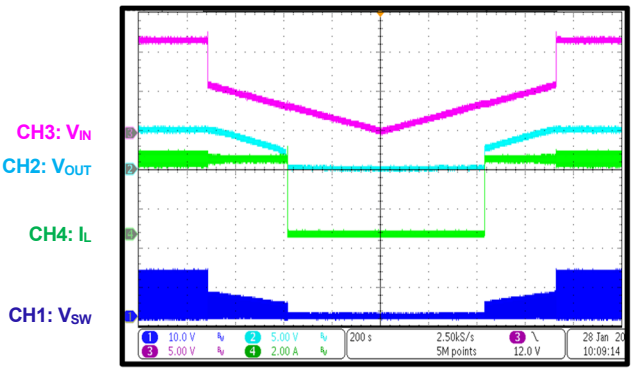
V_{IN} Ramping Down and Up

V_{IN} = 6V to 0V, 0.5V/min, I_{OUT} = 0A



V_{IN} Ramping Down and Up

V_{IN} = 6V to 0V, 0.5V/min, I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

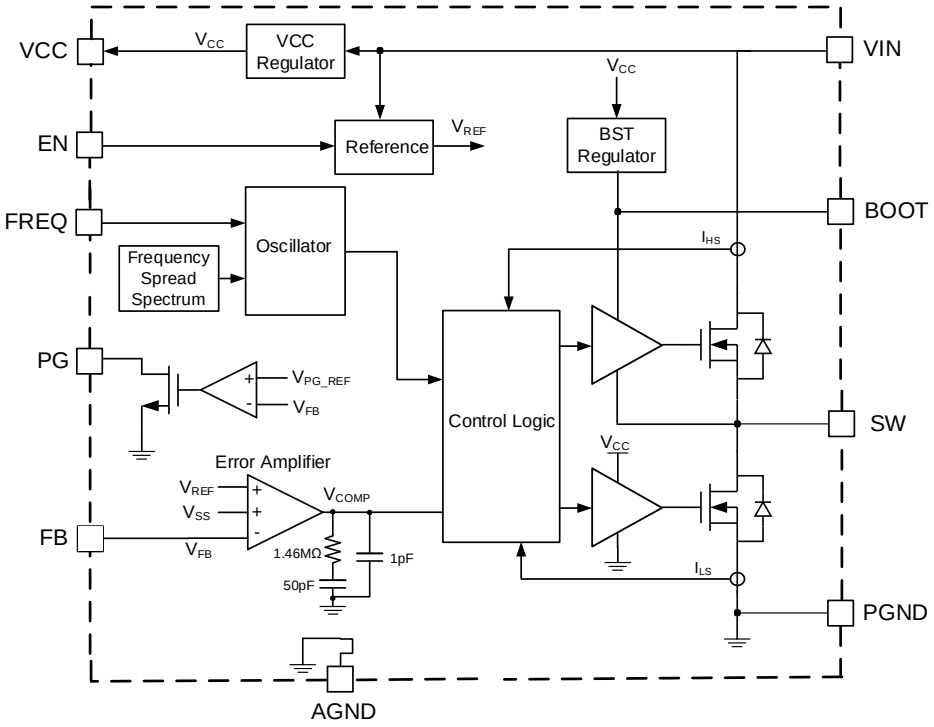


Figure 1: Functional Block Diagram (Adjustable Output)

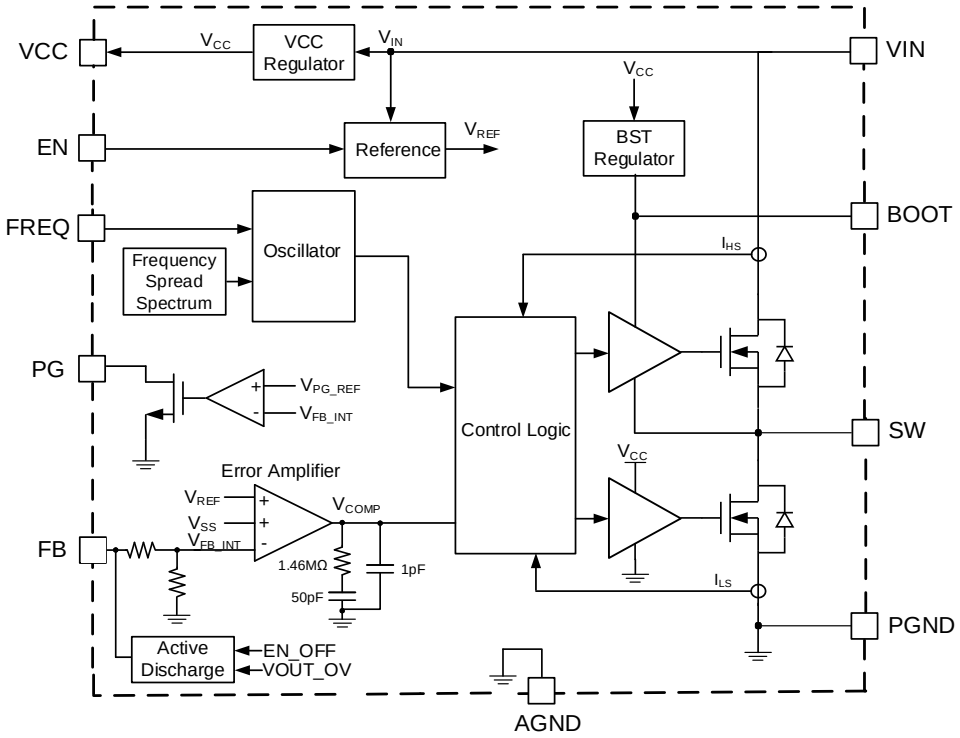


Figure 2: Functional Block Diagram (Fixed Output)

OPERATION

The MPQ4323M is a synchronous, step-down switching regulator with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). The device provides 3A of highly efficient output current (I_{OUT}) with peak current mode control.

The device features a wide input voltage (V_{IN}) range, configurable 350kHz to 2.5MHz switching frequency (f_{SW}), internal soft start (SS), and a precise current limit. The MPQ4323M's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4323M operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts, or until the inductor current (I_L) drops below the zero current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time before the next cycle starts.

If the current in the HS-FET cannot reach the value set by COMP within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until it reaches the value set by COMP, or its 7µs maximum on time is reached. This operation mode extends the duty cycle, which achieves a very low dropout when V_{IN} is almost equal to V_{OUT}.

Light-Load Operation

The MPQ4323M works in advanced asynchronous modulation (AAM) mode to optimize efficiency under light-load and no-load conditions.

When I_L approaches 0A under light-load conditions, the MPQ4323M initiates asynchronous operation. If the load further decreases and V_{COMP} drops below the set value, then the device enters AAM mode (see Figure 3).

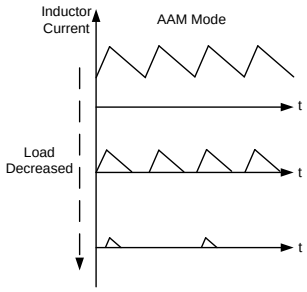


Figure 3: AAM Operation

In AAM mode, the internal clock is reset every time V_{COMP} crosses over the set value, and the crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) with the internal reference voltage (V_{REF}, typically 0.8V) and outputs a current proportional to the difference between the two values. This I_{OUT} is then used to charge the compensation network to form V_{COMP}, which provides the error that controls the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and its maximum is clamped to 2V. COMP is internally pulled down to GND in shutdown mode.

Frequency Spread Spectrum (FSS)

The MPQ4323M uses a 15kHz modulation frequency with a maximum 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps vary with the set oscillator frequency to ensure that the exact f_{SW} steps cycle by cycle (see Figure 4).

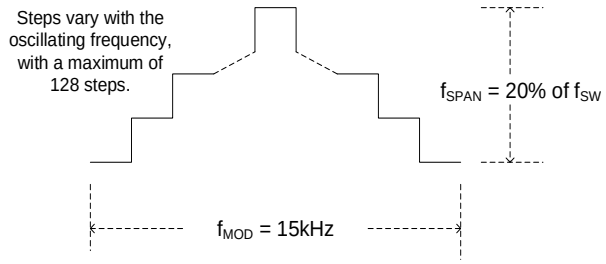


Figure 4: Frequency Spread Spectrum

Side bands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is reduced. This significantly reduces the peak EMI noise.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

When the SS period starts, the SS voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. When V_{SS} is below the internal V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

When the chip is enabled by EN, the first pulse is sent after about 830µs. During this period, the VCC voltage (V_{CC}) is regulated, and the internal bias and charging of the compensator network are completed. After another 2.9ms, V_{OUT} ramps up and reaches the set value. Then SS completes after 1.5ms, and PG pulls high after a 70µs delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, the output has a pre-biased voltage. In this condition, neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 175°C), the device shuts down the power MOSFETs. Once the temperature drops below its lower threshold (about 155°C), then the thermal shutdown condition is removed and the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable V_{REF} and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

When the internal supply rail is up, the internal circuits start to work. If BOOT does not reach its refresh rising threshold (about 2.5V), the LS-FET turns on to charge BOOT. The HS-FET remains off during this time. Once the SS block is enabled, V_{OUT} starts to ramp up slowly. V_{OUT} smoothly reaches its target within 5ms.

Three events can shut down the chip: EN going low, V_{IN} falling below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} is pulled down, and the floating driver works to disable the HS-FET.

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current limit protection. If I_L reaches the high-side (HS) peak current limit (typically 5.8A) while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit (typically 4.4A). Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground and V_{OUT} drops below 70% of its nominal output, the MPQ4323M shuts down and begins discharging V_{SS}. The device restarts with a full SS when V_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

The MPQ4323M stops switching if V_{OUT} exceeds 130% of its nominal regulation value, and then an internal 75Ω discharge path from FB to GND is activated to discharge V_{OUT}. This discharge path can only be activated for the fixed-output version. The part resumes switching once V_{OUT} drops back to 125% of its nominal value. The discharge path of the fixed-output version is also disabled.

For the fixed-output version, the V_{OUT} discharge path is activated if an EN shutdown occurs until V_{CC} drops to the V_{IN} UVLO threshold.

APPLICATION INFORMATION

Figure 5 shows the MPQ4323M's typical application circuit.

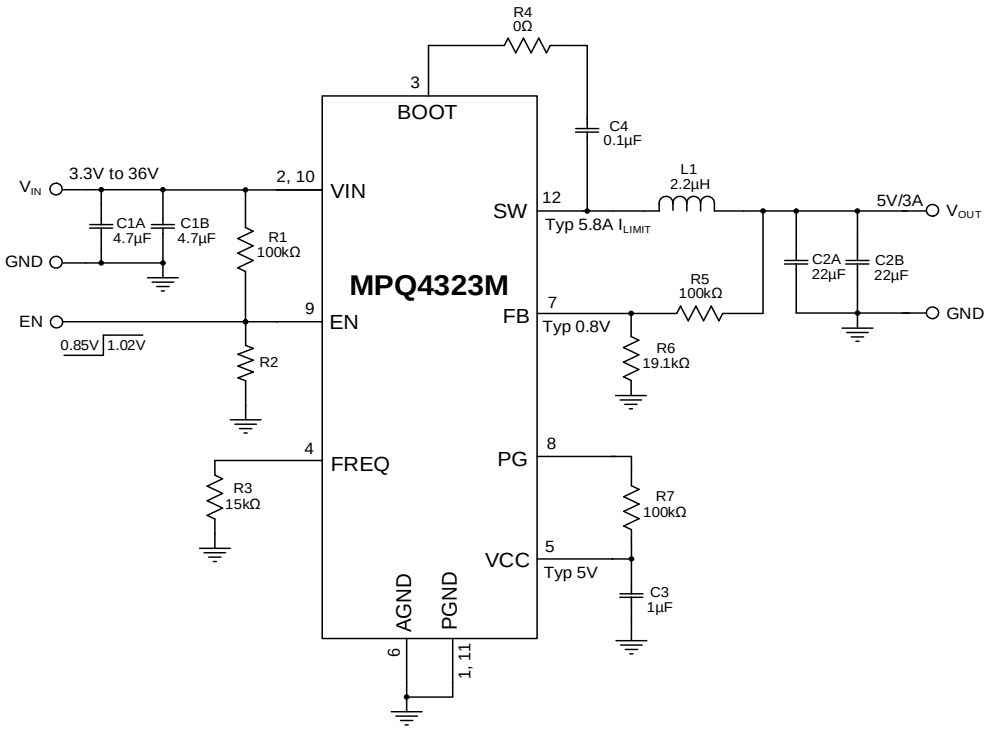


Figure 5: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 11	PGND	-	GND Connection (GND, Pins 1, 6, and 11)
2, 10	VIN	C1A, C1B	Selecting the Input Capacitors (VIN, Pins 2 and 10)
3	BOOT	R4, C4	The Floating Driver and Bootstrap Charging (BOOT)
4	FREQ	R3	Setting the Switching Frequency (FREQ)
5	VCC	C3	Internal VCC (VCC)
6	AGND	-	GND Connection (GND, Pins 1, 6, and 11)
7	FB	R5, R6	Feedback (FB)
8	PG	R7	Power Good (PG) Indication
9	EN	R1, R2	Enable (EN) and UVLO
12	SW	L1, C2A, C2B	Selecting the Inductor and Output Capacitors (SW)

Selecting the Input Capacitors (VIN, Pins 2 and 10)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. Place the capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated using Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, C_{IN} should have an RMS current rating greater than half of the maximum load current. C_{IN} can be electrolytic, tantalum, or ceramic. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated using Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

V_{IN} Over-Voltage Protection (OVP)

If V_{IN} exceeds its over-voltage (OV) rising threshold (typically 37.5V), the MPQ4323M stops switching. Once V_{IN} drops below the OV falling threshold (typically 36.5V), the device resumes normal regulation and switching.

The Floating Driver and Bootstrap Charging (BOOT)

The BOOT capacitor (C4) is recommended to be between 0.1µF to 1µF.

It is not recommended to place a resistor (R_{BOOT}) in series with C4, unless there is a strict EMI requirement. R_{BOOT} helps enhance EMI performance and reduce voltage stress at high input voltages, but it also generates additional power consumption and reduces efficiency. When R_{BOOT} is necessary, it should be below 4Ω.

The voltage between BOOT and SW ($V_{BOOT-SW}$) is regulated to about 5V by the dedicated internal bootstrap (BST) regulator. When $V_{BOOT-SW}$ is below its regulated value, a P-channel MOSFET pass transistor connected from VCC to BOOT turns on to charge the BST capacitor (C_{BOOT}). The external circuit should provide enough voltage headroom to facilitate the charging. When the HS-FET is on, the BOOT voltage (V_{BOOT}) exceeds V_{CC}, so C_{BOOT} cannot be charged.

Under conditions with higher duty cycles, the time available for BST charging is shorter, so C_{BOOT} may not be charged sufficiently. In this case, the external circuit has insufficient voltage and time to charge C_{BOOT}. External circuitry can be used to ensure that the BST voltage (V_{BST}) remains within the normal operation range.

If V_{BST} reaches its UVLO threshold, the HS-FET turns off and the LS-FET turns on with a minimum off time to refresh V_{BST} with the set f_{SW}.

Setting the Switching Frequency (FREQ)

A resistor (R3) can set f_{SW} (see Table 2 on page 32 and the f_{SW} vs. R_{FREQ} curves on page 16).

The MPQ4323M's f_{SW} can be configured by an external resistor (R_{FREQ}) connected from the FREQ pin to ground. The frequency resistor should be located between the FREQ pin and GND, placed as close as possible to the device. Table 2 on page 32 shows the relationship between f_{SW} and R_{FREQ}.

Table 2: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)	R_{FREQ} (kΩ)	f_{SW} (kHz)
100	355	30.1	1150
93.1	385	26.1	1300
86.6	415	22.6	1450
80.6	450	20.5	1600
75	480	19.6	1750
68.1	520	17.8	1900
59	600	16.2	2050
51.1	700	15	2200
40.2	850	14.3	2350
34.8	1000	13.3	2500

It is not possible to have both a high f_{SW} and V_{IN} due to the HS-FET's limited minimum on time. The MPQ4323M's control loop automatically sets the maximum possible f_{SW} to the set frequency, which also reduces excessive power loss. V_{OUT} is regulated by varying the duration of the HS-FET's switch-off time, which automatically reduces f_{SW}.

The device is guaranteed to comply with the HS-FET's minimum on time. An advantage of this method is that the device works at the target f_{SW} for as long as possible, and f_{SW} only changes when the device operates at high input voltages. For more details, see the f_{SW} vs. V_{IN} curves on page 16. In this scenario, R_{FREQ} = 15kΩ and V_{OUT} = 3.3V.

Internal VCC (VCC)

The VCC capacitor (C3) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} drops below 5V, V_{CC} degrades.

Feedback (FB)

The feedback (FB) voltage (V_{FB}) is typically 0.8V, and its output can be adjusted. The external resistor divider connected to FB sets V_{OUT} (see Figure 6).

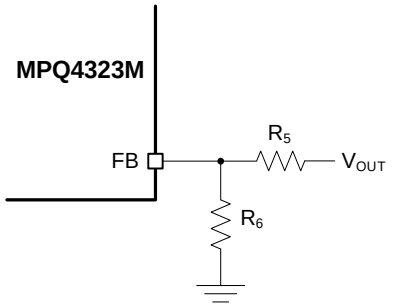


Figure 6: FB Divider Network (Adjustable-Output Version)

Calculate R_6 using Equation (4):

$$R_6 = \frac{R_5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For a fixed output, the FB resistor divider is integrated internally. This means that FB should be directly connected to the output to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V (see Figure 7).

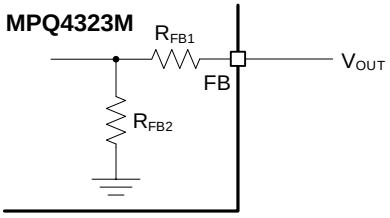


Figure 7: FB Divider Network (Fixed-Output Version)

Table 3 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 3: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3.0	704	256
3.3	800	256
3.8	960	256
5	1344	256

Power Good (PG) Indication

The PG resistor (R7) should have a resistance (R_{PG}) of about 100kΩ.

The MPQ4323M includes an open-drain PG output that indicates whether the regulator output is within its nominal value window.

If using the PG pin, connect it to a logic high power source (e.g. 3.3V) via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high. If V_{OUT} is above 107% or below 93% of the nominal voltage, PG goes low. Float PG if it is not used.

Enable (EN) and UVLO

EN is a digital control pin that turns the regulator on and off.

Enabled by External Logic High/Low Signal

When the EN voltage reaches 0.7V, the bottom gate does not turn on until V_{IN} exceeds 2.7V. The bottom gate then provides an accurate V_{REF} for the EN threshold. Forcing EN above its rising threshold (about 1.02V) turns the device on. Turn the device off by driving EN below 0.85V. There is no internal pull-up or pull-down resistor connected to the EN pin, so do not float EN. An external pull-up or pull-down resistor is required if the control signal cannot give an accurate high or low logic.

Configurable V_{IN} UVLO

The MPQ4323M has an internal, fixed UVLO threshold. The rising threshold is 3.65V, while the falling threshold is about 2.9V. For applications that require a higher UVLO point, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 8).

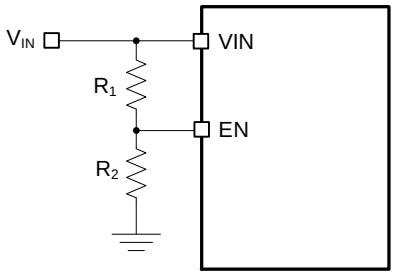


Figure 8: Adjustable UVLO Using EN Divider

The UVLO rising threshold ($V_{IN\_UVLO\_RISING}$) can be calculated using Equation (5):

$$V_{IN\_UVLO\_RISING} = (1+\frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

The UVLO falling threshold ($V_{IN\_UVLO\_FALLING}$) can be calculated using Equation (6):

$$V_{IN\_UVLO\_FALLING} = (1+\frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where V_{EN_RISING} is 1.02V, and $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to control when the device turns on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and Output Capacitors (SW)

The inductance (L_1) can be estimated using Equation (7):

$$L_1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{LP}) can be calculated using Equation (8):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L_1} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under the maximum I_{LP}.

The output voltage ripple (ΔV_{OUT}) can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times (1-\frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}) \quad (9)$$

Where L_1 is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated using Equation (12):

$$C_{OUT} = \frac{I_{OUT}^{2} \times L}{V_{OUT}^{2} \times ((V_{OUTMAX} / V_{OUT})^{2} - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance value.

The characteristics of C_{OUT} also affect the stability of the regulation system. The MPQ4323M can be optimized for a wide range of capacitances and ESR values.

GND Connection (Pins 1, 6, and 11)

See the PCB Layout Guidelines on page 35 for more details.

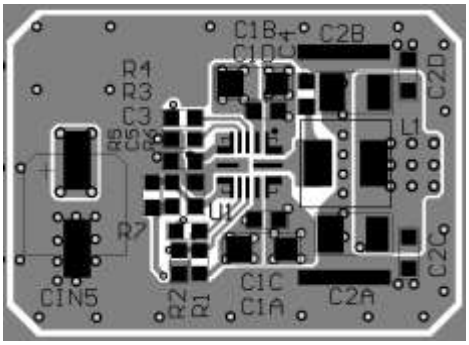
PCB Layout Guidelines (12)

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

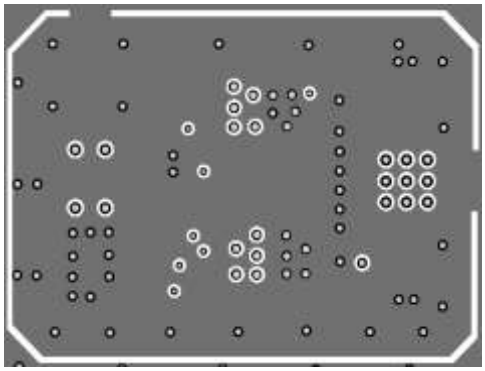
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic C_{IN}, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the FB resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

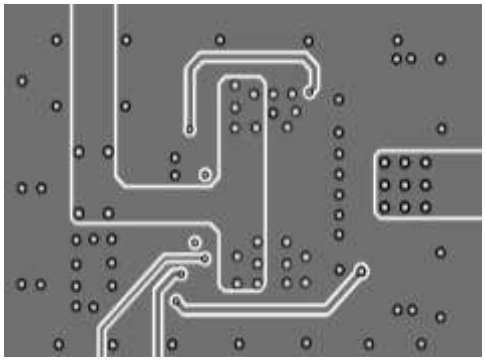
2) The recommended PCB layout is based on Figure 5 on page 30.



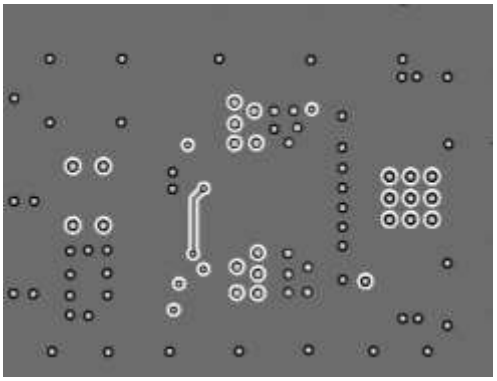
Top Layer and Top Silk



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

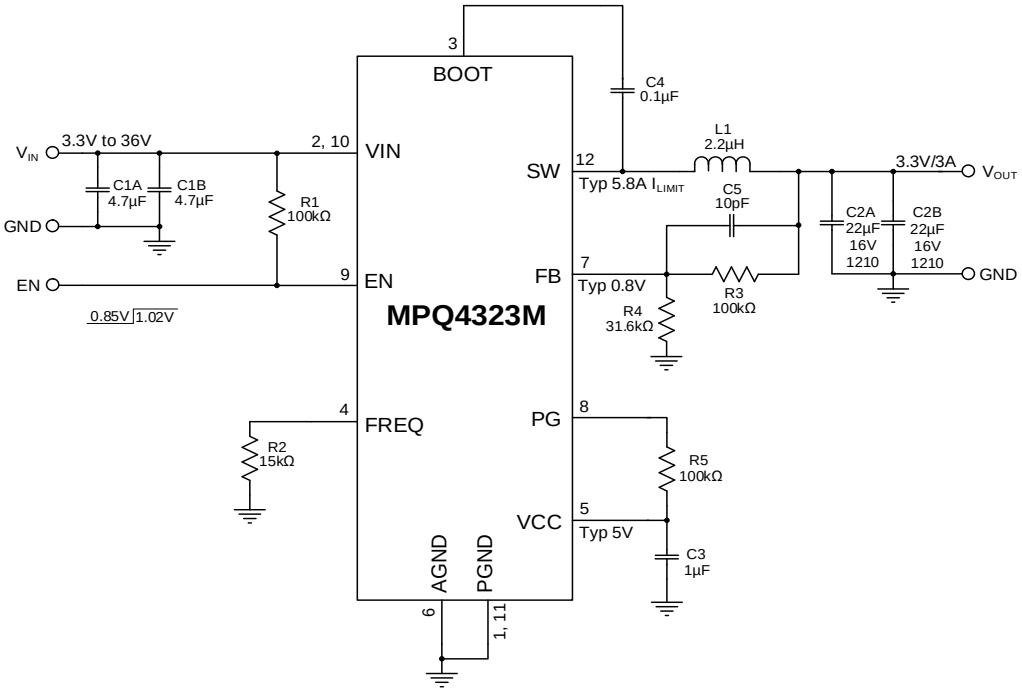


Figure 10: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

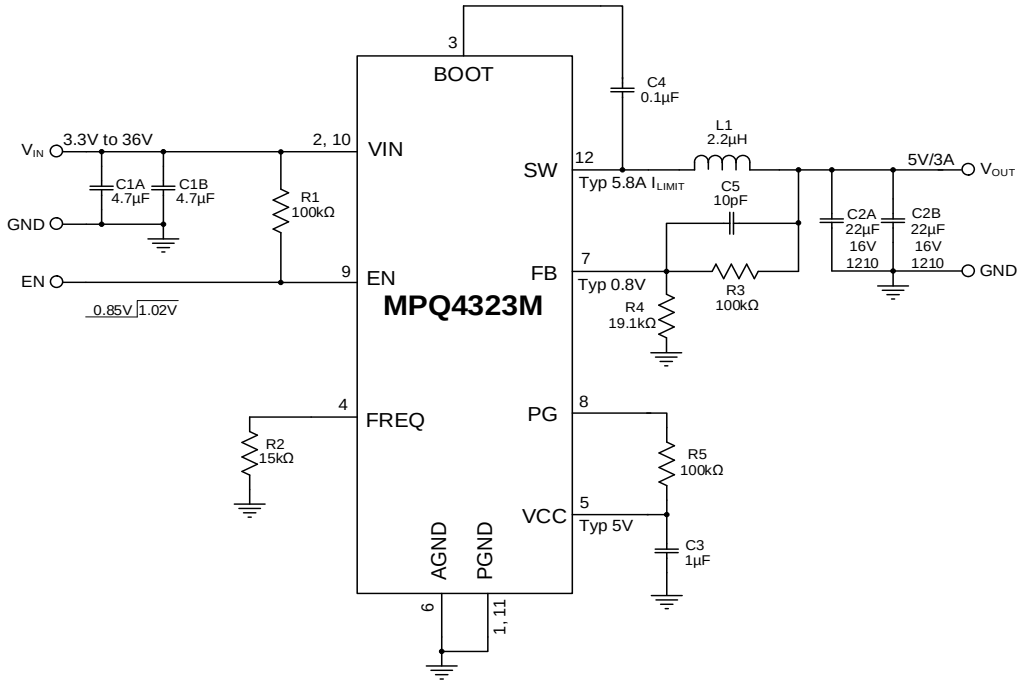


Figure 11: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

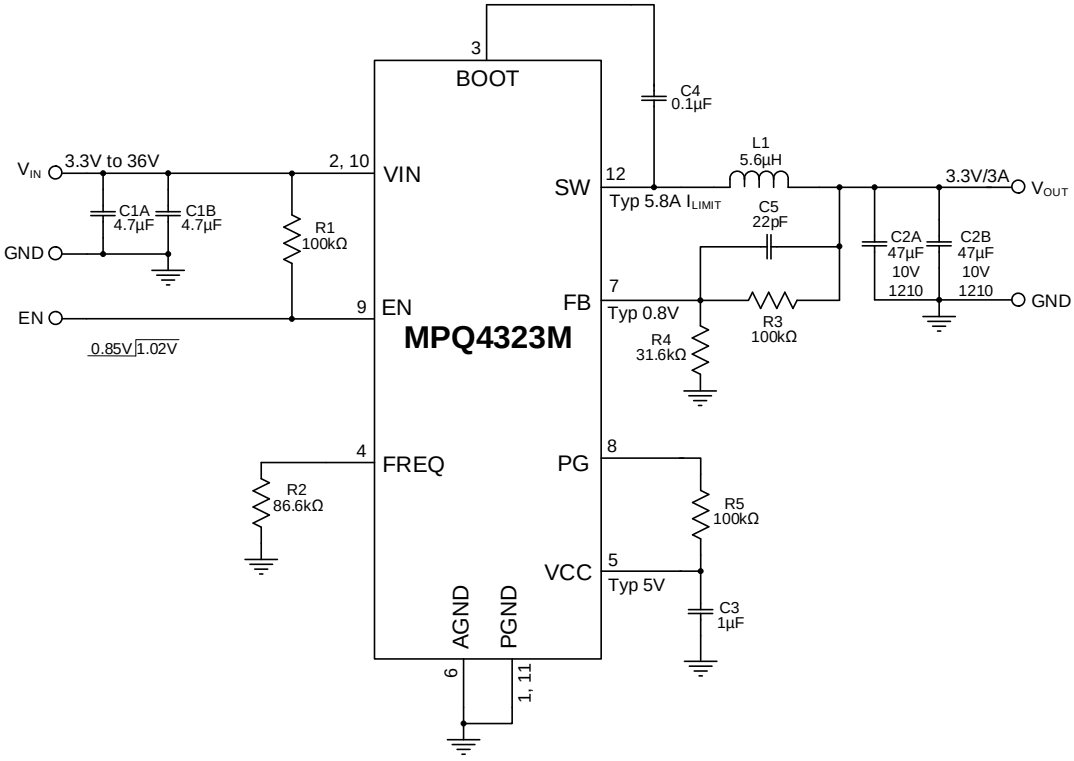


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz)

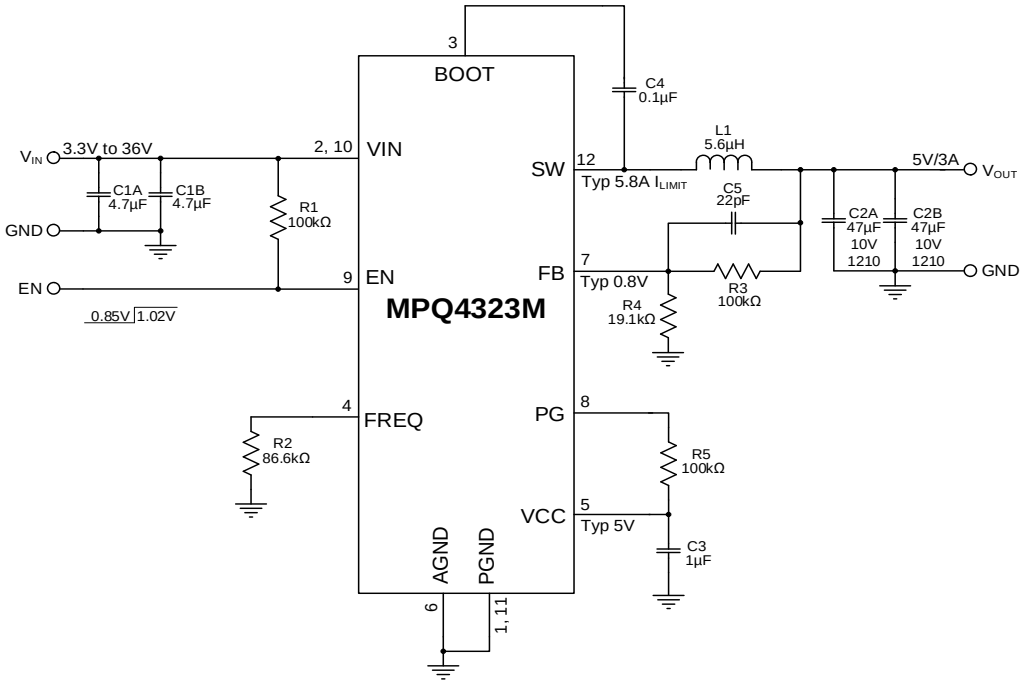


Figure 13: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

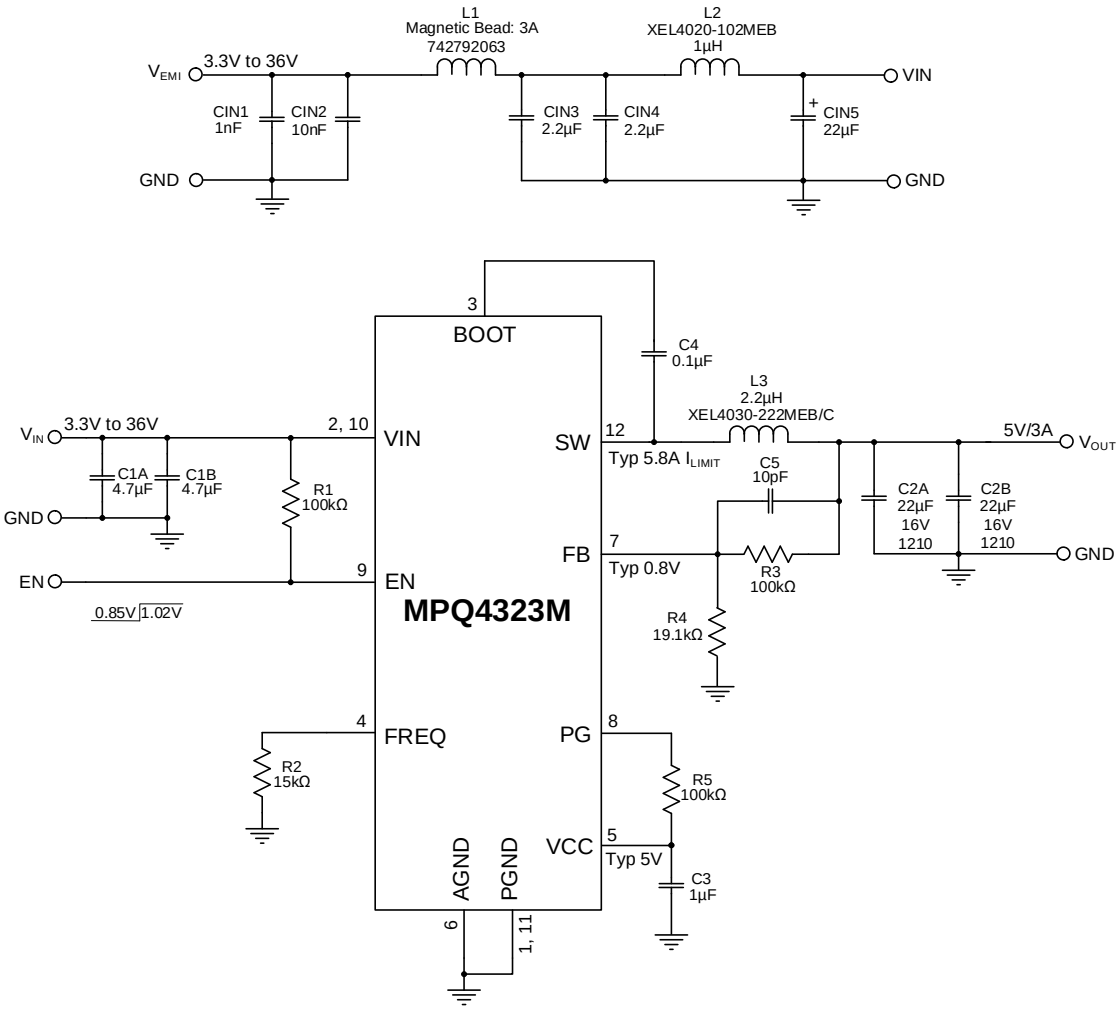


Figure 14: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

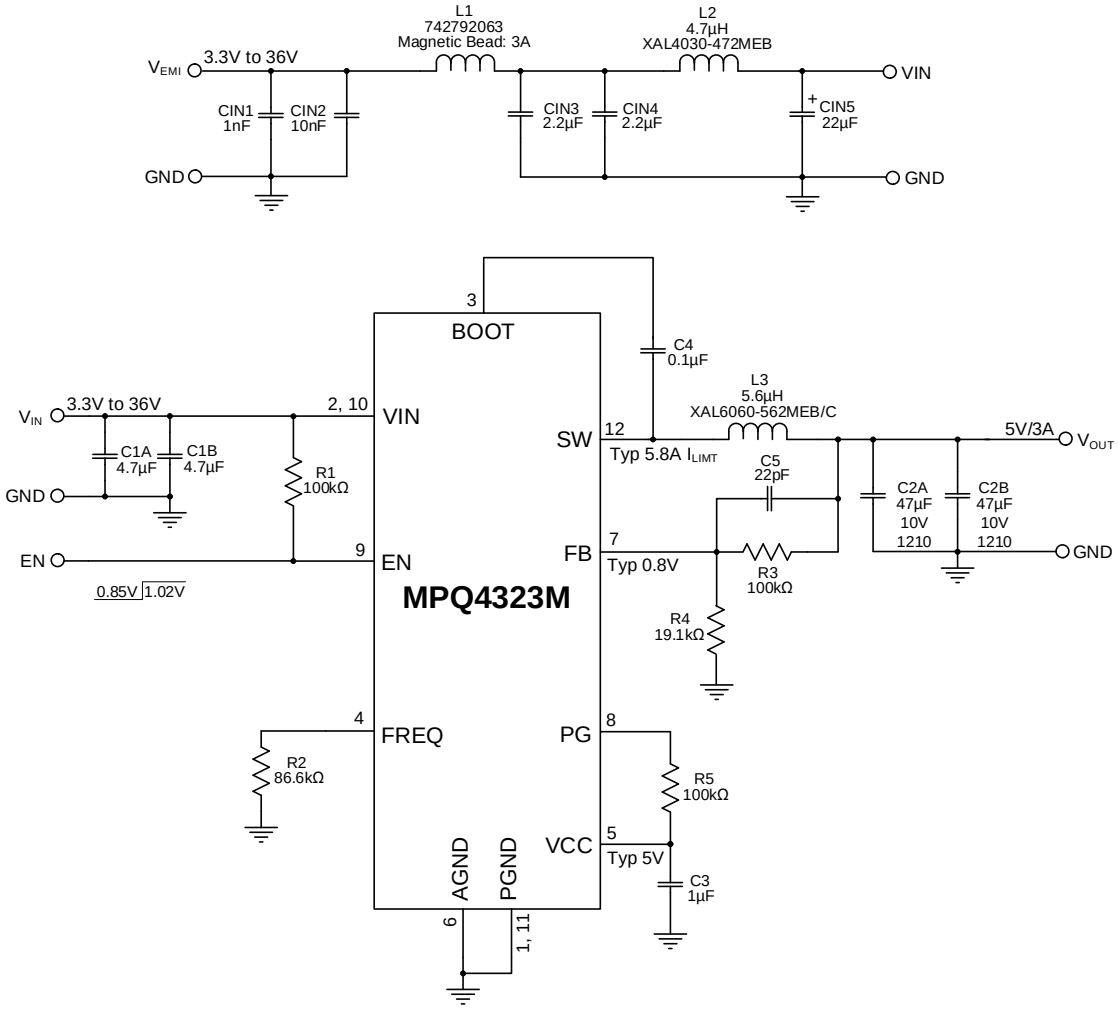
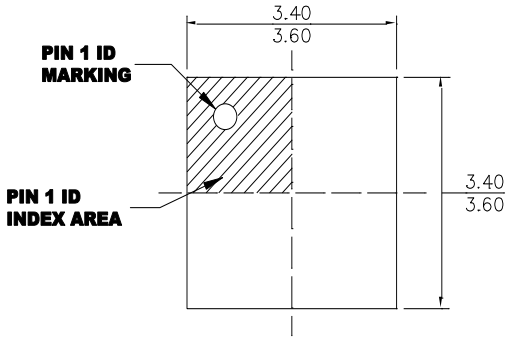


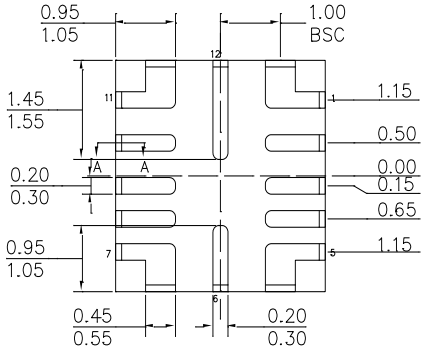
Figure 15: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz with EMI Filters)

PACKAGE INFORMATION

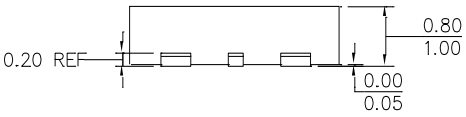
QFN-12L (3.5mmx3.5mm)
Wettable Flank



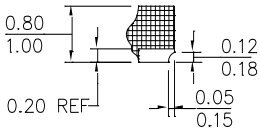
TOP VIEW



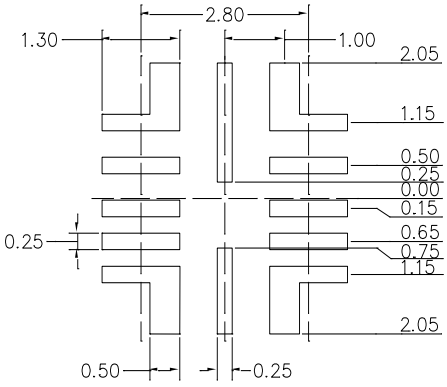
BOTTOM VIEW



SIDE VIEW



SECTION A-A

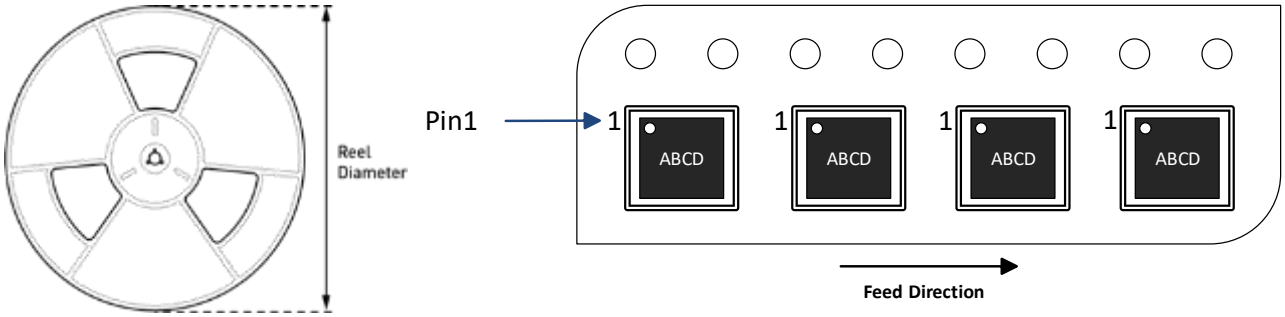


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (13)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4323MGQCE-AEC1-Z	QFN-12L (3.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) "N/A" indicates not available tubes. For 500-piece tape & reel prototype quantities, contact the factory. (Order code for 500-piece partial reel is "-P," and tape & reel dimensions remain the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/8/2022	Initial Release	-