



# PSMNR89-25YLE

N-channel 25 V, 0.98 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

14 October 2022

Product data sheet

## 1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFPAK56 package optimized for low  $R_{DSon}$  and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low  $R_{DSon}$  / low  $I^2R$  conduction losses
- LFPAK56 package for applications that demand the highest performance and reliability in a 30 mm<sup>2</sup> footprint
- Low leakage <1  $\mu$ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

## 3. Applications

- Hot swap in 12 V - 20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	25	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	270	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	224	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	0.85	0.98	mΩ
		$V_{GS} = 7\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.13	1.35	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 12\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	1.8	10	20	nC
$Q_{G(tot)}$	total gate charge		15	33	54	nC

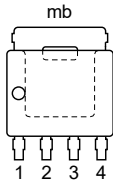
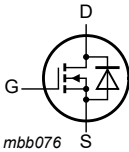
## N-channel 25 V, 0.98 mOhm, ASFET for hotswap with enhanced SOA in LPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
S	softness factor	$I_S = 25 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 12 \text{ V}$ ; $T_J = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 16</a>	-	1	-	

[1] 270 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076 S</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR89-25YLE	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR89-25YLE	E89L25Y

## 8. Limiting values

Table 5. Limiting values

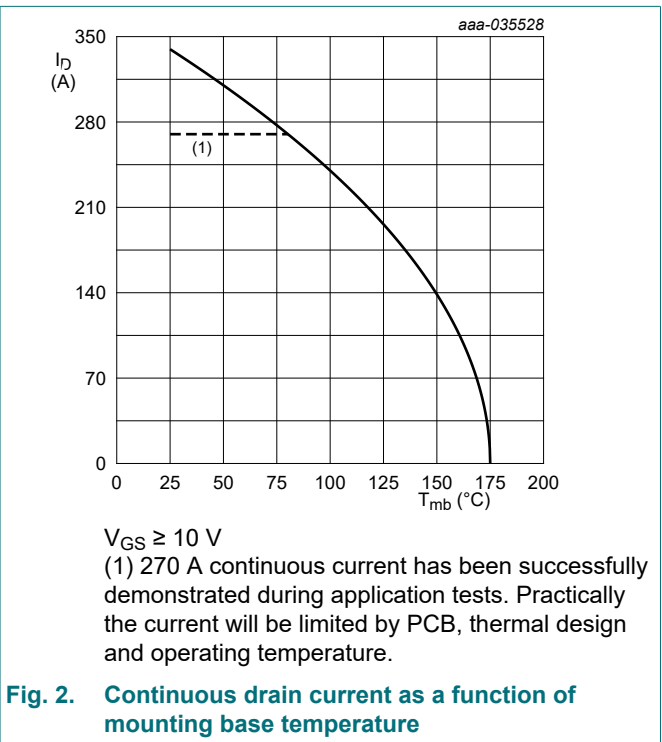
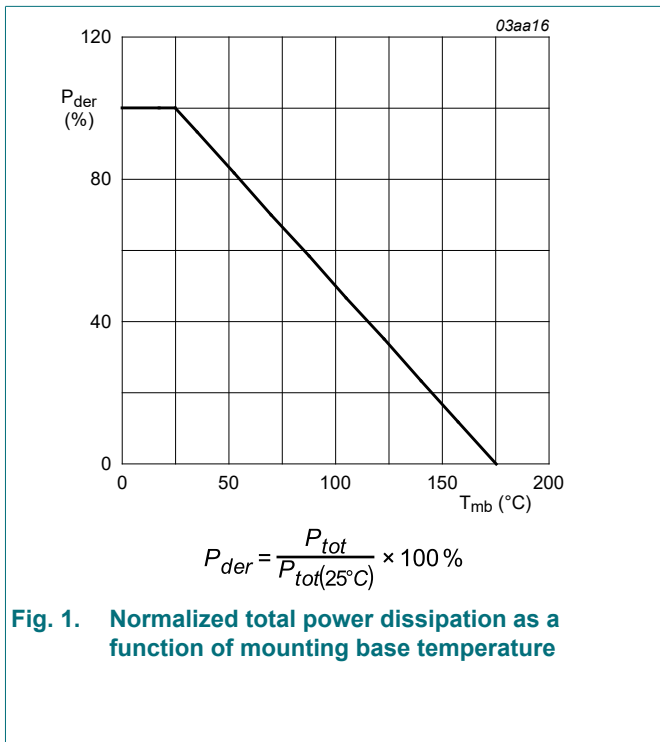
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_J = 25 \text{ }^\circ\text{C}$  unless otherwise stated.

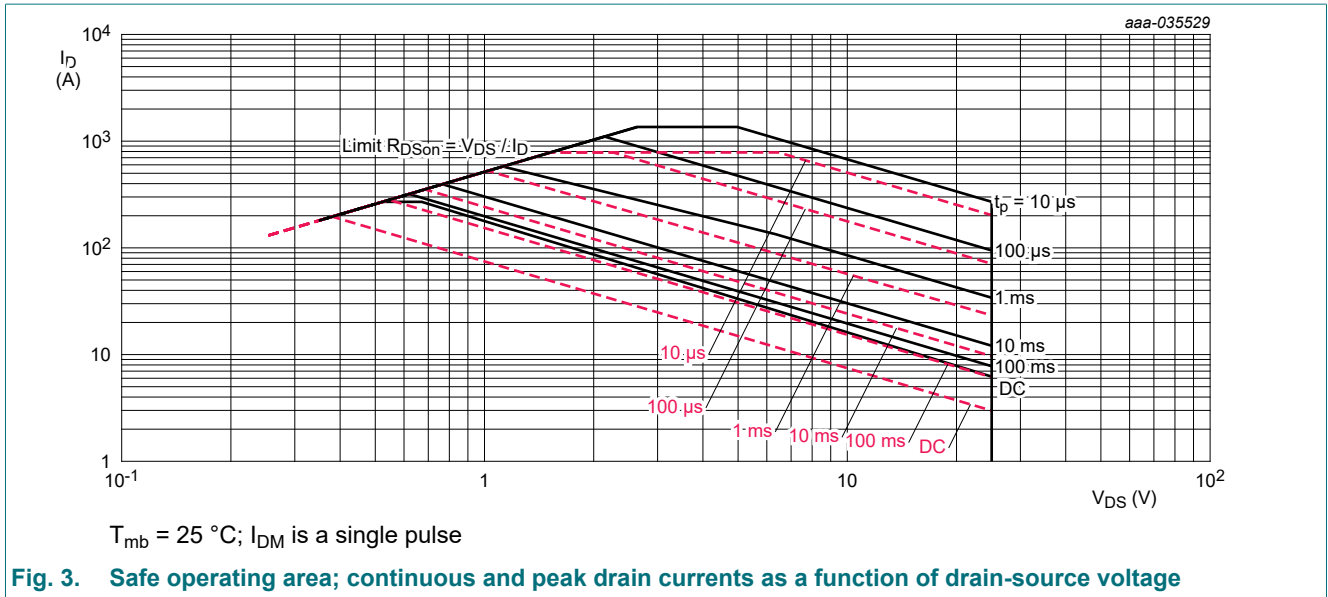
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_J \leq 175 \text{ }^\circ\text{C}$	-	25	V
$V_{DGR}$	drain-gate voltage	$25 \text{ }^\circ\text{C} \leq T_J \leq 175 \text{ }^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	224	W
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	[1]	270	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>		240	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	1359	A
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_J$	junction temperature		-55	175	$^\circ\text{C}$

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Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{slid(M)}}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{\text{mb}} = 25\text{ °C}$	-	224	A
$I_{\text{SM}}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{\text{mb}} = 25\text{ °C}$	-	1359	A
<b>Avalanche ruggedness</b>					
$E_{\text{DS(AL)S}}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$ ; $V_{\text{sup}} \leq 25\text{ V}$ ; $R_{\text{GS}} = 50\text{ }\Omega$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{j(init)}} = 25\text{ °C}$ ; unclamped; $t_p = 5\text{ ms}$	[2]	-	2.1 J
$I_{\text{AS}}$	non-repetitive avalanche current	$V_{\text{sup}} \leq 25\text{ V}$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{j(init)}} = 25\text{ °C}$ ; $R_{\text{GS}} = 50\text{ }\Omega$	[2]	-	128 A

- [1] 270 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test.

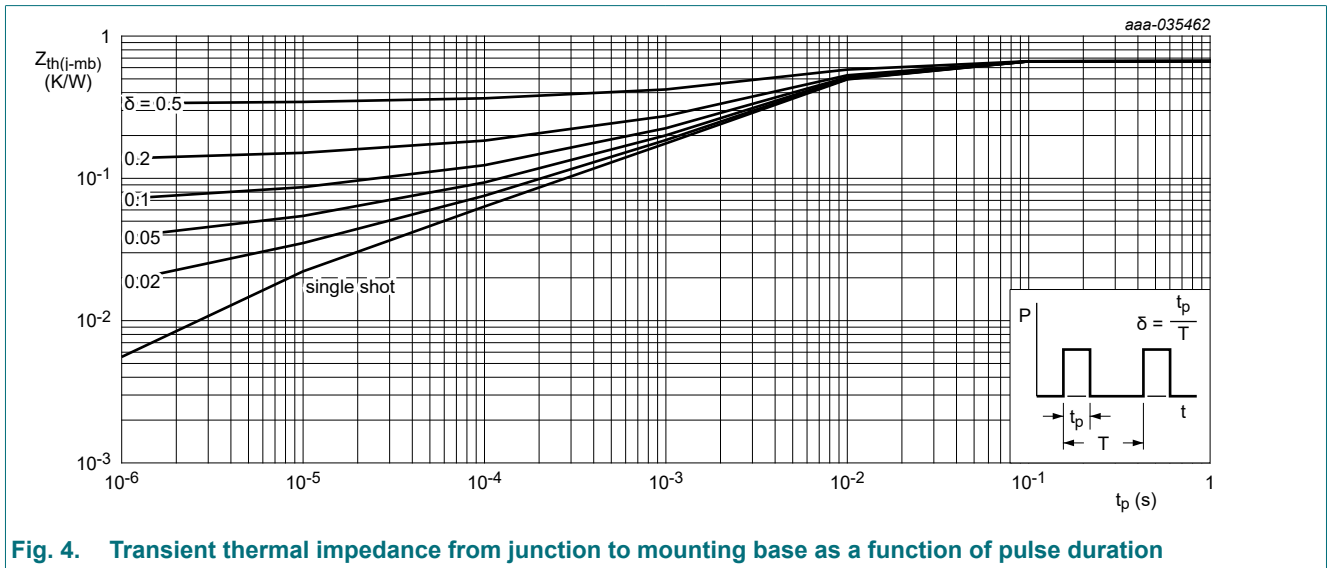


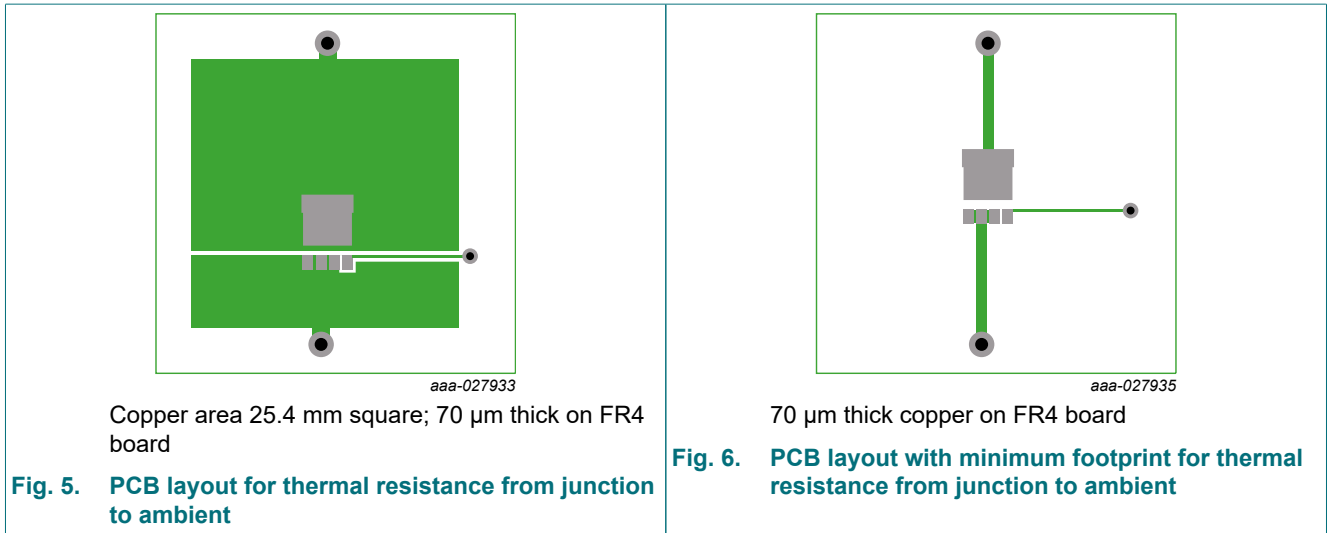


### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.4	0.67	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5 Fig. 6	-	42	-	K/W
			-	85	-	K/W





## 10. Characteristics

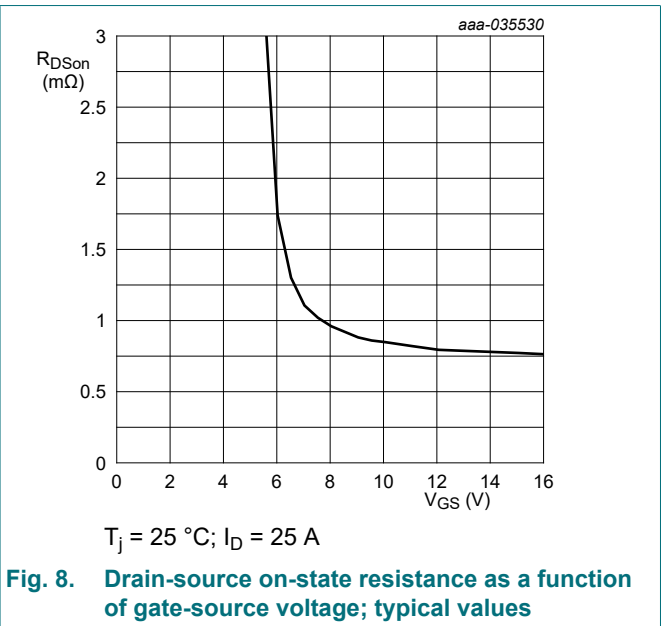
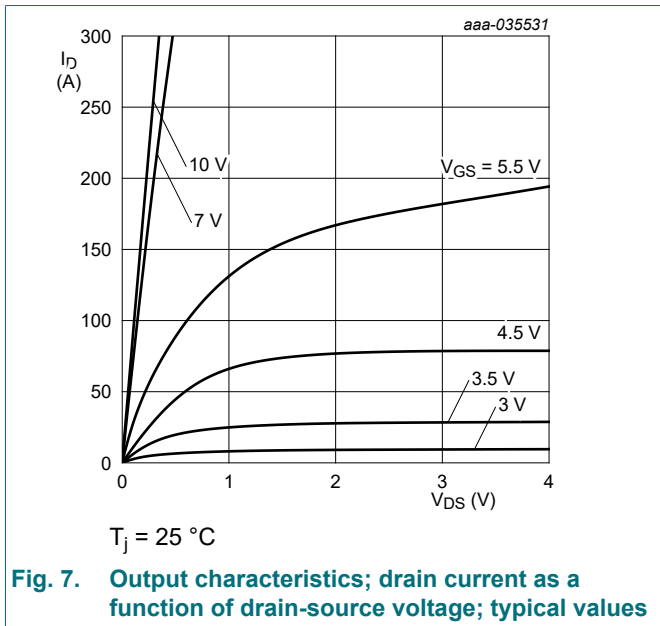
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.96	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-3.8	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	3.4	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	0.85	0.98	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	1.8	m $\Omega$
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	1.13	1.35	m $\Omega$
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	2.4	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	1.2	3.1	7.7	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	15	33	54	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	33	73	120	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C$	-	37	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	4.3	16	31	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		2	7.6	14	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		2.2	8.5	16	nC
$Q_{GD}$	gate-drain charge		1.8	10	20	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	3.5	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	2981	4968	7452	pF
$C_{oss}$	output capacitance		1261	2101	3152	pF
$C_{rss}$	reverse transfer capacitance		106	391	938	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\text{ }\Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	42	-	ns
$t_r$	rise time		-	99	-	ns
$t_{d(off)}$	turn-off delay time		-	27	-	ns
$t_f$	fall time		-	36	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	38	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.78	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	33	-	ns
$Q_r$	recovered charge		[1]	25	-	nC
$t_a$	reverse recovery rise time		-	16.4	-	ns
$t_b$	reverse recovery fall time		-	16.4	-	ns
S	softness factor		-	1	-	

[1] includes capacitive recovery



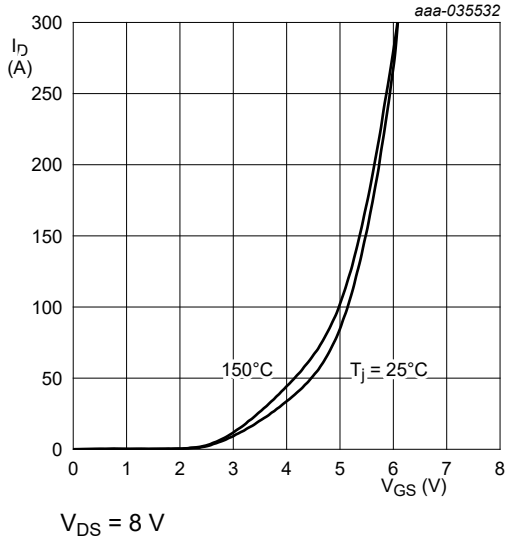


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

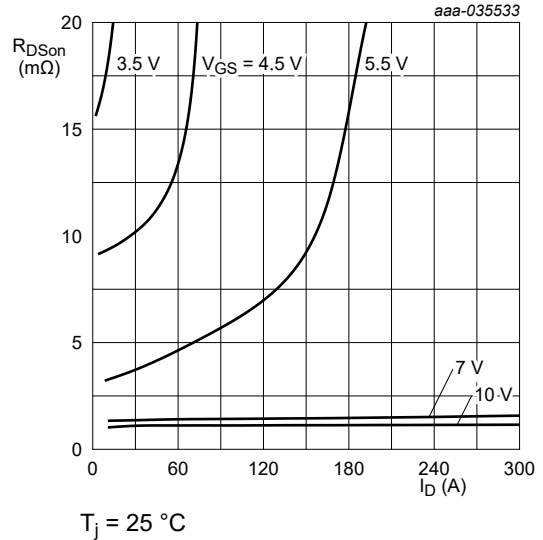


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

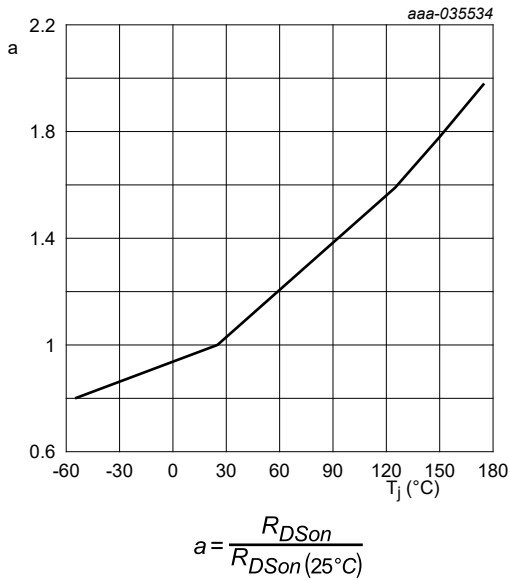


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

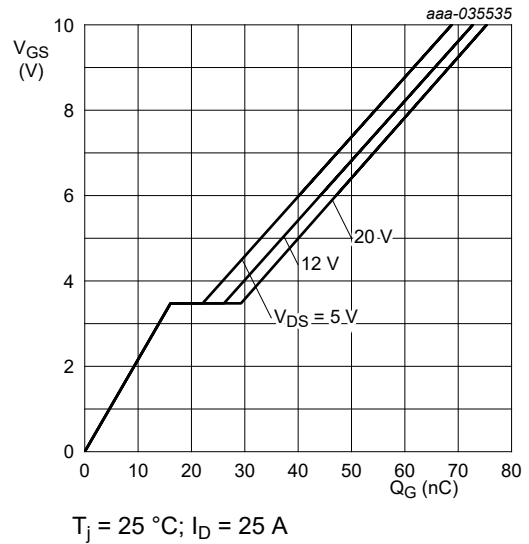


Fig. 12. Gate-source voltage as a function of gate charge; typical values

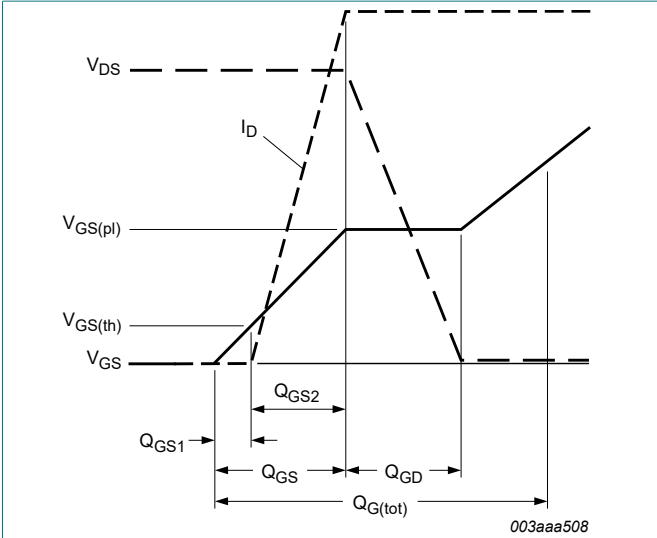


Fig. 13. Gate charge waveform definitions

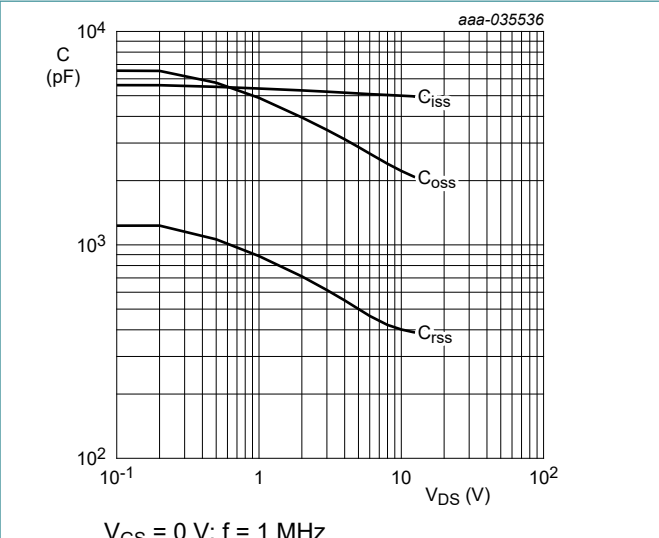


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

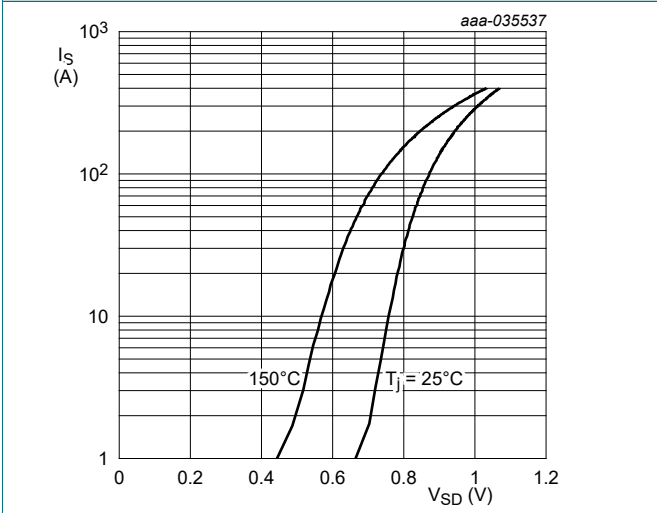


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

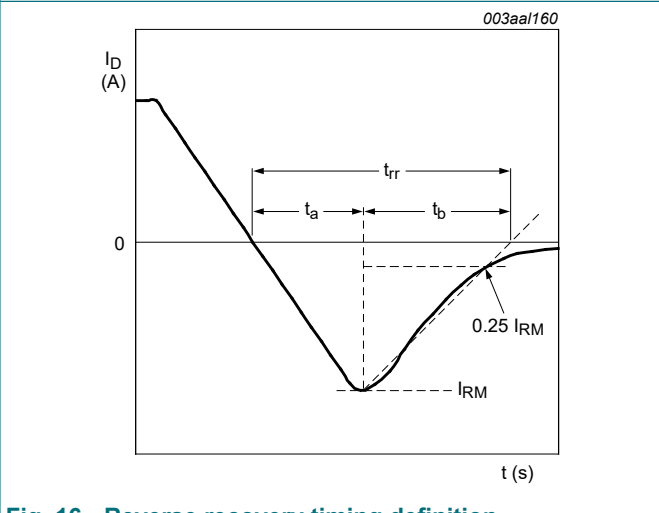


Fig. 16. Reverse recovery timing definition



### 11. Package outline

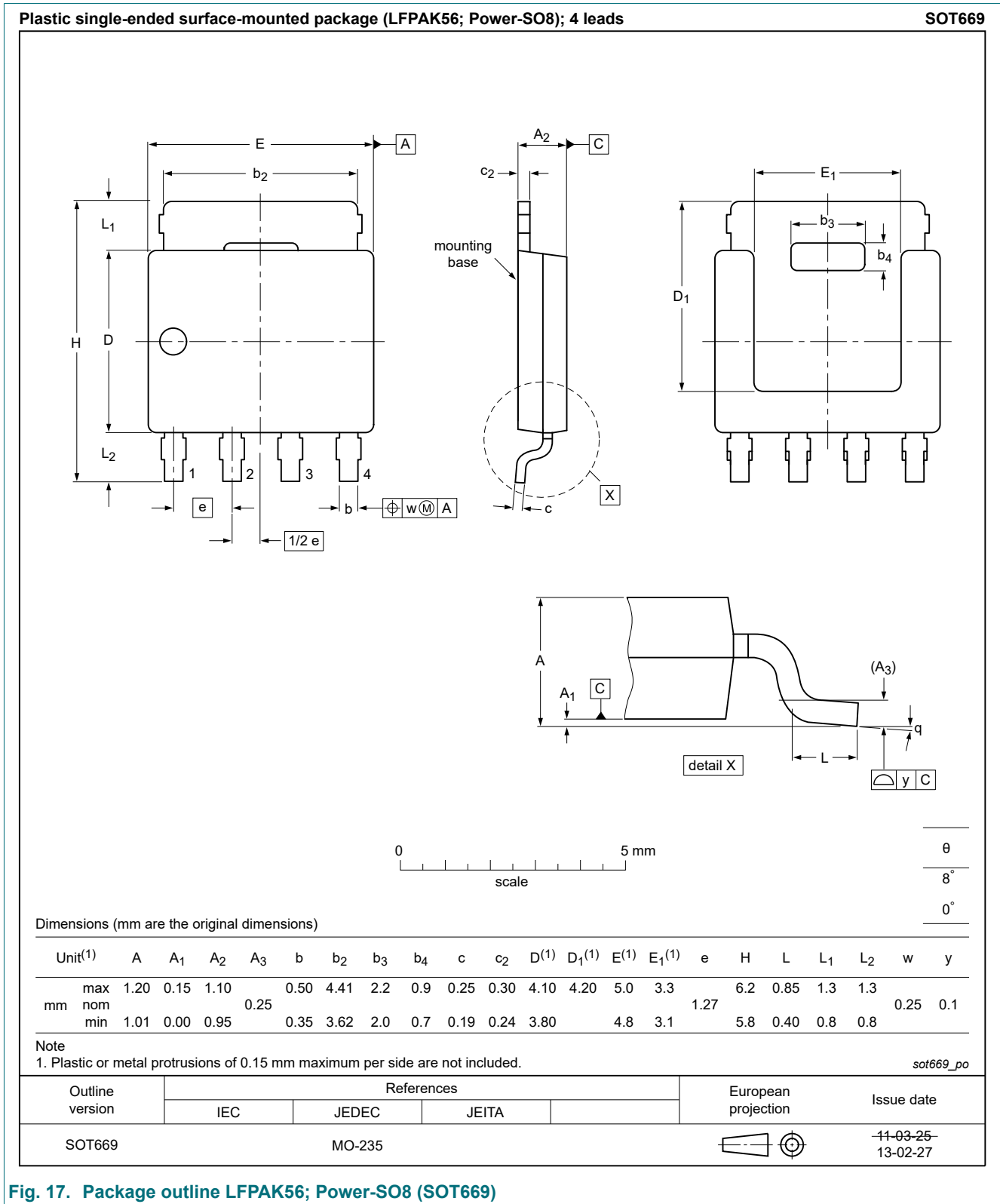
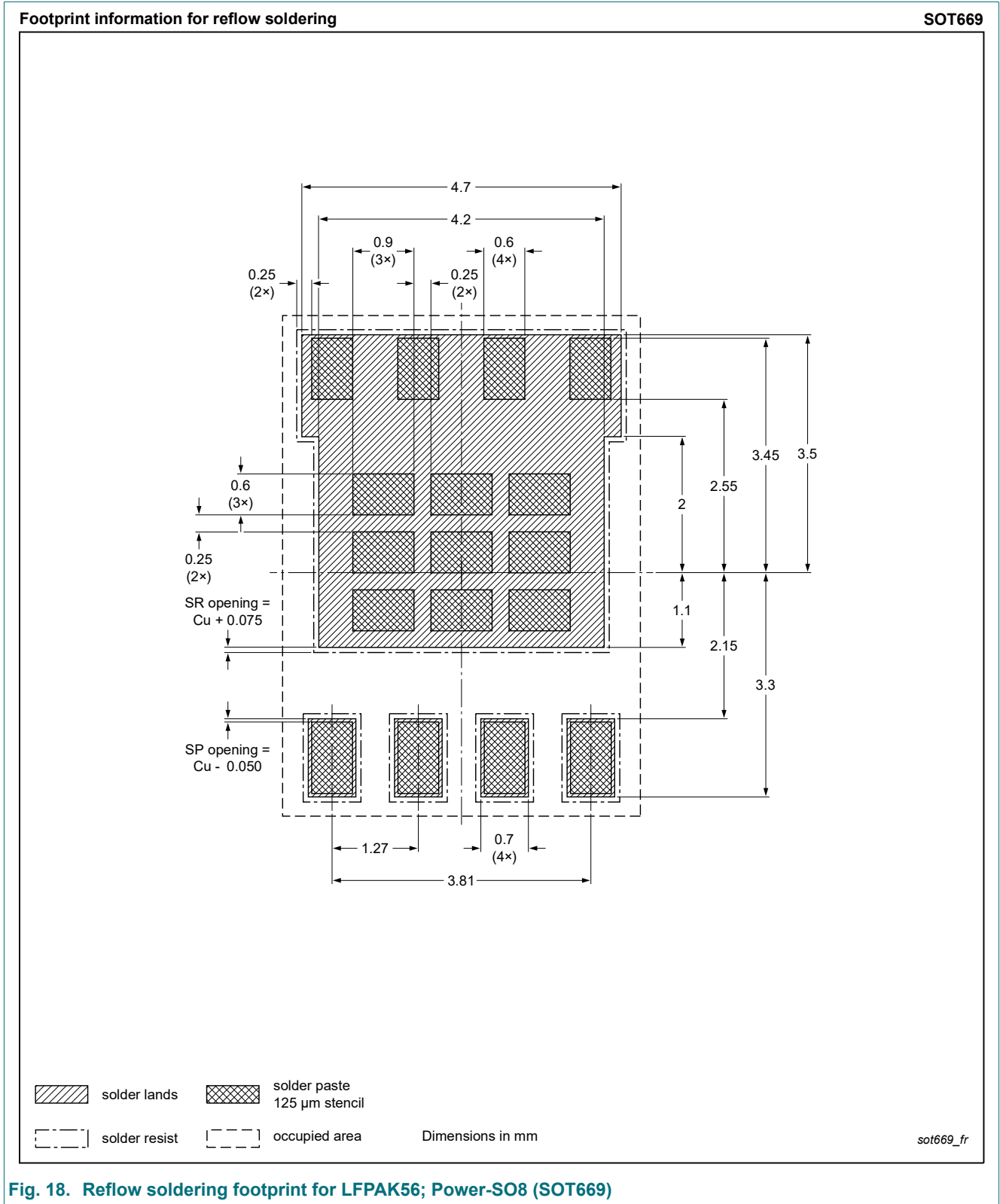


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

### 12. Soldering



**Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)**

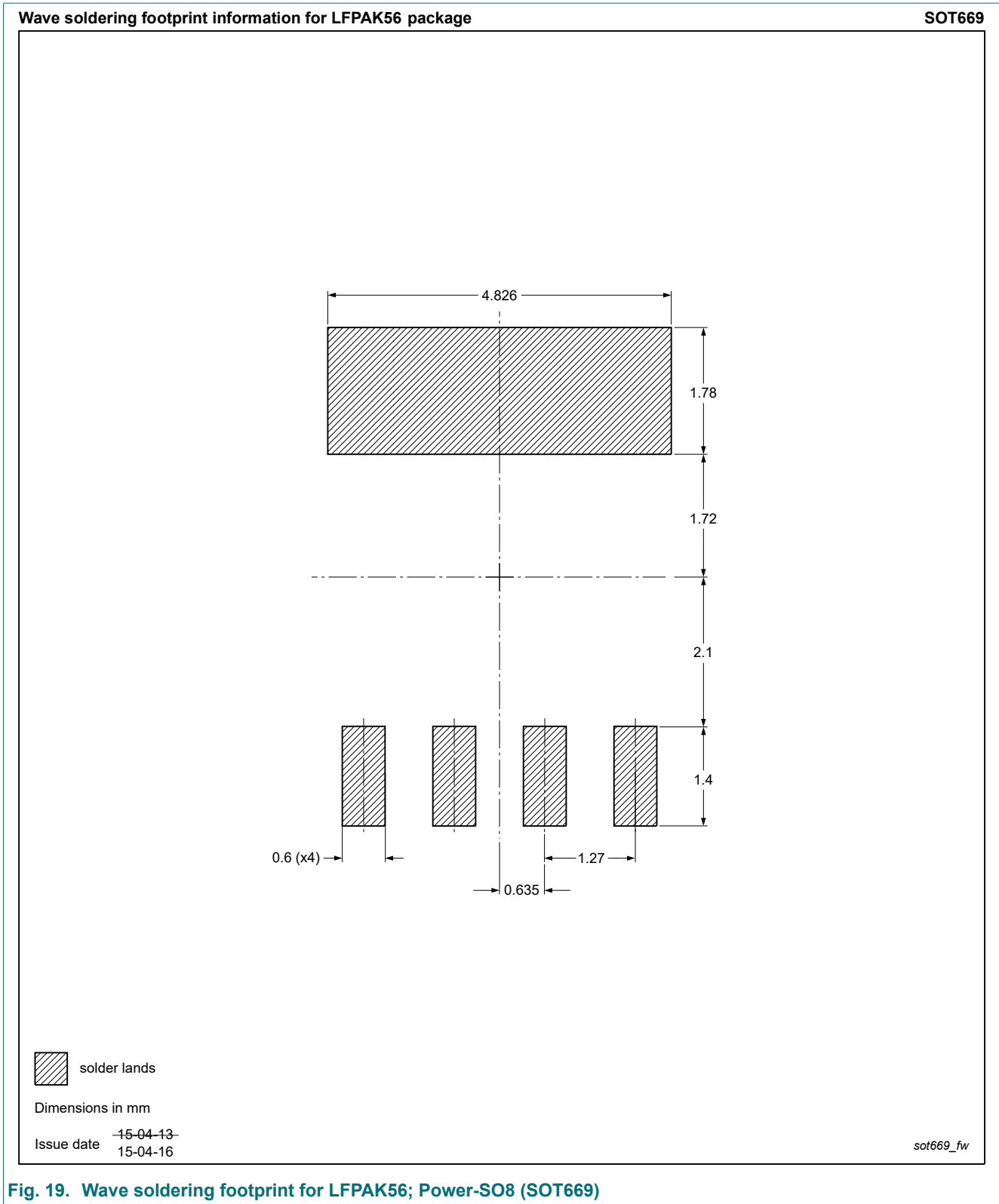


Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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