CYW9P62S1-43012EVB-01

PSoC 62S1 Wi-Fi BT Pioneer Kit Guide

Doc. # 002-28722 Rev. *B

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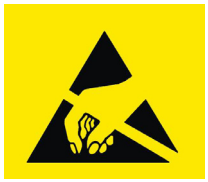
Contents

Safety and Regulatory Compliance Information

The CYW9P62S1-43012EVB-01 PSoC® 62S1 Wi-Fi BT Pioneer Kit is intended for development purposes only. Users are advised to test and evaluate this kit in an RF development environment.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required authorizations are first obtained. Contact support@cypress.com for details.

The CYW9P62S1-43012EVB-01, as shipped from the factory, has been verified to meet with the requirements of CE as a Class A product.



PSoC 62S1 Wi-Fi BT Pioneer Boards contain electrostatic discharge (ESD)- sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, which can cause a discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused PSoC 62S1 Wi-Fi BT Pioneer Boards in the protective shipping package.

End-of-Life/Product Recycling

The end-of-life cycle for this kit is five years from the date of manufacture mentioned on the back of the box. Contact your nearest recycler to discard the kit.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is unavailable, use appropriate ESD protection by wearing an anti-static wrist strap attached to a grounded metal object.

Handling Boards

PSoC 62S1 Wi-Fi BT Pioneer Board is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad, if available. Do not slide the board over any surface.

1. Introduction

Thank you for your interest in the CYW9P62S1-43012EVB-01 PSoC 62S1 Wi-Fi BT Pioneer Kit. The PSoC 62S1 Wi-Fi BT Pioneer Kit enables you to evaluate and develop your applications using the PSoC 62 Series MCU (hereafter called “PSoC 6 MCU”) and CYW43012 WICED Wi-Fi/BT combo device.

PSoC 6 MCU is Cypress’ latest, ultra-low-power PSoC specifically designed for wearables and IoT products. PSoC 6 MCU is a true programmable embedded system-on-chip, integrating a 150-MHz Arm® Cortex®-M4 as the primary application processor, a 100-MHz Arm Cortex-M0+ that supports low-power operations, up to 2 MB Flash and 1 MB SRAM, CapSense® touch-sensing, and programmable analog and digital peripherals that allow higher flexibility, in-field tuning of the design, and faster time-to-market. The PSoC 6 MCU on this kit, CY8C6247FDI-D52 has 1 MB Flash and 288 KB SRAM.

The PSoC 62S1 Wi-Fi BT Pioneer Board offers compatibility with Arduino™ shields. The board features a PSoC 6 MCU, and a CYW43012 Wi-Fi/Bluetooth combo module. Cypress CYW43012 is a 28-nm, ultra-low-power device that supports single-stream, dual-band IEEE 802.11n-compliant Wi-Fi MAC/baseband/radio and Bluetooth 5.0 BR/EDR/LE. The WLAN section supports SDIO interface to the host MCU (PSoC 6 MCU), and the Bluetooth section supports high-speed 4-wire UART interface to the host MCU. In addition, the board features an onboard programmer/debugger (KitProg3), a 512-Mbit Quad SPI NOR flash, a 4-Mbit Quad SPI F-RAM, a micro-B connector for USB device interface, a 5-segment CapSense slider, two CapSense buttons, two user LEDs, and one push button.

You can use ModusToolbox™ to develop and debug your PSoC 6 MCU projects. ModusToolbox software is a set of tools that enable you to integrate Cypress devices into your existing development methodology.

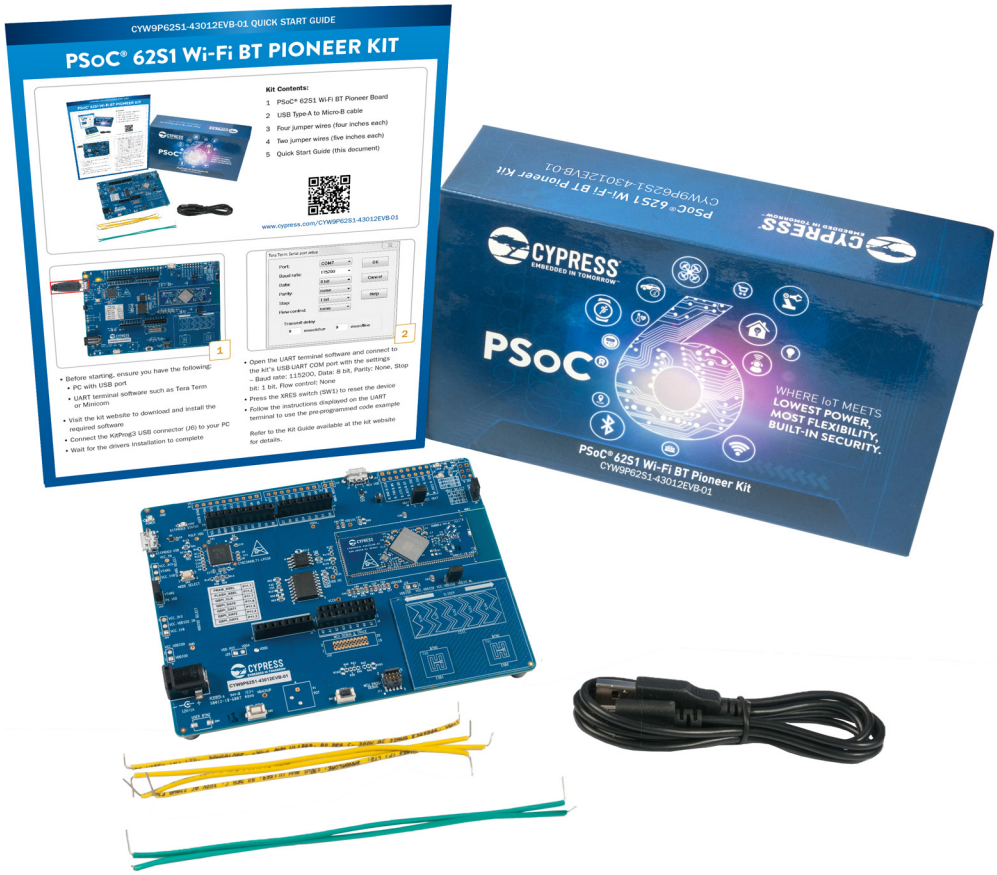
If you are new to PSoC 6 MCU and ModusToolbox IDE, refer to the application note AN228571 - Getting Started with PSoC 6 MCU on ModusToolbox to help you familiarize with the PSoC 6 MCU and help you create your own design using the ModusToolbox IDE.

1.1 Kit Contents

The CYW9P62S1-43012EVB-01 PSoC 62S1 Wi-Fi BT Pioneer Kit has the following contents, as shown in Figure 1-1.

- PSoC 62S1 Wi-Fi BT Pioneer Board
- USB Type-A to Micro-B cable
- Four jumper wires (4 inches each)
- Two jumper wires (5 inches each)
- Quick Start Guide

Figure 1-1. Kit Contents



Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/support.

1.2 Getting Started

This guide will help you get acquainted with the PSoC 62S1 Wi-Fi BT Pioneer Kit:

- The Kit Operation chapter on page 11 describes the major features of the PSoC 62S1 Wi-Fi BT Pioneer Kit and functionalities such as programming, debugging, and the USB-UART and USB-I^2C bridges.
- The Hardware chapter on page 26 provides a detailed hardware description, methods to use the onboard NOR flash, kit schematics, and the bill of materials (BOM).
- Application development using PSoC 62S1 Wi-Fi BT Pioneer Kit is supported in various development ecosystems such as ModusToolbox and Mbed OS. For the latest software support for this development kit including the different development ecosystems, refer to the kit webpage.
  - ModusToolbox software is a free development ecosystem that includes the ModusToolbox IDE. Using ModusToolbox IDE, you can enable and configure device resources, middleware libraries, and program and debug the device. You can download the software from the ModusToolbox home page. See the ModusToolbox User Guide for additional information.
  - Mbed OS: Visit Cypress' Mbed OS page on instructions to develop applications on Cypress' target board on the Mbed OS platform.
- There is a wide range of code examples to evaluate the PSoC 62S1 Wi-Fi BT Pioneer Board. These examples help you familiarize yourself with the PSoC 6 MCU and create your own design. These examples are available in various development ecosystems such as ModusToolbox IDE and Mbed OS. Visit Cypress' code example page to access examples for the following development ecosystems:
  - ModusToolbox based examples
  - Mbed OS based examples

1.3 Board Overview

The PSoC 62S1 Wi-Fi BT Pioneer Board has the following features:

- CYW9P62S1-43012CAR-01 carrier module that contains WM-BAC-CYW-50 System in Package (SiP) module by Universal Global Scientific Industrial (USI), which has
  - PSoC 6 MCU (CY8C6247FDI-D52)
  - CYW43012 module which supports 2.4/5.0-GHz WLAN and Bluetooth functionality
- 512-Mbit external Quad SPI NOR Flash that provides a fast, expandable memory for data and code
- 4-Mbit Quad SPI ferroelectric random-access memory (F-RAM)
- KitProg3 onboard SWD programmer/debugger with USB-UART and USB-I2C bridge functionality
- CapSense touch-sensing slider (5 elements), two buttons, based on self-capacitance (CSD) and mutual-capacitance (CSX) sensing
- A micro-B connector for USB device interface for PSoC 6 MCU
- 1.8 V operation of PSoC 6 MCU is supported
- Two user LEDs, one user button, and a reset button for PSoC 6 MCU
- One Mode selection button and one Status LED for KitProg3

1.4 Additional Learning Resources

Cypress provides a wealth of data at www.cypress.com/psoc6 to help you to select the right PSoC device for your design and to help you to quickly and effectively integrate the device into your design.

1.5 Technical Support

For assistance, visit Cypress Support or contact customer support at +1(800) 541-4736 Ext. 3 (in the USA) or +1 (408) 943-2600 Ext. 3 (International).

You can also use the following support resources if you need quick assistance:

- Self-help (Technical Documents)
- Local Sales Office Locations

1.6 Documentation Conventions

Table 1-1. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Creator User Guide*.
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: $2 + 2 = 4$
Text in gray boxes	Describes cautions or unique functionality of the product.

1.7 Acronyms

Table 1-2. Acronyms Used in this Document

Acronym	Definition
ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
BOM	Bill of Materials
BT	Bluetooth
CINT	Integration Capacitor
CMOD	Modulator Capacitor
CPU	Central Processing Unit
CSD	CapSense Sigma Delta
CSX	CapSense Crosspoint
DC	Direct Current
Del-Sig	Delta-Sigma

Table 1-2. Acronyms Used in this Document *(continued)*

Acronym	Definition
DMA	Direct Memory Access
ECO	External Crystal Oscillator
ESD	Electrostatic Discharge
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
IDE	Integrated Development Environment
IoT	Internet of Things
LED	Light-emitting Diode
LPO	Low Power Oscillator
MAC	Medium Access Control
OOB	Out-of Box
PC	Personal Computer
PDM	Pulse Density Modulation
PSoC	Programmable System-on-Chip
PWM	Pulse Width Modulation
QSPI	Quad Serial Peripheral Interface
SAR	Successive Approximation Register
SDIO	Secure Digital Input Output
SiP	System in Package
SPI	Serial Peripheral Interface
SRAM	Serial Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WCO	Watch Crystal Oscillator
WLAN	Wireless Local Area Network

2. Kit Operation

This chapter introduces you to various features of the PSoC 62S1 Wi-Fi BT Pioneer Board, including the theory of operation and the onboard KitProg3 programming and debugging functionality, USB-UART and USB-I2C bridges.

2.1 Board Details

The PSoC 62S1 Wi-Fi BT Pioneer Board is built around a PSoC 6 MCU. Figure 2-1 shows the block diagram of the PSoC 6 MCU device used on the board. For details of device features, see the device datasheet.

Figure 2-1. PSoC 6 MCU Block Diagram

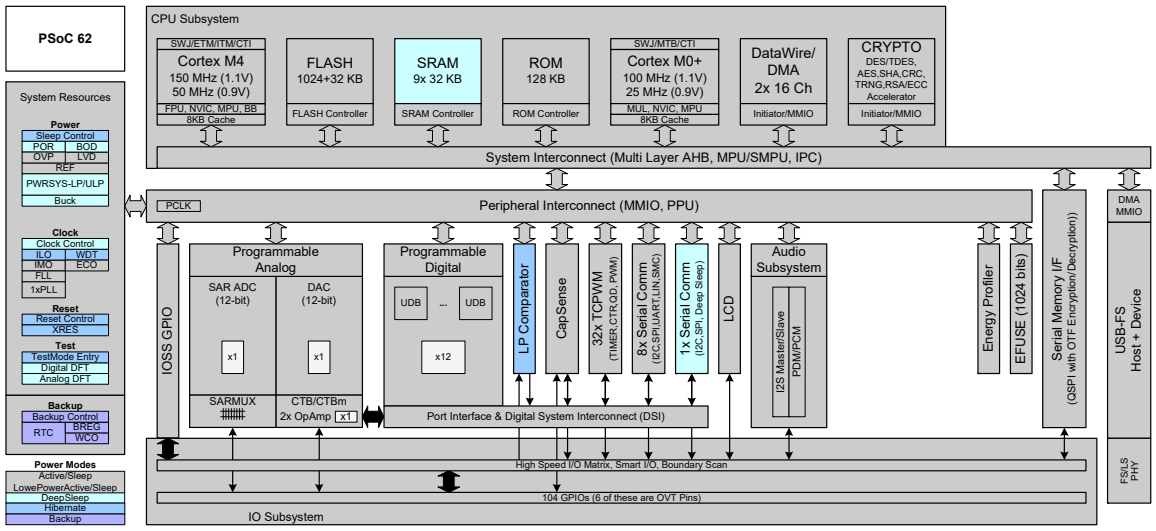


Figure 2-2 shows the block diagram of the CYW9-BASE-01 Pioneer Board (modified for CYW9P62S1-43012EVB-01).

Figure 2-3 shows the block diagram of the CYW9P62S1-43012CAR-01 Carrier Module.

Figure 2-2. Block Diagram of Pioneer Board

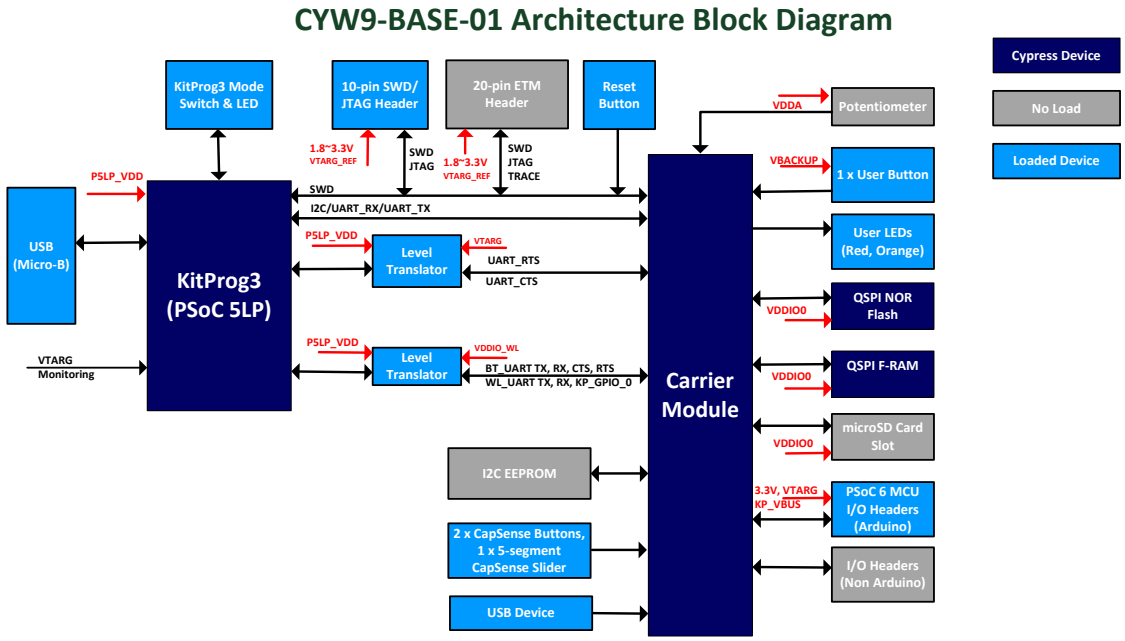


Figure 2-3. Block Diagram of CYW9P62S1-43012CAR-01 Carrier Module

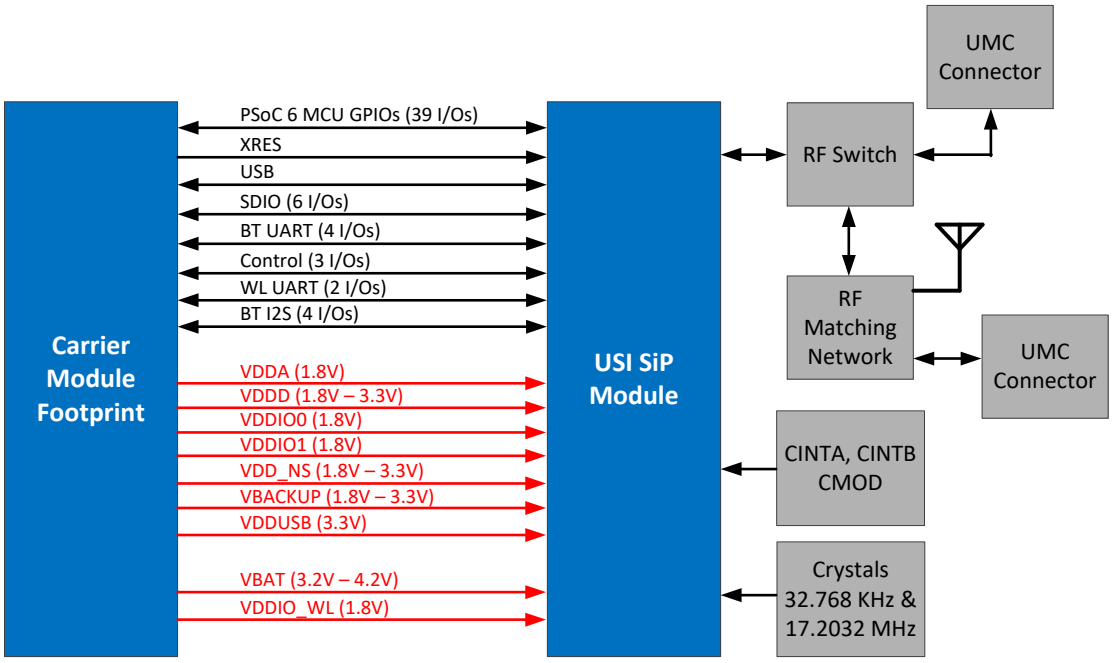


Figure 2-4 shows the pinout of the PSoC 62S1 Wi-Fi BT Pioneer Board.

Figure 2-4. PSoC 62S1 Wi-Fi BT Pioneer Board Pinout

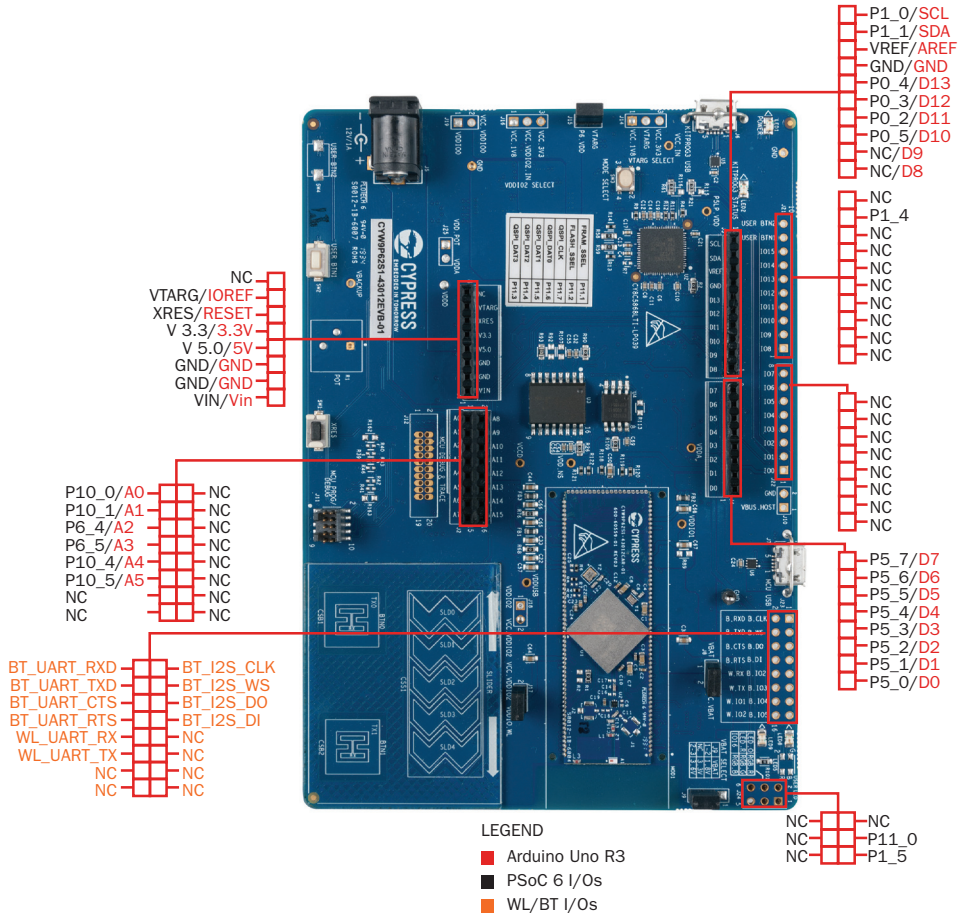


Table 2-1. PSoC 62S1 Wi-Fi BT Pioneer Board Pinout

Pin	Primary On-board Function	Secondary On-board Function	Connection details
PSoC 6 MCU Pins			
XRES	Hardware Reset	–	–
P0[2]	Arduino D11 (J3.4)	–	–
P0[3]	Arduino D12 (J3.5)	–	–
P0[4]	Arduino D13 (J3.6)	–	–
P0[5]	Arduino D10 (J3.3)	–	–
P1[0]	I2C SCL	Arduino (J3.10)	Remove R58 to disconnect from KitProg3.
P1[1]	I2C SDA	Arduino (J3.9)	Remove R59 to disconnect from KitProg3.
P1[4]	User button with Hibernate wakeup capability	GPIO on non-Arduino header (J21.9)	–

Table 2-1. PSoC 62S1 Wi-Fi BT Pioneer Board Pinout *(continued)*

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P1[5]	Orange user LED (LED8)	GPIO on non-Arduino header IO7 (J24.2)	–
P5[0]	UART_RX	Arduino D0 (J4.1)	Remove R21 to disconnect from KitProg3.
P5[1]	UART_TX	Arduino D1 (J4.2)	Remove R61 to disconnect from KitProg3.
P5[2]	UART_RTS	Arduino D2 (J4.3)	Remove R19 to disconnect from KitProg3.
P5[3]	UART_CTS	Arduino D3 (J4.4)	Remove R18 to disconnect from KitProg3.
P5[4]	Arduino D4 (J4.5)	–	–
P5[5]	Arduino D5 (J4.6)	–	–
P5[6]	Arduino D6 (J4.7)	–	–
P5[7]	Arduino D7 (J4.8)	–	–
P6[4]	Arduino A2 (J2.5)	PSoC 6 MCU JTAG TDO/SWD SWO	Remove R4 to disconnect from Arduion A2. Populate R3 to connect to PSoC 6 MCU JTAG TDO/SWD SWO.
P6[5]	Arduino A3 (J2.7)	PSoC 6 MCU JTAG TDI	Remove R8 to disconnect from Arduino A3. Populate R7 to connect to PSoC 6 MCU JTAG TDI.
P6[6]	PSoC 6 MCU JTAG TMS/SWD SWDIO	–	–
P6[7]	PSoC 6 MCU JTAG TCK/SWD SWCLK	–	–
P7[0]	CapSense Button1 TX	GPIO on non-Arduino header IO9 (J21.2)	Remove R25 to disconnect from CapSense. Populate R143 to connect to GPIO on non-Arduino header.
P7[1]	CapSense CINTA	–	–
P7[2]	CapSense CINTB	–	–
P7[7]	CapSense CMOD	–	–
P9[0]	CapSense Slider0 RX	GPIO on non-Arduino header IO10 (J21.3)	Remove R28 to disconnect from CapSense. Populate R142 to connect to GPIO on non-Arduino header.
P9[1]	CapSense Slider1 RX	GPIO on non-Arduino header IO11 (J21.4)	Remove R29 to disconnect from CapSense. Populate R152 to connect to GPIO on non-Arduino header.
P9[2]	CapSense Slider2 RX	GPIO on non-Arduino header IO12 (J21.5)	Remove R30 to disconnect from CapSense. Populate R153 to connect to GPIO on non-Arduino header.
P9[3]	CapSense Slider3 RX	GPIO on non-Arduino header IO13 (J21.6)	Remove R31 to disconnect from CapSense. Populate R151 to connect to GPIO on non-Arduino header.
P9[4]	CapSense Slider4 RX	GPIO on non-Arduino header IO14 (J21.7)	Remove R32 to disconnect from CapSense. Populate R149 to connect to GPIO on non-Arduino header.

Table 2-1. PSoC 62S1 Wi-Fi BT Pioneer Board Pinout *(continued)*

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P9[7]	CapSense Button0 TX	GPIO on non-Arduino header IO8 (J21.1)	Remove R24 to disconnect from CapSense. Populate R144 to connect to GPIO on non-Arduino header.
P10[0]	Arduino A0 (J2.1)	–	–
P10[1]	Arduino A1 (J2.3)	–	–
P10[4]	Arduino A4 (J2.9)	–	–
P10[5]	Arduino A5 (J2.11)	–	–
P11[0]	Red user LED (LED9)	GPIO on non-Arduino header (J24.4)	–
P11[1]	QSPI F-RAM CS	–	–
P11[2]	QSPI Flash CS	–	–
P11[3:6]	QSPI Flash IO[3:0]	–	–
P11[7]	QSPI Flash CLK	–	–
P12[6]	ECO Crystal XIN	–	–
P12[7]	ECO Crystal XOUT	–	–
CYW43012 Pins			
BT_UART_TXD	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_RXD	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_CTS	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_UART_RTS	UART interface with Host MCU (PSoC 6 MCU)	–	–
BT_I2S_CLK	I2S serial clock	–	–
BT_I2S_WS	I2S serial word select	–	–
BT_I2S_DO	I2S serial data out	–	–
BT_I2S_DI	I2S serial data in	–	–
WL_UART_RX	Wi-Fi debug UART Rx Pin	–	–
WL_UART_TX	Wi-Fi debug UART Tx Pin	–	–

The CYW9P62S1-43012EVB-01 PSoC 62S1 Wi-Fi BT Pioneer Kit comes with the PSoC 62S1 Wi-Fi BT Pioneer Board. Figure 2-5 and Figure 2-6 show the markup of the Pioneer Board.

Figure 2-5. PSoC 62S1 Wi-Fi BT Pioneer Board - Top View

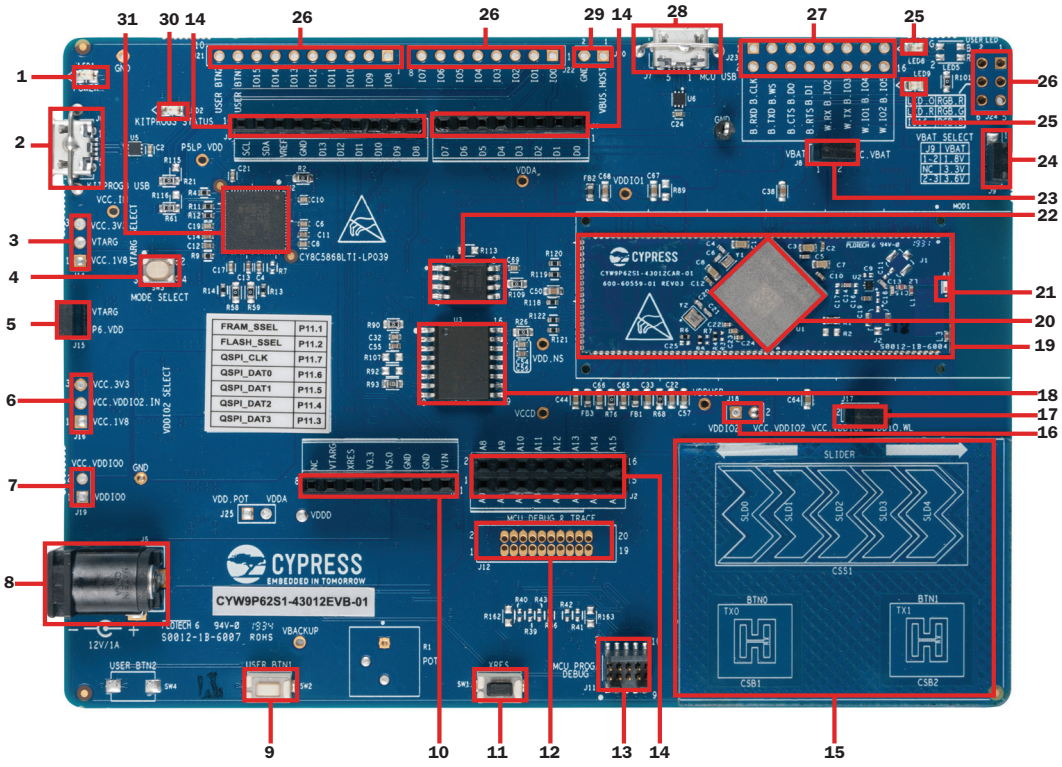
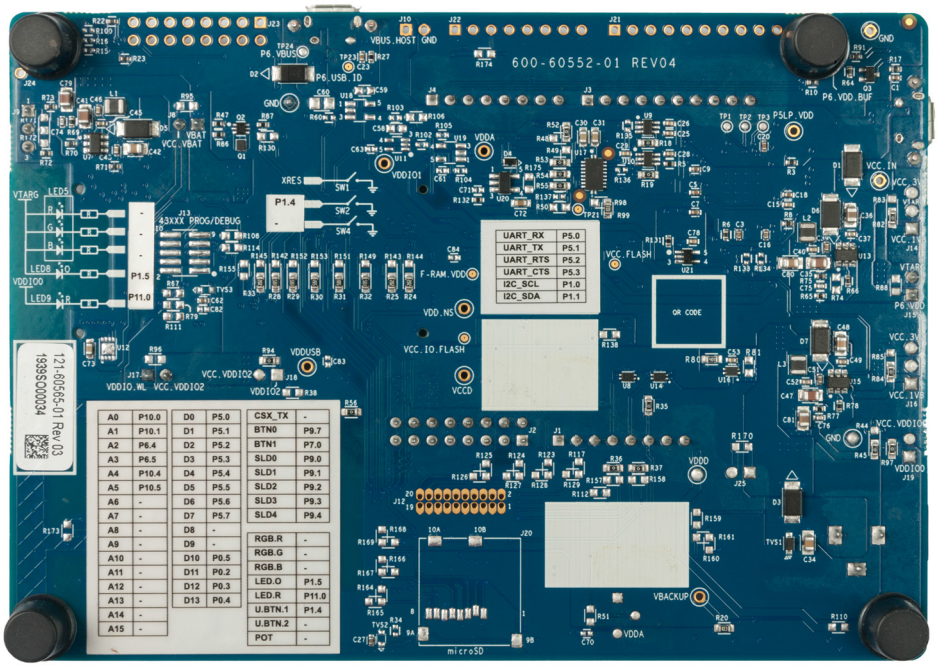


Figure 2-6. PSoC 62S1 Wi-Fi BT Pioneer Board - Bottom View



The PSoC 62S1 Wi-Fi BT Pioneer Board has the following components:

1. **Power LED (LED1):** This Yellow LED indicates the status of power supplied to board.
2. **KitProg3 USB connector (J6):** The USB cable provided along with the PSoC 62S1 Wi-Fi BT Pioneer Board connects between this USB connector and the PC to use the KitProg3 onboard programmer and debugger and to provide power to the board.
3. **PSoC 6 MCU VDD power selection jumper (J14):** This jumper is used to select the PSoC 6 MCU VDD supply voltage between 1.8 V and 3.3 V. J14 is not loaded for this kit and R82 is loaded, due to which only 1.8 V operation is supported.
4. **KitProg3 programming mode selection button (SW3):** This button can be used to switch between various modes of operation of KitProg3 (CMSIS-DAP BULK, CMSIS-DAP HID or DAPLink modes). For more details, see the KitProg3 User Guide.
5. **PSoC 6 MCU VDD current measurement jumper (J15):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDD power domain. Please refer to Power Supply System on page 33 for details on power domains that are monitored by current measurement jumpers.
6. **PSoC 6 MCU VDDIO2 and CYW43012 VDDIO power selection jumper (J16):** This jumper is used to select the PSoC 6 MCU VDDIO2 and CYW43012 VDDIO supply voltage between 1.8 V and 3.3 V. This is not loaded by default. This board supports operation of VDDIO at 1.8 V.
7. **PSoC 6 MCU VDDIO0 current measurement jumper (J19):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDDIO0 power domain. This is not loaded by default. Before populating the jumper for current measurements, ensure that R97 is removed.
8. **External power supply VIN connector (J5):** This connector connects an external DC power supply input to the onboard regulators.

9. **PSoC 6 MCU user button (SW2):** This button can be used to provide an input to the PSoC 6 MCU. Note that by default it connects the PSoC 6 MCU pin to ground when pressed, so you need to configure the PSoC 6 MCU pin as a digital input with resistive pull-up for detecting the button press. It also provides a wake-up source from low-power modes of the device.
10. **Arduino-compatible power header (J1):** This header powers the Arduino shields. It also has a provision to power the kit though the VIN input.
11. **PSoC 6 MCU reset button (SW1):** This button is used to reset the PSoC 6 MCU. It connects the PSoC 6 MCU reset (XRES) pin to ground.
12. **PSoC 6 MCU debug and trace header (J12):** This header can be connected to an Embedded Trace Macrocell (ETM)-compatible programmer/debugger. This is not loaded by default.
13. **PSoC 6 MCU program and debug header (J11):** This 10-pin header allows you to program and debug the PSoC 6 MCU using an external programmer such as MiniProg4.
14. **Arduino Uno R3-compatible I/O headers (J2, J3, and J4):** These I/O headers bring out pins from the PSoC 6 MCU to interface with Arduino shields. Some of these pins are multiplexed with onboard peripherals and are not connected to the PSoC 6 MCU by default. For a detailed information on how to rework the kit to access these pins, see Table 2-1 on page 13.
15. **CapSense slider (SLIDER) and buttons (BTN0 and BTN1):** The CapSense touch-sensing slider and two buttons, all of which are capable of both self-capacitance (CSD) and mutual-capacitance (CSX) operation, allow you to evaluate Cypress' fourth-generation CapSense technology. The slider and buttons have a 1-mm acrylic overlay for smooth touch sensing.
16. **PSoC 6 MCU VDDIO2 current measurement jumper (J18):** An ammeter can be connected to this jumper to measure the current consumed by the PSoC 6 MCU VDDIO2 power domain. This jumper is not loaded by default on the board. Before populating the jumper for current measurements, ensure that R94 is removed.
17. **CYW43012 VDDIO current measurement jumper(J17):** An ammeter can be connected to this jumper to measure the current consumed by the CYW43012 VDDIO power domain.
18. **Cypress serial NOR flash memory (S25FS512S, U3):** A S25FS512S NOR flash of 512-Mbit capacity is connected to the Quad SPI interface of the PSoC 6 MCU. The NOR device can be used for both data and code memory with execute-in-place (XIP) support and encryption.
19. **Cypress PSoC 6 (1M) with CYW43012 USI SiP Carrier Module (CYW9P62S1-43012CAR-01, MOD1):** This kit is designed to highlight the features of the PSoC 6 MCU on the CYW9P62S1-43012CAR-01. For details, see CYW9P62S1-43012CAR-01 (MOD1) on page 26. This kit is designed to highlight the features of the PSoC 6 MCU. For details on PSoC 6 MCU pin mapping, refer to Table 2-1 on page 13.
20. **USI WM-BAC-CYW-50 SiP module:** WM-BAC-CYW-50 is an SiP module that includes the PSoC 6 MCU, CY8C6247FDI-D52 and CYW43012 (Wi-Fi + Bluetooth combo device). The module provides 2.4 GHz and 5 GHz dual-band WLAN and Bluetooth functionality and complies with IEEE 802.11a/b/g/n and Bluetooth Version 5.0.
21. **Wi-Fi/BT antenna:** This is an onboard antenna connected to the Wi-Fi and Bluetooth module.

22. **Cypress Quad SPI Ferroelectric-RAM (CY15V104QSN, U4):** The CY15V104QSN is a 4-Mbit nonvolatile memory employing an advanced ferroelectric process. F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years and is connected to the Quad SPI interface of the PSoC 6 MCU.
23. **CYW43012 VBAT current measurement jumper (J8):** An ammeter can be connected to this jumper to measure the current consumed by the CYW43012 VBAT power domain.
24. **CYW43012 VBAT power selection jumper (J9):** This board supports VBAT voltages of 3.3 V and 3.6 V. VBAT is 3.3 V when the jumper is not inserted and 3.6 V when the jumper is inserted.
25. **PSoC 6 MCU user LEDs (LED8 and LED9):** These two user LEDs can operate at the entire operating voltage range of the PSoC 6 MCU. The LEDs are active LOW, so the pins must be driven to ground to turn ON the LEDs.
26. **PSoC 6 I/O header (J21, J22, J24):** These headers provide connectivity to PSoC 6 MCU GPIOs that are not connected to the Arduino compatible headers. Some of these I/Os are also connected to on-board peripherals see Table 2-1 on page 13 for pin mapping.
27. **Wi-Fi/BT GPIO header (J23):** This header brings out a few IOs of the CYW43012 for general purpose applications.
28. **PSoC 6 USB device connector (J7):** The USB cable provided with the PSoC 62S1 Wi-Fi BT Pioneer Kit can also be connected between this USB connector and the PC to use the PSoC 6 MCU USB device applications.
29. **Optional USB Host power supply header (J10):** This header provides an option to supply external power to the PSoC 6 USB when used as a USB Host. This is not loaded by default.
30. **KitProg3 status LED (LED2):** This Yellow LED indicates the status of KitProg3. For details on the KitProg3 status, see the KitProg3 User Guide.
31. **KitProg3 (PSoC 5LP) programmer and debugger (CY8C5868LTI-LP039, U2):** The PSoC 5LP device (CY8C5868LTI-LP039) serving as KitProg3, is a multi-functional system, which includes a SWD programmer, debugger, USB-I2C bridge and USB-UART bridge. For more details, see the KitProg3 User Guide.

See Hardware Functional Description on page 26 for details on various hardware blocks.

2.2 KitProg3: On-Board Programmer/Debugger

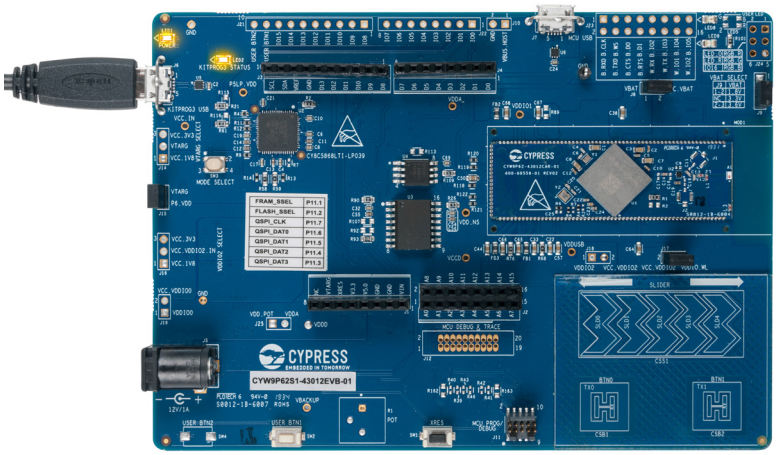
The PSoC 62S1 Wi-Fi BT Pioneer Board can be programmed and debugged using the onboard KitProg3. KitProg3 is an onboard programmer/debugger with additional USB-UART and USB-I2C functionality. A Cypress PSoC 5LP device is used to implement the KitProg3. For more details on the KitProg3 functionality, see the KitProg3 User Guide.

2.2.1 Programming and Debugging using ModusToolbox

This section presents a quick overview of programming and debugging using ModusToolbox. For detailed instructions, see **Help** > **ModusToolbox IDE Documentation** > **User Guide**.

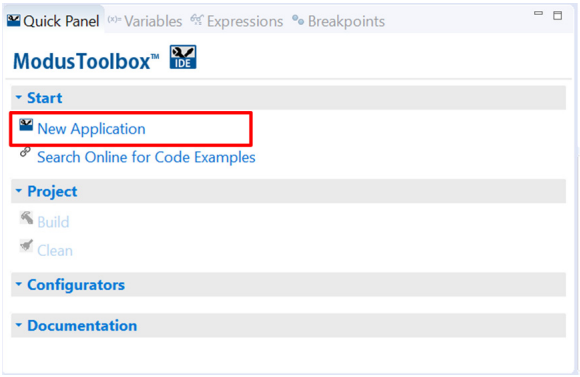
1. Connect the board to the PC using the USB cable, as shown in Figure 2-7. It enumerates as a USB Composite Device. KitProg3 can operate either in CMSIS-DAP Bulk mode (default), CMSIS-DAP HID mode or DAPLink mode (DAPLink mode is required for programing using Mbed CLI). KitProg3 also supports CMSIS-DAP Bulk with two UARTs. Programming is faster with the Bulk mode. The status LED (Yellow) is always ON in Bulk mode, ramping at a 1 Hz rate in HID mode, and ramping at a 2 Hz rate in DAPLink mode. Press and release the Mode select button (SW3) to switch between these modes. If you do not see the desired LED status, see the KitProg3 User Guide for details on the KitProg3 status and troubleshooting instructions.

Figure 2-7. Connect USB Cable to USB Connector on the Board



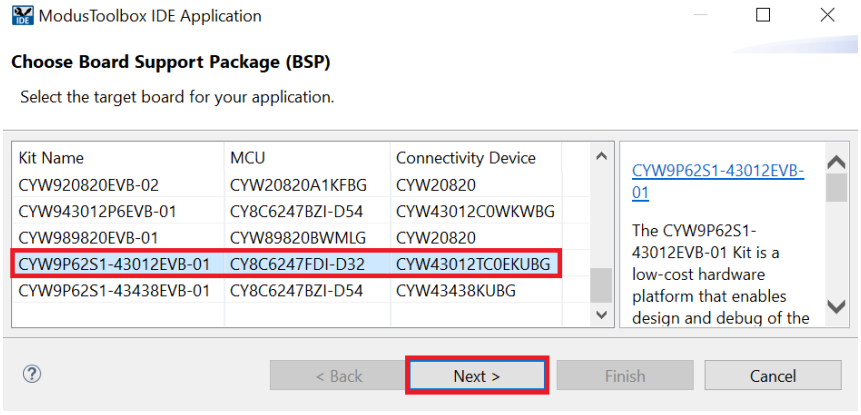
2. In the ModusToolbox IDE, import the desired code example (application) into a new workspace.
   a. Click on **New Application** from **Quick Panel**.

Figure 2-8. Create New Application



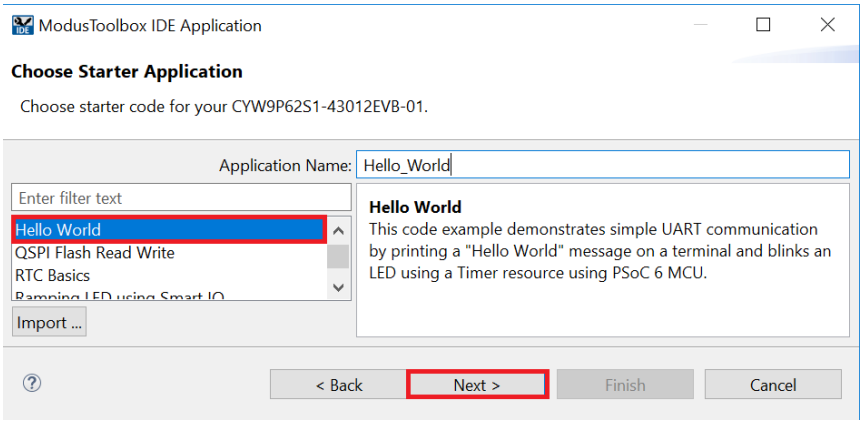
b. Select the CYW9P62S1-43012EVB-01 in the **Choose Board Support Package (BSP)** window and click **Next**, as shown in Figure 2-9.

Figure 2-9. New Application Creation: Choose Board Support Package (BSP)



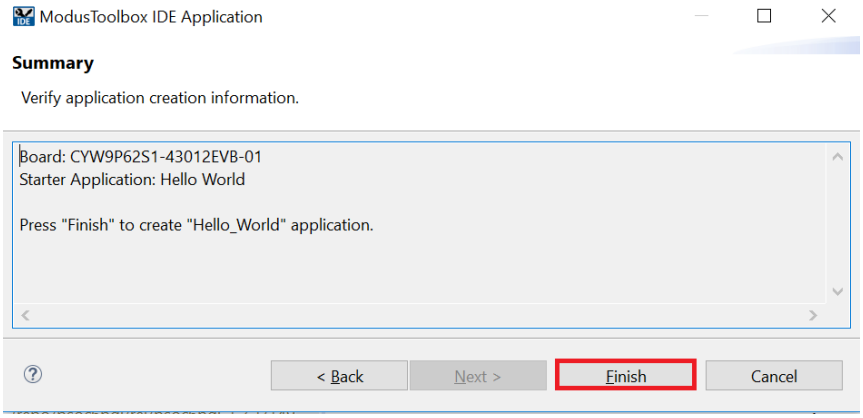
c. Select the application in the **Choose Starter Application** window and click **Next**, as shown in Figure 2-10. You may optionally change the application name in this window before clicking **Next**.

Figure 2-10. New Application Creation: Choose Starter Application



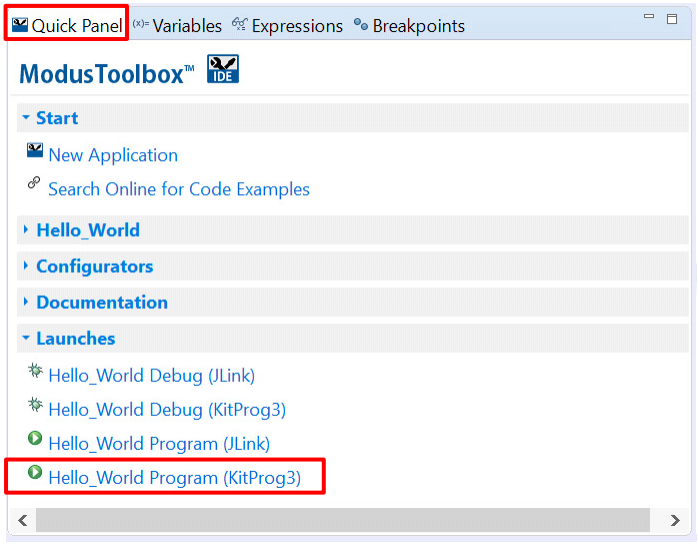
d. Click **Finish** in the **Summary** window, as shown in Figure 2-11.

Figure 2-11. New Application Creation: Summary



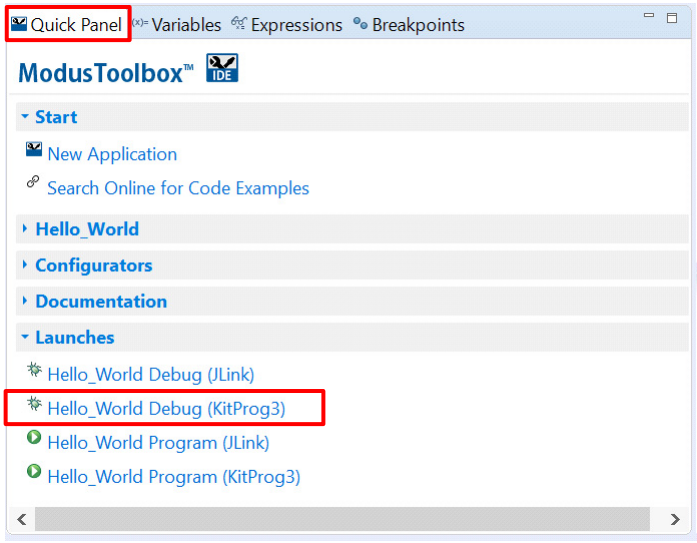
3. To build and program a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Program (KitProg3)** configuration as shown in Figure 2-12.

Figure 2-12. Programming in ModusToolbox



4. ModusToolbox has an integrated debugger. To debug a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Debug (KitProg3)** configuration as shown in Figure 2-13. For a detailed explanation on how to debug using ModusToolbox, see KBA224621.

Figure 2-13. Debugging in ModusToolbox



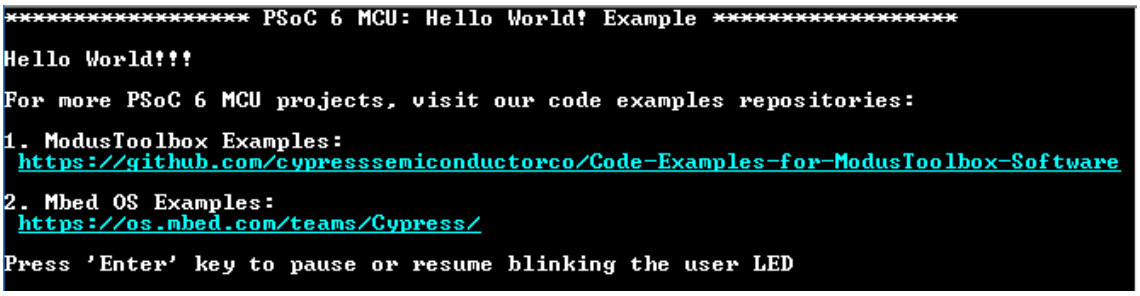
2.2.1.1 Using the OOB Example – PSoC 6 MCU: Hello World

The PSoC 62S1 Wi-Fi BT Pioneer Board is by default programmed with the code example: PSoC 6 MCU: Hello World. The steps below describe how to use the example. For a detailed description of the project refer to the example's readme file in the GitHub repository.

Note: At any point, if you overwrite the OOB example, you can restore it by programming the PSoC 6 MCU: Hello World application. Refer Programming and Debugging using ModusToolbox on page 20 for programming the board.

1. Connect the board to your PC using the provided USB cable through the KitProg3 USB connector.
2. Open a terminal program and select the KitProg3 COM port. Set the serial port parameters to 8N1 and 115200 baud.
3. Press the XRES switch (SW1) on the board and confirm that "Hello World!!!" and other text is displayed on the UART Terminal application as shown in Figure 2-14.

Figure 2-14. Hello World in Terminal



4. Confirm that the kit LED blinks at 1 Hz.
5. Press the Enter key. Confirm that the kit LED stops blinking. The terminal displays the message "LED blinking paused".
6. Press the Enter key again. Confirm that the kit LED resumes blinking at 1 Hz. The message displayed on the terminal is updated to "LED blinking resumed".

You can repeat steps 5 and 6 indefinitely.

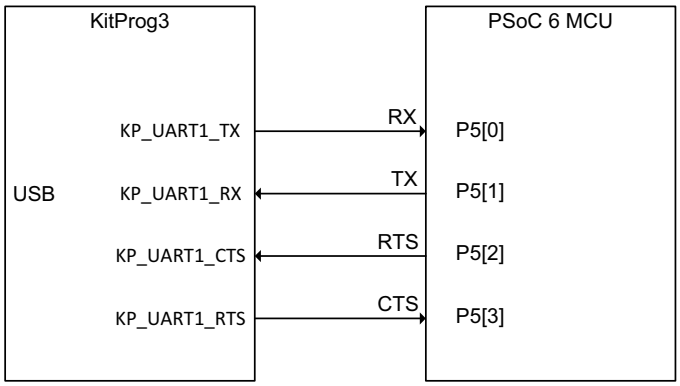
2.2.2 USB-UART Bridge

The KitProg3 on the PSoC 62S1 Wi-Fi BT Pioneer Board can act as a USB-UART bridge.

The KitProg 3 has two USB-UART bridges. The primary UART is connected to the PSoC 6 MCU and the secondary UART is connected to the CYW43012. The primary UART can always be accessed through USB, while the secondary UART can be accessed by changing the mode of the KitProg3 to BULK with two UARTs Mode. For more details on the KitProg3 USB-UART functionality, see the KitProg3 User Guide.

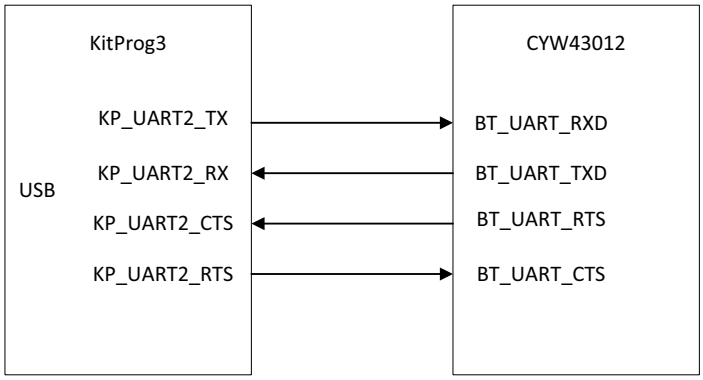
The primary UART and flow-control lines between the PSoC 6 MCU and the KitProg3 are hard-wired on the board, as Figure 2-15 shows.

Figure 2-15. UART Connection between KitProg3 and PSoC 6 MCU



The secondary UART and flow-control lines between the CYW43012 and the KitProg3 are hard-wired on the board, as Figure 2-16 shows.

Figure 2-16. UART Connection between KitProg3 and CYW43012

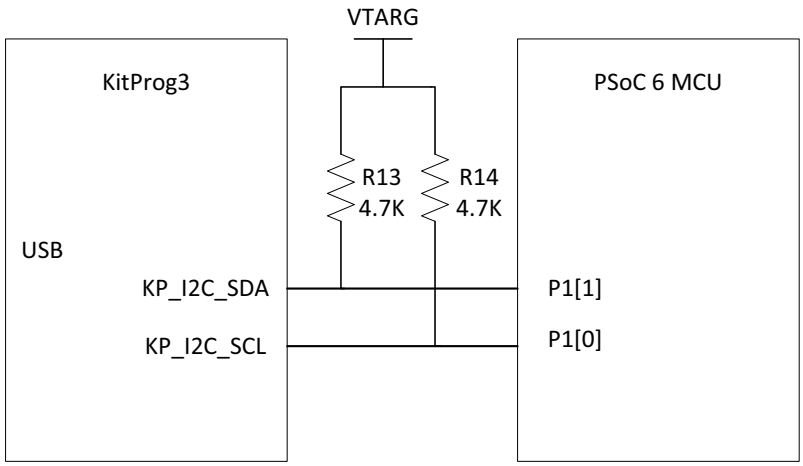


For more details on the KitProg3 USB-UART functionality, see the KitProg3 User Guide.

2.2.3 USB-I2C Bridge

The KitProg3 can function as a USB-I2C bridge and can communicate with the Bridge Control Panel (BCP) software which acts as an I2C master. The I2C lines on the PSoC 6 MCU are hard-wired on the board to the I2C lines of the KitProg3, with onboard pull-up resistors as Figure 2-17 shows. The USB-I2C supports I2C speeds of 50 kHz, 100 kHz, 400 kHz, and 1 MHz. For more details on the KitProg3 USB-I2C functionality, see the KitProg3 User Guide.

Figure 2-17. I2C Connection between KitProg3 and PSoC 6 MCU



3. Hardware

3.1 Schematics

Refer to the schematic files available in the kit webpage.

3.2 Hardware Functional Description

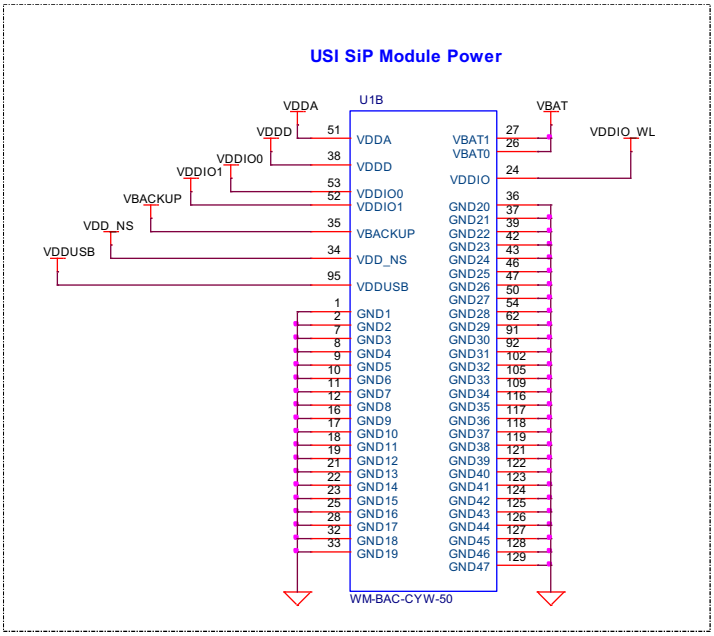
This section explains in detail the individual hardware blocks.

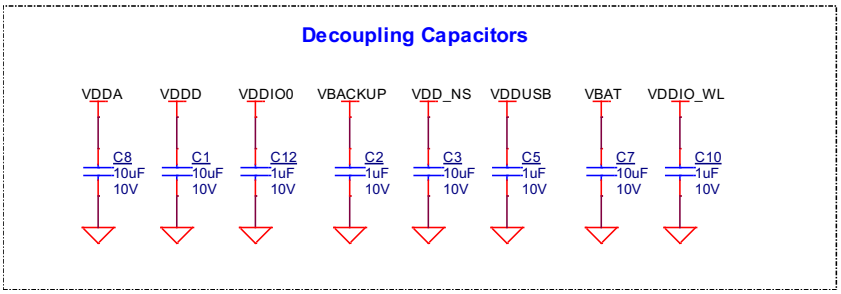
3.2.1 CYW9P62S1-43012CAR-01 (MOD1)

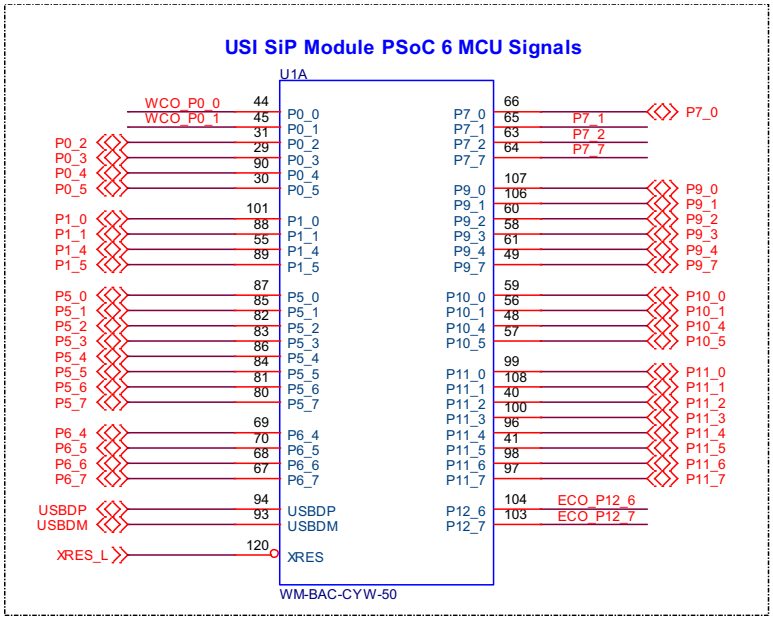
CYW9P62S1-43012CAR-01 PSoC 6 (1M) with CYW43012 USI SiP Carrier Module is a castellated PCB module which consists mainly of an USI SiP module, WM-BAC-CYW-50, with a PSoC 6 MCU and CYW43012. The module also houses a 2.45 GHz/5.5 GHz dual band chip antenna, RF switch for antenna diversity, crystal oscillators for the PSoC 6 MCU, modulation and integration capacitors to support CapSense and other passive components required for the proper working of the PSoC 6 MCU and CYW43012. The antenna used is 2450AD14A5500 Dual Band 2.45 GHz/5.5 GHz Mini Chip Antenna from Johanson. The castellated PCB module has 137 castellated pads, which are used for different voltage rails and I/O signals of PSoC 6 MCU and CYW43012.

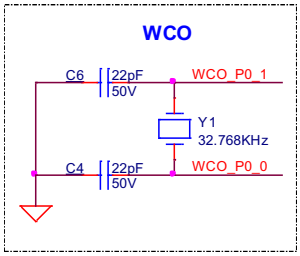
For more information, see the PSoC 6 MCU webpage, PSoC 6 MCU datasheet and WM-BAC-CYW-50 module webpage.

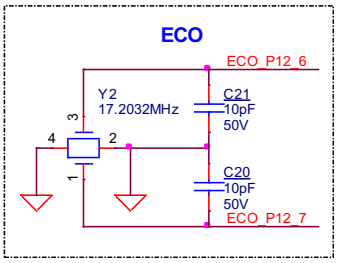
Figure 3-1. Schematics of CYW9P62S1-43012CAR-01

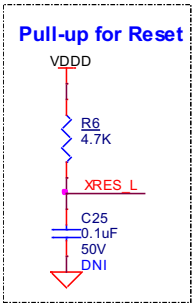


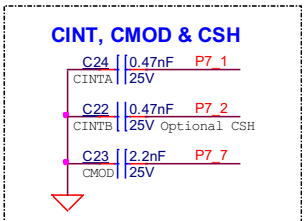

Decoupling Capacitors
VDDA
VDDD
VDDIO0
VBACKUP
VDD_NS
VDDUSB
VBAT
VDDIO_WL
C8 10uF 10V
C1 10uF 10V
C12 1uF 10V
C2 1uF 10V
C3 10uF 10V
C5 1uF 10V
C7 10uF 10V
C10 1uF 10V

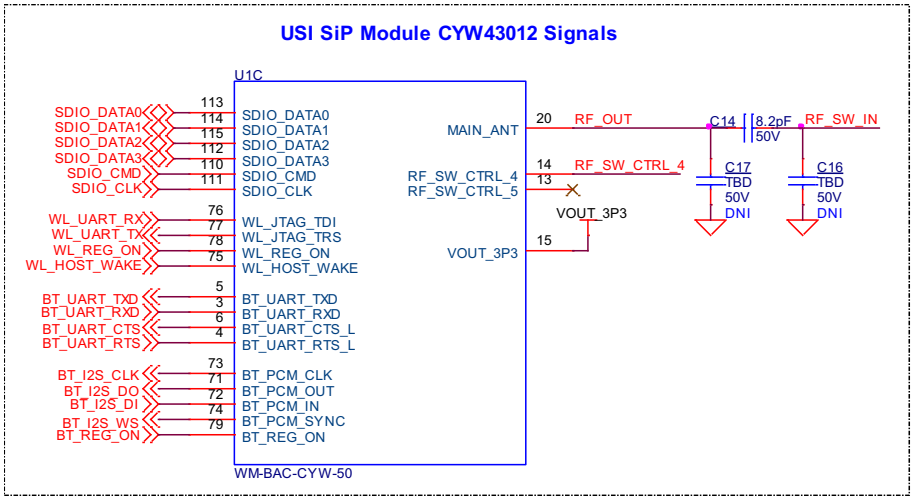

USI SiP Module PSoC 6 MCU Signals
U1A
WM-BAC-CYW-50
WCO_P0_0
WCO_P0_1
P0_2
P0_3
P0_4
P0_5
P1_0
P1_1
P1_4
P1_5
P5_0
P5_1
P5_2
P5_3
P5_4
P5_5
P5_6
P5_7
P6_4
P6_5
P6_6
P6_7
USBDP
USBDM
XRES_L
P7_0
P7_1
P7_2
P7_7
P9_0
P9_1
P9_2
P9_3
P9_4
P9_7
P10_0
P10_1
P10_4
P10_5
P11_0
P11_1
P11_2
P11_3
P11_4
P11_5
P11_6
P11_7
P12_6
P12_7
ECO_P12_6
ECO_P12_7
XRES

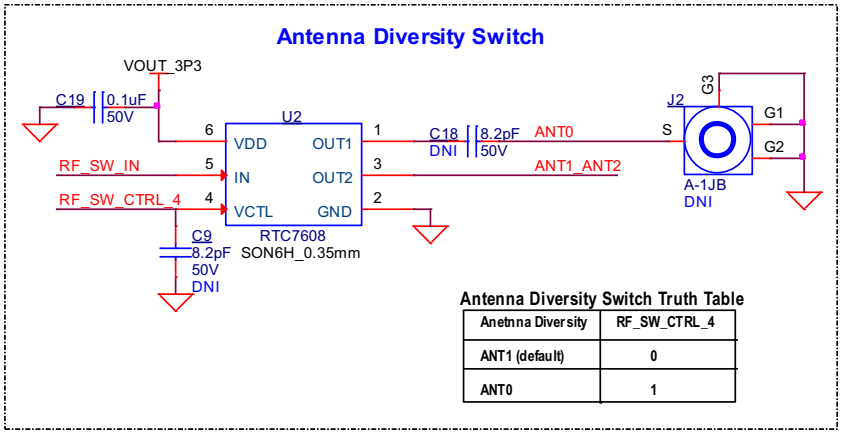

WCO
C6 22pF 50V
WCO_P0_1
Y1 32.768KHz
C4 22pF 50V
WCO_P0_0

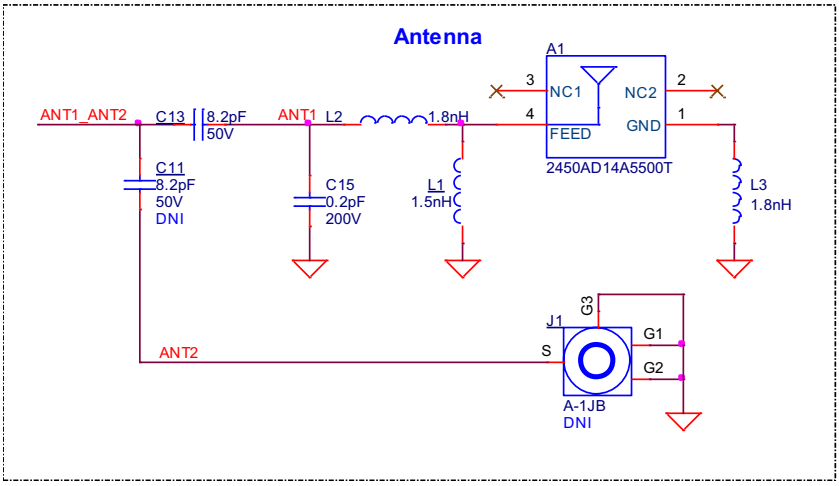

ECO
ECO_P12_6
Y2 17.2032MHz
C21 10pF 50V
C20 10pF 50V
ECO_P12_7

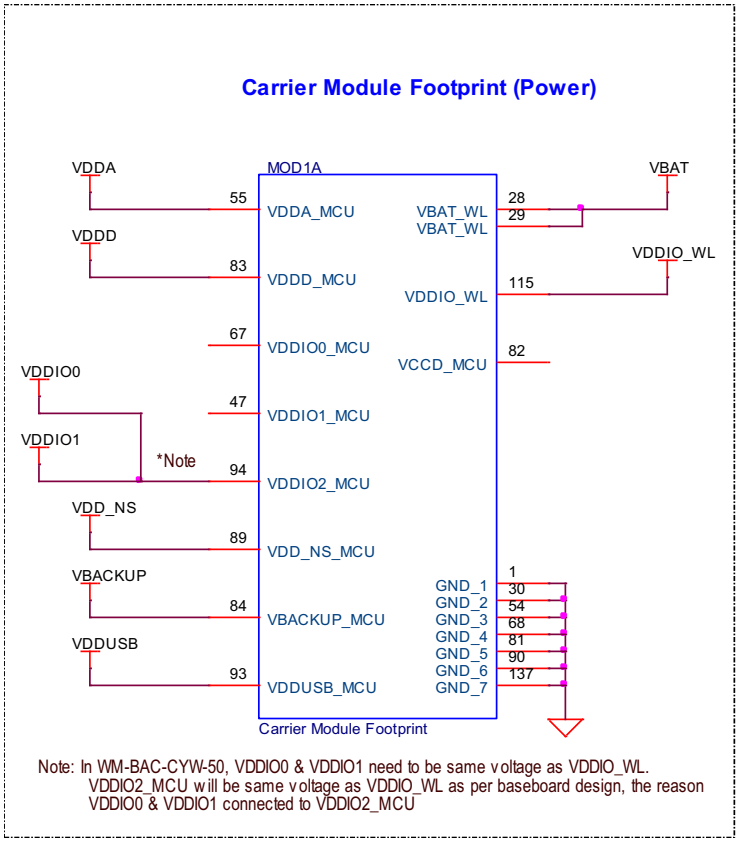

Pull-up for Reset
VDDD
R6 4.7K
XRES_L
C25 0.1uF 50V DNI

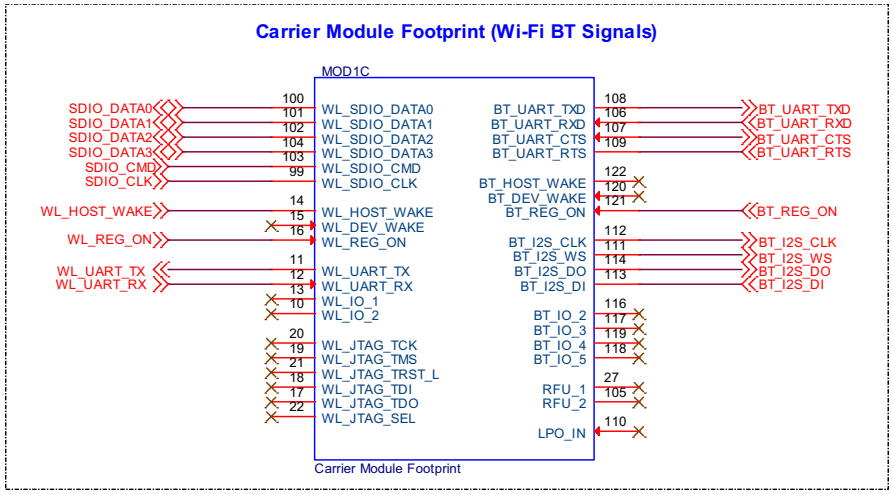

CINT, CMOD & CSH
C24 0.47nF 25V
CINTA
P7_1
C22 0.47nF 25V Optional CSH
CINTB
P7_2
C23 2.2nF 25V
CMOD
P7_7

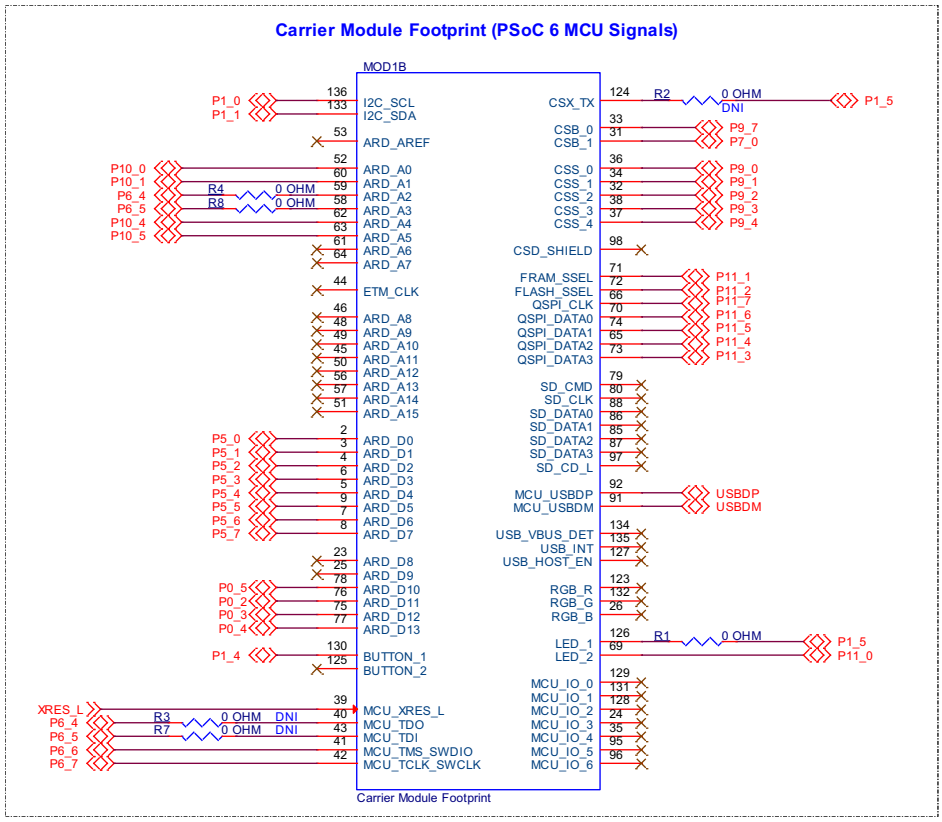

USI SiP Module CYW43012 Signals
U1C
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
SDIO_CMD
SDIO_CLK
WL_UART_RX
WL_UART_TX
WL_REG_ON
WL_HOST_WAKE
BT_UART_TXD
BT_UART_RXD
BT_UART_CTS
BT_UART_RTS
BT_I2S_CLK
BT_I2S_DO
BT_I2S_DI
BT_I2S_WS
BT_REG_ON
WL_JTAG_TDI
WL_JTAG_TRS
BT_UART_CTS_L
BT_UART_RTS_L
BT_PCM_CLK
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
MAIN_ANT
RF_SW_CTRL_4
RF_SW_CTRL_5
VOUT_3P3
RF_OUT
RF_SW_IN
C14 8.2pF 50V
C17 TBD 50V DNI
C16 TBD 50V DNI
WM-BAC-CYW-50


Antenna Diversity Switch
VOUT_3P3
C19 0.1uF 50V
U2
VDD
IN
VCTL
OUT1
OUT2
GND
RTC7608
SON6H_0.35mm
C9 8.2pF 50V DNI
RF_SW_IN
RF_SW_CTRL_4
C18 8.2pF 50V DNI
ANT0
ANT1_ANT2
J2
G1
G2
G3
A-1JB DNI
Antenna Diversity Switch Truth Table
Anetnna Diversity
RF_SW_CTRL_4
ANT1 (default)
0
ANT0
1


Antenna
A1
NC1
NC2
FEED
GND
2450AD14A5500T
ANT1_ANT2
C13 8.2pF 50V
ANT1
L2 1.8nH
C11 8.2pF 50V DNI
C15 0.2pF 200V
L1 1.5nH
L3 1.8nH
J1
G1
G2
G3
A-1JB DNI
ANT2


Carrier Module Footprint (Power)
MOD1A
VDDA
55
VDDA_MCU
VDDD
83
VDDD_MCU
67
VDDIO0_MCU
VDDIO0
47
VDDIO1_MCU
VDDIO1
*Note
94
VDDIO2_MCU
VDD_NS
89
VDD_NS_MCU
VBACKUP
84
VBACKUP_MCU
VDDUSB
93
VDDUSB_MCU
VBAT_WL
VBAT_WL
28
29
VBAT
VDDIO_WL
115
VDDIO_WL
VCCD_MCU
82
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
1
30
54
68
81
90
137
Carrier Module Footprint
Note: In WM-BAC-CYW-50, VDDIO0 & VDDIO1 need to be same voltage as VDDIO_WL.
VDDIO2_MCU will be same voltage as VDDIO_WL as per baseboard design, the reason
VDDIO0 & VDDIO1 connected to VDDIO2_MCU


Carrier Module Footprint (Wi-Fi BT Signals)
MOD1C
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
SDIO_CMD
SDIO_CLK
WL_HOST_WAKE
WL_REG_ON
WL_UART_TX
WL_UART_RX
100
101
102
104
103
99
14
15
16
11
12
13
10
20
19
21
18
17
22
WL_SDIO_DATA0
WL_SDIO_DATA1
WL_SDIO_DATA2
WL_SDIO_DATA3
WL_SDIO_CMD
WL_SDIO_CLK
WL_HOST_WAKE
WL_DEV_WAKE
WL_REG_ON
WL_UART_TX
WL_UART_RX
WL_IO_1
WL_IO_2
WL_JTAG_TCK
WL_JTAG_TMS
WL_JTAG_TRST_L
WL_JTAG_TDI
WL_JTAG_TDO
WL_JTAG_SEL
BT_UART_TXD
BT_UART_RXD
BT_UART_CTS
BT_UART_RTS
BT_HOST_WAKE
BT_DEV_WAKE
BT_REG_ON
BT_I2S_CLK
BT_I2S_WS
BT_I2S_DO
BT_I2S_DI
BT_IO_2
BT_IO_3
BT_IO_4
BT_IO_5
RFU_1
RFU_2
LPO_IN
108
106
107
109
122
120
121
112
111
114
113
116
117
119
118
27
105
110
BT_UART_TXD
BT_UART_RXD
BT_UART_CTS
BT_UART_RTS
BT_REG_ON
BT_I2S_CLK
BT_I2S_WS
BT_I2S_DO
BT_I2S_DI
Carrier Module Footprint

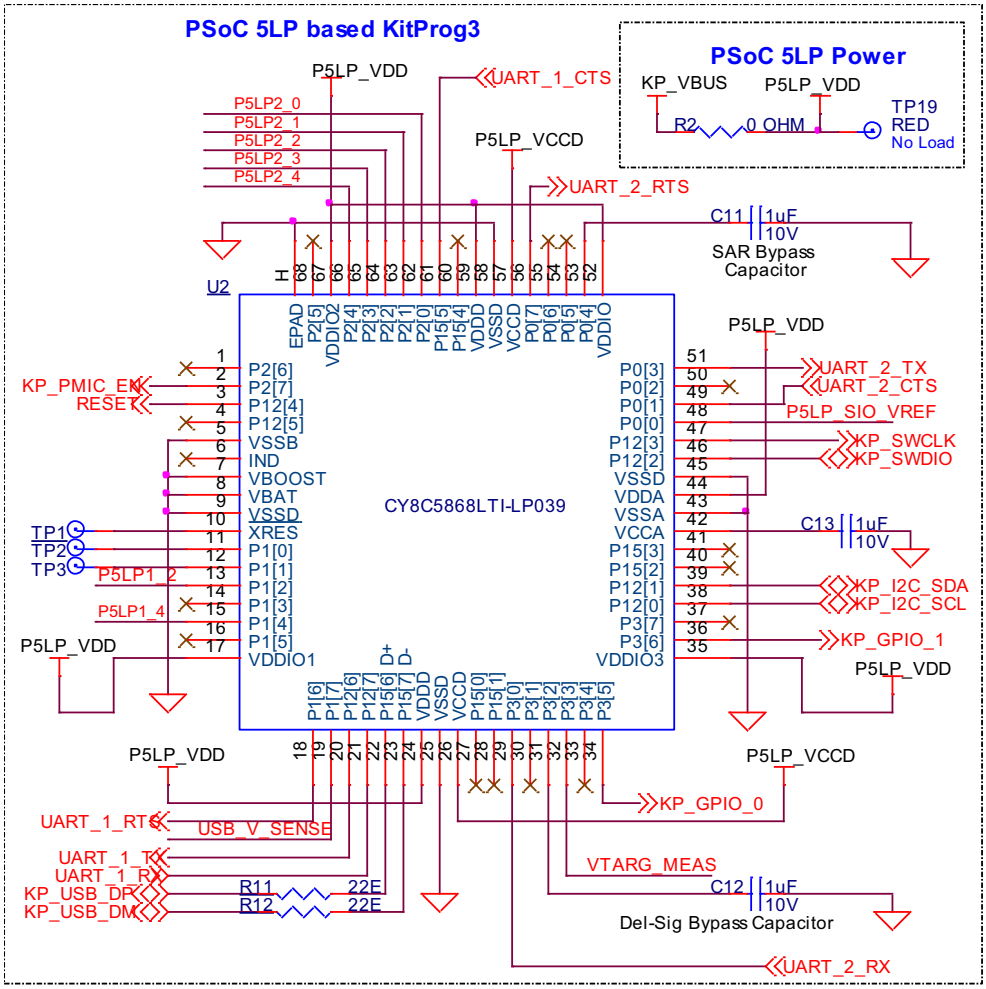

Carrier Module Footprint (PSoC 6 MCU Signals)
MOD1B
Carrier Module Footprint
P1_0
P1_1
I2C_SCL
I2C_SDA
ARD_AREF
P10_0
P10_1
P6_4
P6_5
P10_4
P10_5
R4
R8
0 OHM
ARD_A0
ARD_A1
ARD_A2
ARD_A3
ARD_A4
ARD_A5
ARD_A6
ARD_A7
ETM_CLK
ARD_A8
ARD_A9
ARD_A10
ARD_A11
ARD_A12
ARD_A13
ARD_A14
ARD_A15
P5_0
P5_1
P5_2
P5_3
P5_4
P5_5
P5_6
P5_7
ARD_D0
ARD_D1
ARD_D2
ARD_D3
ARD_D4
ARD_D5
ARD_D6
ARD_D7
ARD_D8
ARD_D9
P0_5
P0_2
P0_3
P0_4
ARD_D10
ARD_D11
ARD_D12
ARD_D13
P1_4
BUTTON_1
BUTTON_2
XRES_L
P6_4
P6_5
P6_6
P6_7
R3
R7
0 OHM
DNI
MCU_XRES_L
MCU_TDO
MCU_TDI
MCU_TMS_SWDIO
MCU_TCLK_SWCLK
CSX_TX
R2
P1_5
CSB_0
CSB_1
P9_7
P7_0
CSS_0
CSS_1
CSS_2
CSS_3
CSS_4
P9_0
P9_1
P9_2
P9_3
P9_4
CSD_SHIELD
FRAM_SSEL
FLASH_SSEL
QSPI_CLK
QSPI_DATA0
QSPI_DATA1
QSPI_DATA2
QSPI_DATA3
P11_1
P11_2
P11_7
P11_6
P11_5
P11_4
P11_3
SD_CMD
SD_CLK
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
SD_CD_L
MCU_USBDP
MCU_USBDM
USBDP
USBDM
USB_VBUS_DET
USB_INT
USB_HOST_EN
RGB_R
RGB_G
RGB_B
LED_1
LED_2
R1
P11_0
MCU_IO_0
MCU_IO_1
MCU_IO_2
MCU_IO_3
MCU_IO_4
MCU_IO_5
MCU_IO_6

3.2.2 PSoC 5LP-based KitProg3 (U2)

An onboard PSoC 5LP (CY8C5868LTI-LP039) device is used as KitProg3 to program and debug PSoC 6 MCU. The PSoC 5LP device connects to the USB port of a PC through a USB connector and to the SWD and other communication interfaces of PSoC 6 MCU.

The PSoC 5LP device is a true system-level solution providing MCU, memory, analog, and digital peripheral functions in a single chip. For more information, visit the PSoC 5LP web page. Also, see the CY8C58LPxx Family datasheet.

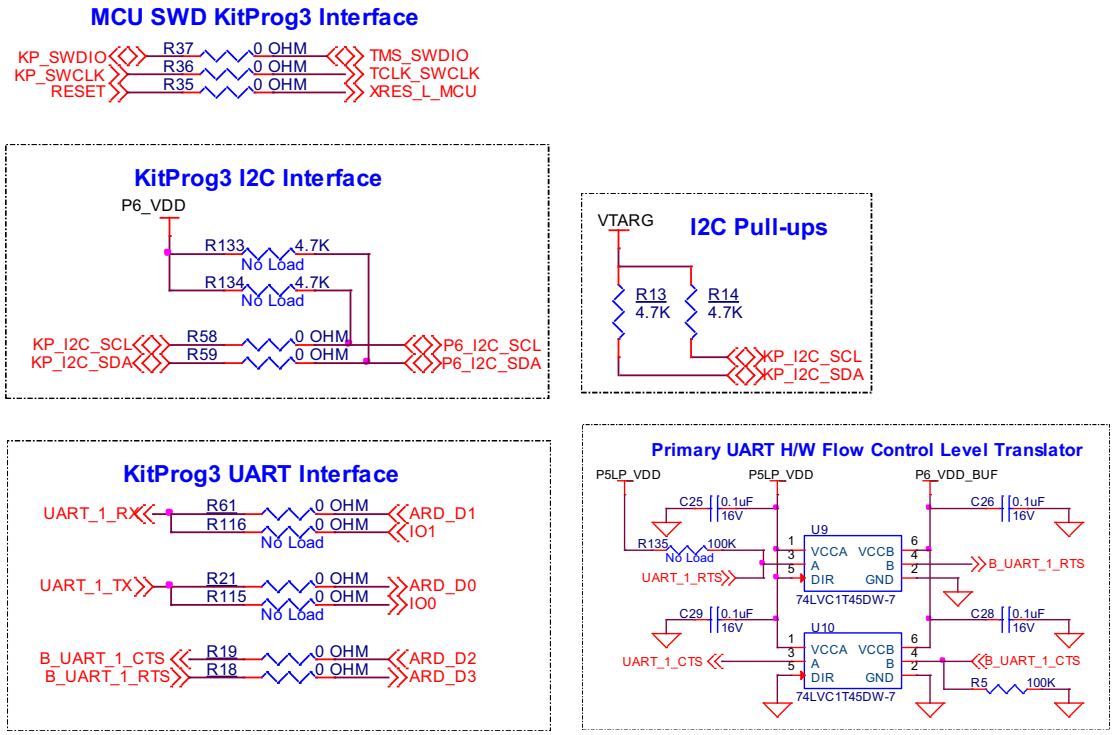
Figure 3-2. Schematics of PSoC 5LP based KitProg3



3.2.3 Serial Interconnection between PSoC 5LP and PSoC 6 MCU

In addition to the use as an onboard programmer, the PSoC 5LP device functions as an interface for the USB-UART and USB-I2C bridges, as shown in Figure 3-3. The USB-Serial pins of the PSoC 5LP device are hard-wired to the I2C/UART pins of the PSoC 6 MCU. These pins are also available on the Arduino-compatible I/O headers.

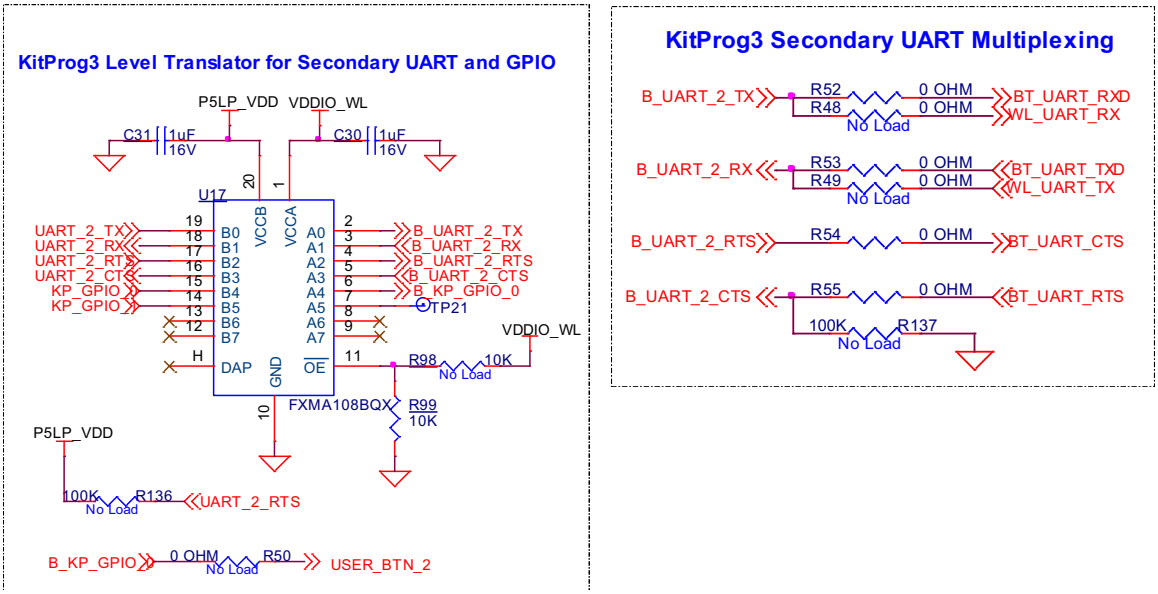
Figure 3-3. Schematics of Programming and Serial Interface Connections



3.2.4 Serial Interconnection Between PSoC 5LP and CYW43012

The PSoC 5LP device also has a secondary UART that is connected to the BT_UART of the CYW43012 (USI WM-BAC-CYW-50).

Figure 3-4. Serial Interconnection Between PSoC 5LP and CYW43012

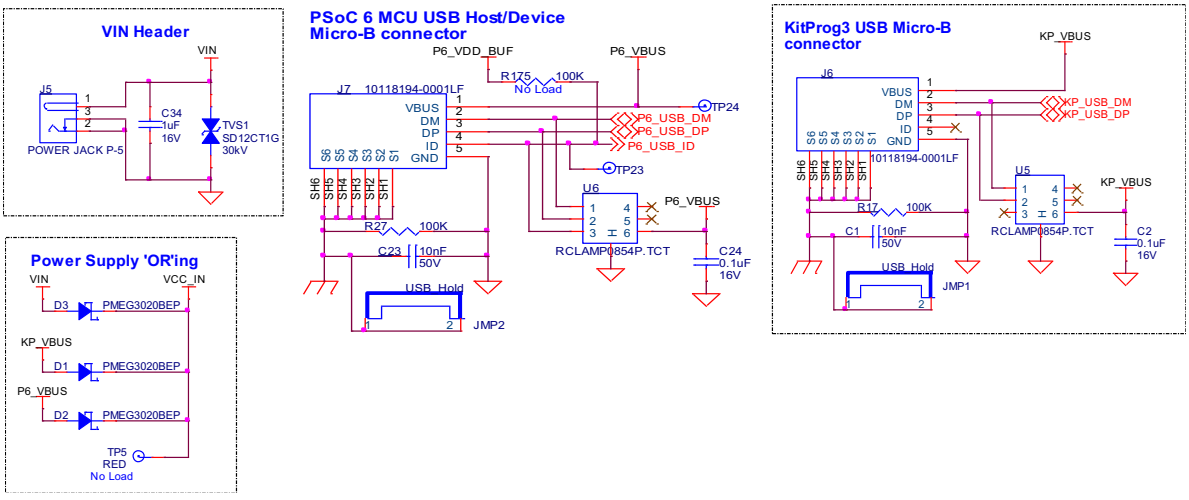


3.2.5 Power Supply System

The power supply system on this board is versatile, allowing the input supply to come from the following sources:

- 5V from the onboard USB Micro-B connectors (**J6** or **J7**)
- 7V–12V from external power supply through the VIN barrel jack (**J5**) or from an Arduino shield

Figure 3-5. Schematics of Power Supply Input and OR'ing



3.2.5.1 *Voltage regulators*

The power supply system is designed for the voltage configurations listed in Table 3-1. Some configurations achievable on this kit are outside the operating range for the device. However, it is not possible to achieve all applicable configurations by changing jumper positions but rather requires re-work of respective 0-ohm resistors.

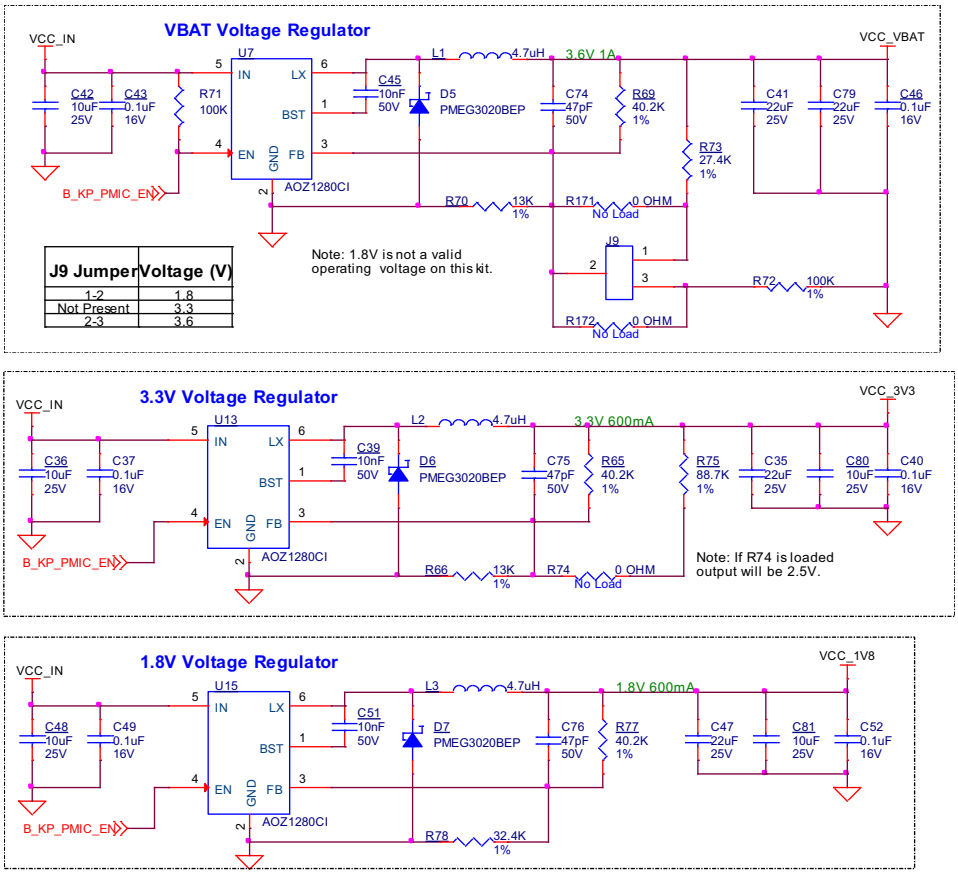
VDDIO_WL and VDDIO2_MCU must be at the same voltage since they power the SDIO interface between the PSoC 6 MCU and CYW43012. Hence both are supplied by the VCC_VDDIO2_IN domain.

Three buck regulators **U15**, **U13** and **U7** are used to achieve 1.8 V, 3.3 V and 3.6 V outputs respectively. Figure 3-6 shows the schematics of the voltage regulator circuits.

Table 3-1. Operating voltage ranges of domains

Voltage Domain	Carrier Module (MOD1) Power Pins powered by the domain	Operating Voltage		Voltage Configuration applicable in kit	Voltage Selection Header
		Min (V)	Max (V)		
VCC_VBAT	VBAT_WL	3.2	4.2	3.6V, 3.3V	J9
VCC_VDDIO2_IN	VDDIO2_MCU, VDDIO_WL	1.62	1.98	1.8V	J16 (not loaded)
VTARG	VDDD_MCU, VDDIO1_MCU, VDDA_MCU, VDD_NS_MCU, VBACKUP_MCU	1.7	1.98	1.8V	J14 (not loaded)
VCC_VDDIO0	VDDIO0_MCU	1.7	1.98	1.8V	None (uses 0 Ohms)

Figure 3-6. Voltage Regulators



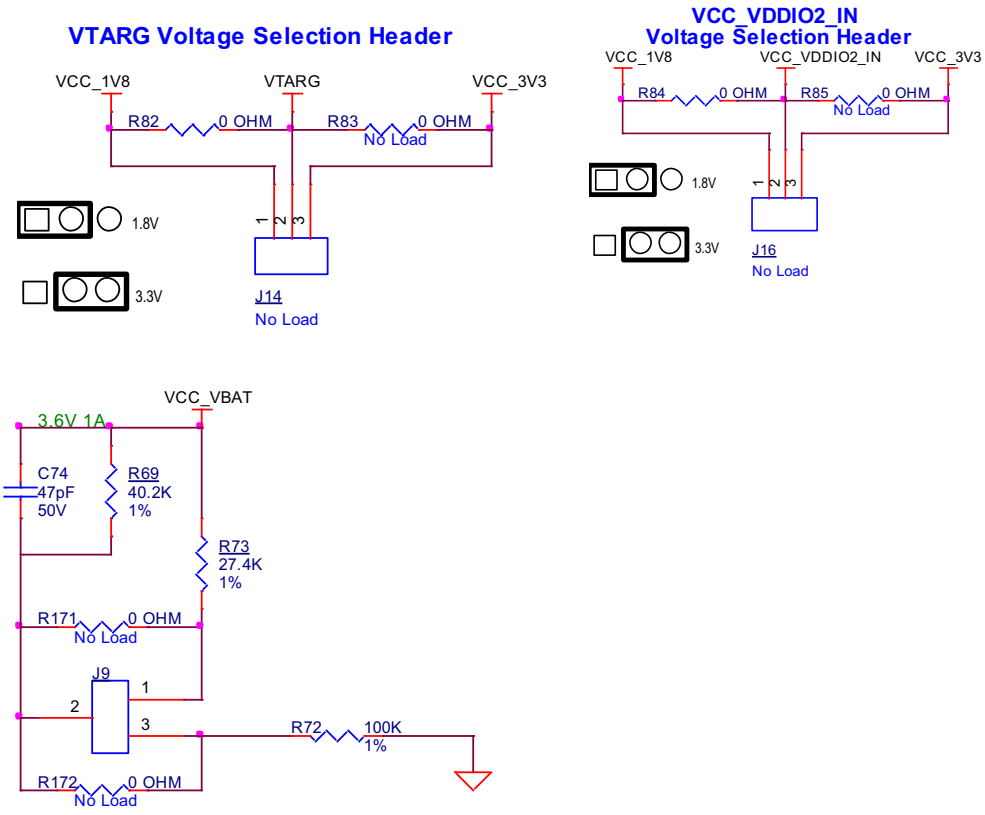
3.2.5.2 *Voltage Selection*

VCC_VBAT has a dedicated regulator that changes voltage by varying the feedback voltage through the resistor network at **J9**.

VTARG and VCC_VDDIO2_IN have dedicated 3-pin voltage selection headers **J14** and **J16** respectively that select between VCC_3V3 or VCC_1V8 voltages. Figure 3-7 shows the schematics of the power selection circuits.

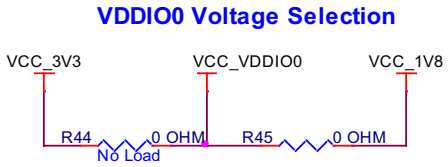
Note: In this kit, CYW43012 only works with VCC_VDDIO2_IN at VCC_1V8 configuration and hence by default, **R84** is loaded and **J16** is not loaded. Similarly, PSoC 6 MCU only works with VTARG at VCC_1V8 configuration and hence **R82** is loaded and **J14** is not loaded.

Figure 3-7. Voltage Selection Headers



VCC_VDDIO0 voltage can be selected between VCC_3V3 and VCC_1V8 using zero-ohm resistors. In this kit it is connected to VCC_1V8 as Quad SPI Flash (powered by VCC_VDDIO0) only works as 1.8V. Please do not change VCC_VDDIO0 to VCC_3V3 in this kit. Figure 3-8 shows the schematics of the voltage selection circuits.

Figure 3-8. Voltage Selection



3.2.5.3 *Current Measurement Headers*

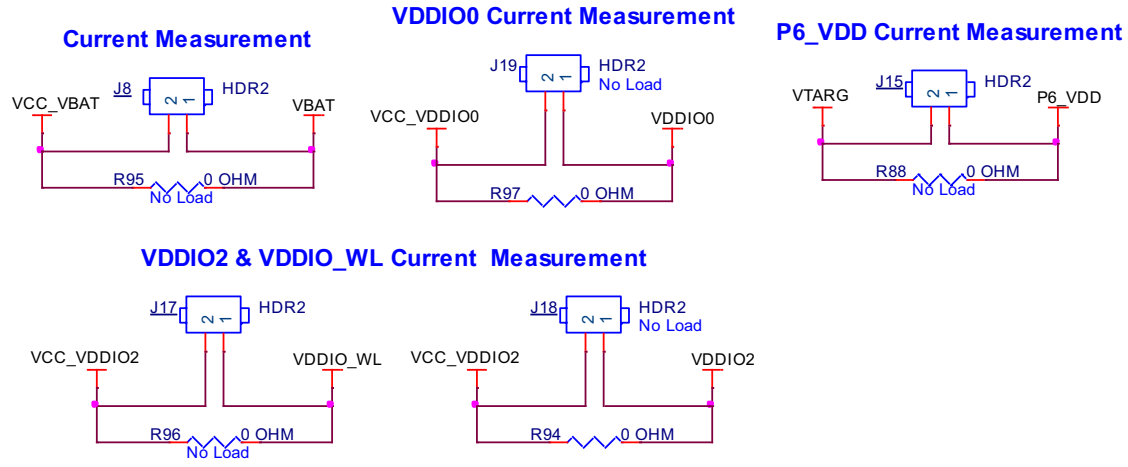
The current of the following domains have dedicated 2-pin headers to facilitate easy current measurement using an ammeter across the pins.

Note: If Header is not loaded by default, it is by-passed by a 0-ohm resistor parallel to it. Please make sure to remove the corresponding 0-ohm resistor (as per Figure 3-9) before measuring current across the header.

Table 3-2. Current Measurement Headers

Domain Name	Header Reference Designator	Loaded by default
VBAT	J8	Y
P6_VDD	J15	Y
VDDIO_WL	J17	Y
VDDIO2	J18	N
VDDIO0	J19	N

Figure 3-9. Current Measurement Headers



3.2.6 I/O Headers

3.2.6.1 Arduino-compatible Headers (J1, J2, J3, J4)

The board has four Arduino-compatible headers: **J1**, **J2**, **J3**, and **J4**. You can connect 3.3 V Arduino-compatible shields to develop applications based on the shield's hardware.

Note: 5-V shields are not supported and connecting a 5-V shield may permanently damage the board.

Note: All Arduino header pins are not connected to the same voltage reference. ARD_D[10:13] are powered by VDDIO0 whereas rest are powered by domains connected to VTARG. Hence arduino shields particularly that use ARD_D[10:13] must not be used if VTARG is 1.8V.

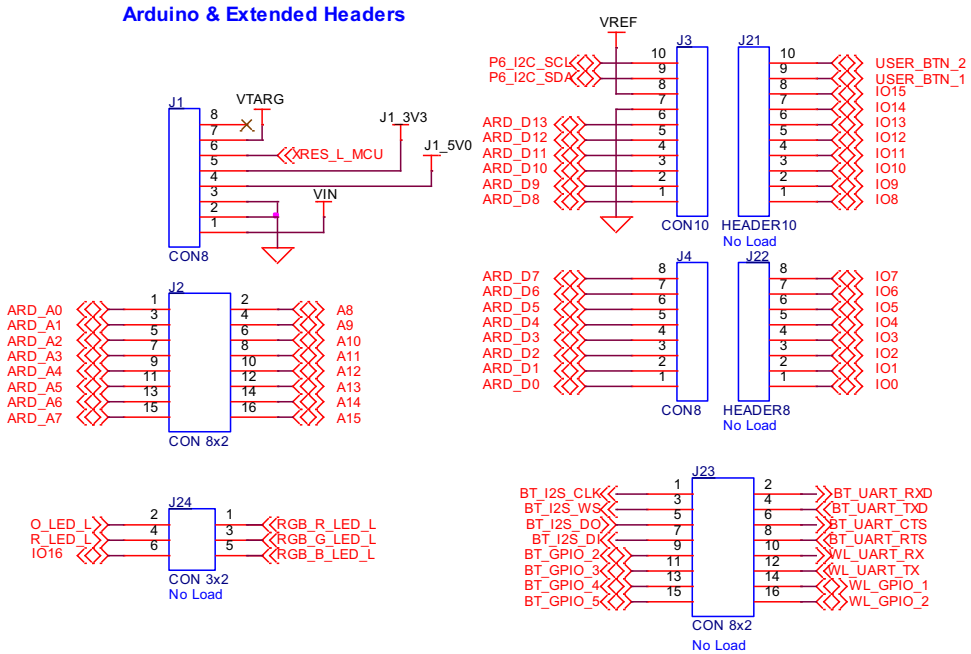
3.2.6.2 PSoC 6 MCU I/O Headers (J21, J22, and J24)

These headers provide connectivity to PSoC 6 MCU GPIOs that are not connected to the Arduino-compatible headers. Majority of these pins are multiplexed with onboard peripherals and are not connected to PSoC 6 MCU by default.

3.2.6.3 WL/BT I/O Headers (J23)

These headers provide connectivity to a few of the CYW43012 GPIOs that are available at the castellated pads. All these I/O work at VDDIO_WL voltage (1.8 V by default).

Figure 3-10. I/O Headers



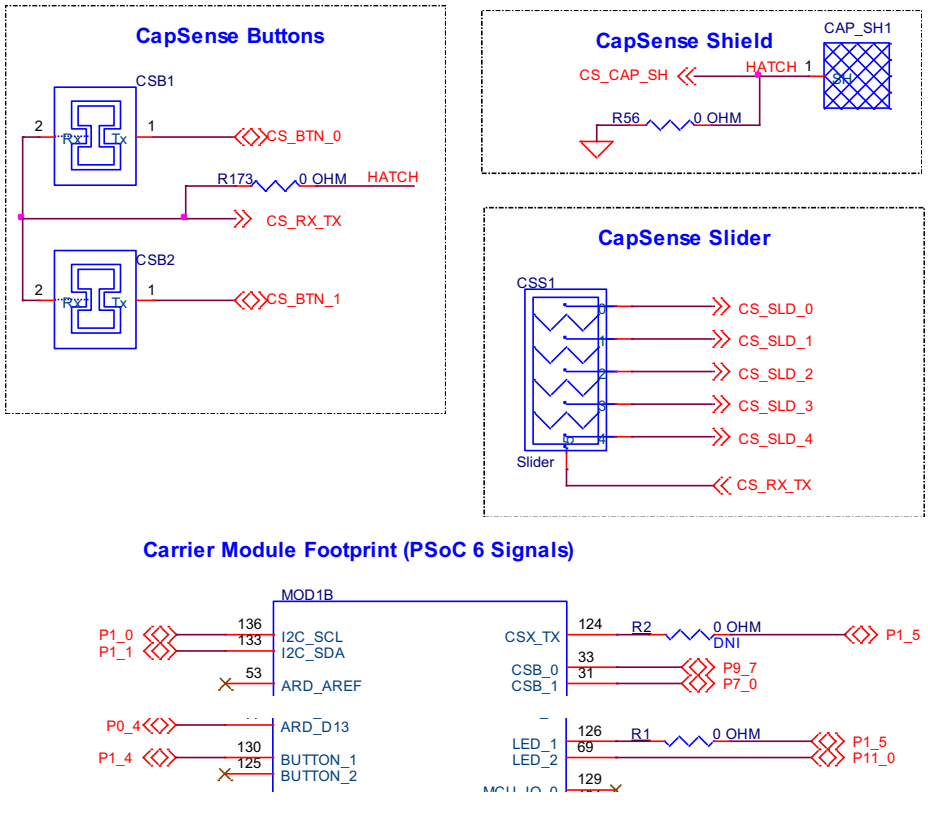
3.2.7 CapSense Circuit

A CapSense slider and two buttons, all supporting both self-capacitance (CSD) and mutual-capacitance (CSX) sensing are connected to PSoC 6 MCU as Figure 3-11 shows. Three external capacitors - CMOD for CSD, CINTA and CINTB for CSX - are present on the CYW9P62S1-43012CAR-01. For details on using CapSense including design guidelines, see the Getting Started with CapSense Design Guide.

Note: CSX is not supported by default, Remove R173 on the baseboard and R1 on the Carrier Module and load R2 on the carrier module to enable CSX.

Note that CapSense Shield functionality is not available on this kit.

Figure 3-11. Schematics of CapSense Circuit



Simultaneous GPIO switching with unrestricted drive strengths and frequency can affect CapSense and ADC performance. For more details, see the Errata section of the corresponding device datasheet.

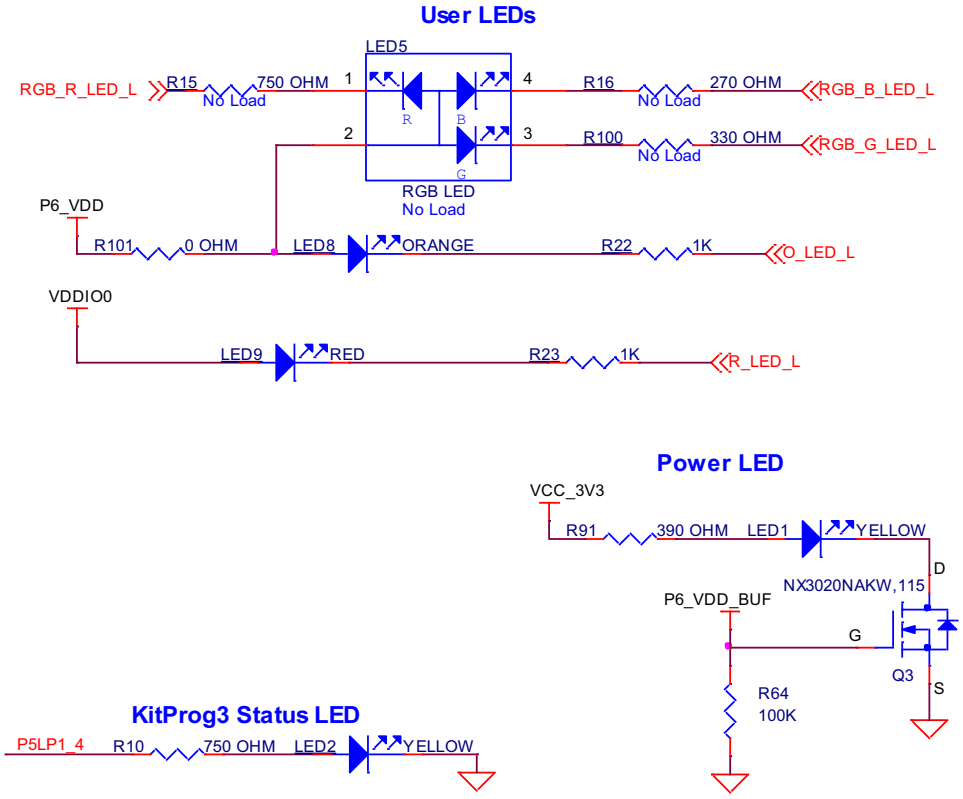
3.2.8 LEDs

LED2 (Yellow) indicates the status of KitProg3 (See the KitProg3 User Guide for details). **LED1** (Yellow) indicates the status of the power supplied to the board.

The board also has two user-controllable LEDs (**LED8** and **LED9**) connected to PSoC 6 MCU pins for user applications.

Note: The RGB LED is not loaded on this kit.

Figure 3-12. LEDs

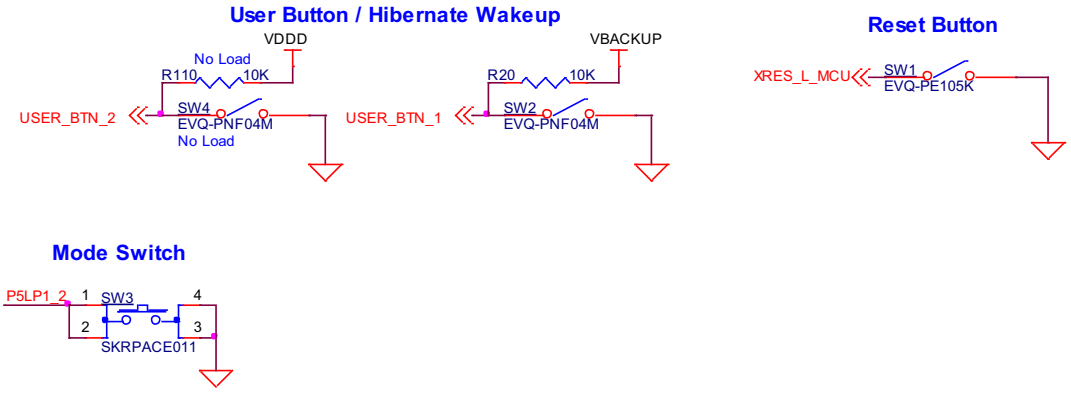


3.2.9 Push Buttons

The board has a reset button, one user-controllable button and a KitProg3 Mode selection button. The reset button (**SW1**) is connected to the XRES pin of the PSoC 6 MCU and is used to reset the device. A user button (**SW2**) is connected to pin P1[4] of the PSoC 6 MCU. The Mode selection button (**SW3**) is connected to the PSoC 5LP device for programming mode selection (Refer to the KitProg3 User Guide for details). All buttons are active LOW configuration and short to GND when pressed. The CYW9P62S1-43012CAR-01 has a pull-up on the PSoC 6 MCU XRES line.

Note: SW4 is not loaded on this kit.

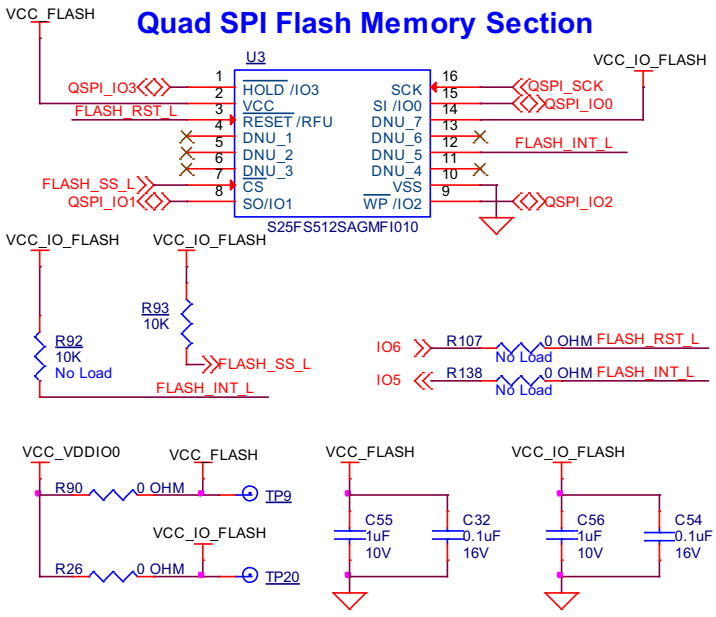
Figure 3-13. Schematics of Push Buttons



3.2.10 Cypress Quad SPI NOR Flash

The PSoC 62S1 Wi-Fi BT Pioneer Board has a Cypress NOR flash memory (S25FS512SAGM-FI010) of 512Mb capacity. The NOR flash is connected to the Quad SPI interface of the PSoC 6 MCU device. The NOR flash device can be used for both data and code with execute-in-place (XIP) support and encryption.

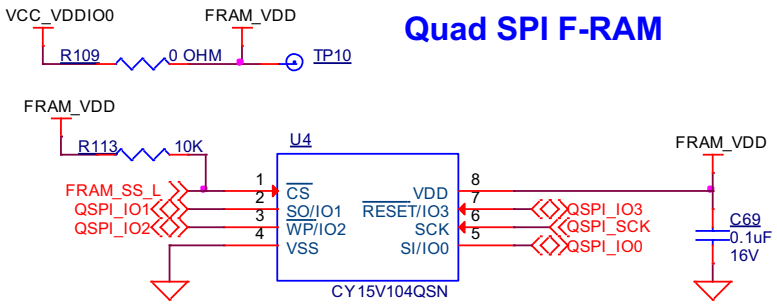
Figure 3-14. Schematics of QSPI Flash



3.2.11 Cypress Quad SPI F-RAM

The PSoC 62S1 Wi-Fi BT Pioneer Board contains the CY15V104QSN Excelon™ F-RAM device, which can be accessed through Quad SPI interface. The F-RAM is 4-Mbit (512K × 8) and is capable of Quad SPI speed up to 108 MHz but on this kit it is limited to 75 MHz.

Figure 3-15. Schematics of Quad SPI F-RAM

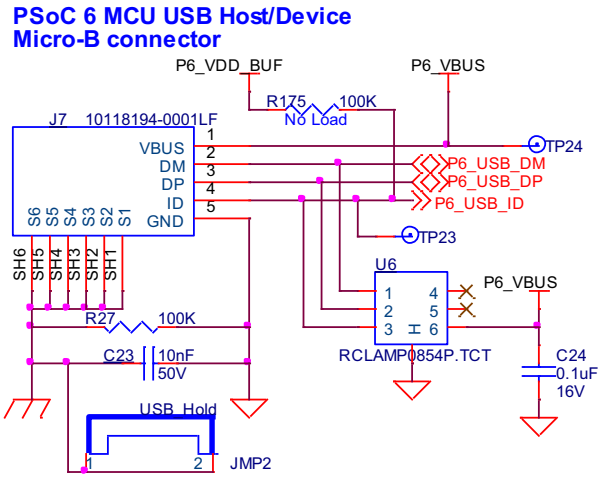


3.2.12 PSoC 6 USB

The board contains a micro-B USB connector for PSoC 6 MCU. In this kit, it is capable of USB device functionality only.

USB Host functionality is not supported on this kit.

Figure 3-16. PSoC 6 USB

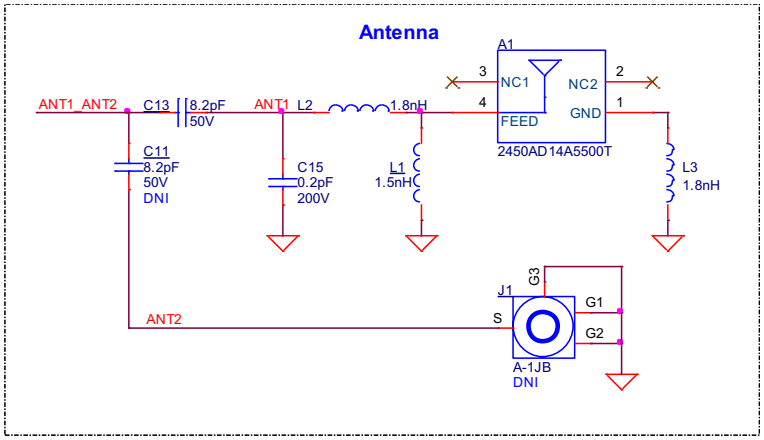


3.3 PSoC 62S1 Wi-Fi BT Pioneer Kit Rework

3.3.1 U.FL (UMCC) Connector for External Antenna

The RF output of CYW43012 is connected to the chip antenna by default. To disconnect the chip antenna and connect an external antenna, remove C13 and populate C11, J1 on CYW9P62S1-43012CAR-01.

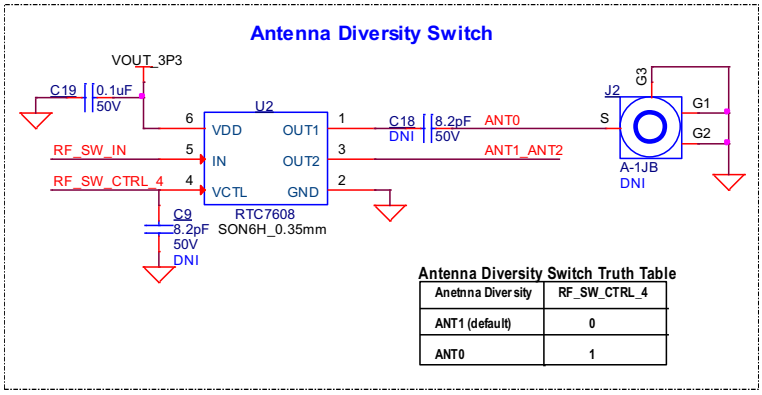
Figure 3-17. Schematics of U.FL (UMCC) Connector for External Antenna



3.3.2 U.FL (UMCC) Connector for Antenna Diversity

To evaluate antenna diversity, an external antenna can be connected to the output of antenna diversity RF switch. Populate C18 and J2 on CYW9P62S1-43012CAR-01 for the same.

Figure 3-18. Schematics of U.FL (UMCC) Connector for Antenna Diversity



3.4 Bill of Materials

Refer to the BOM files in the kit webpage.

3.5 Frequently Asked Questions

1. How does CYW9P62S1-43012EVB-01 handle a voltage connection when multiple power sources are plugged in?

   There are three different options to power the baseboard; KitProg3 Micro-B USB connector (**J6**), PSoC 6 Micro-B USB connector (**J7**), and External DC supply via VIN connector (**J5**). The voltage from each of the sources in passed through ORing diodes that supply VCC_IN.

2. What are the input voltage tolerances? Is there any overvoltage protection on this kit?

   Input voltage levels are as follows:

Table 3-3. Input voltage levels

Supply	Typical I/P Voltage	Absolute max
USB Micro-B connector **(J6, J7)**	4.5 V to 5.5 V	5.5 V
VIN connector **(J5)**	7 V to 12 V	18 V

   There is no overvoltage protection on this kit.

3. I am unable to program the target device.
   a. Check **J15** to ensure that jumper shunt is placed.
   b. Make sure that no external devices are connected to the external programming header J11.
   c. Update your KitProg3 version to the latest one using the steps mentioned in the KitProg3 User Guide.

4. What additional overlays can be used with the CapSense?

   Any kind of overlays (up to 5-mm thickness) like wood, acrylic, and glass can be used with CapSense. Note that additional tuning may be required when the overlay is changed.

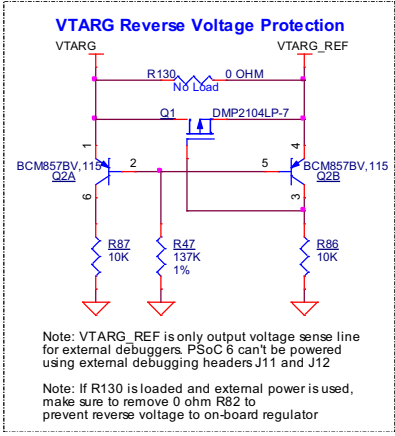
5. Can I power the kit using external program/debug headers J11 and J12?

   No, this is not possible by default in this board. The target MCU is powered by on-board regulators only and hence one of the 3 main sources (**J5**, **J6** and **J7**) must be present.

   There is a protection circuit that prevents reverse voltage from VTARG_REF to VTARG. Hence the board can't be powered through **J11** and **J12**. However this can be by-passed by loading R130.

   Note: This modification is not recommended as the target MCU will have no protection and will be permanently damaged if 5V is supplied.

Figure 3-19. VTARG Reverse Voltage Protection



Revision History

Document Revision History

Document Title: CYW9P62S1-43012EVB-01 PSoC 62S1 Wi-Fi BT Pioneer Kit Guide Document Number: 002-28722			
Revision	**ECN Number**	**Issue Date**	**Description of Change**
**	6707976	12/17/2019	New kit guide.
*A	6768042	01/07/2020	Updated Hardware chapter on page 26: Updated "Hardware Functional Description" on page 26: Updated "CYW9P62S1-43012CAR-01 (MOD1)" on page 26: Added hyperlinks in required places.
*B	6776820	01/16/2020	Updated Hardware chapter on page 26: Updated "Hardware Functional Description" on page 26: Updated "CYW9P62S1-43012CAR-01 (MOD1)" on page 26: Updated Figure 3-1.