ISM95 Series

Product Feature:

Low Jitter, Non-PLL Based Output CMOS Compatible Logic Levels Compatible with Leadfree Processing Applications: Fibre Channel Server & Storage Sonet/SDH 802.11/Wifi T1/E1, T3/E3

| | System Clock | | | |
|---|--|--|--|--|
| Frequency Range | 1.000 MHz to 156.250 MHz | | | |
| Frequency Stability (Inclusive of Calibration Tolerance at 25°C, Frequency Stability over Operating Temperature Range, Supply Voltage Change, Output Load Change, and First Year Aging at 25°C) | ±10ppm Maximum ±15ppm Maximum ±20ppm Maximum ±25ppm Maximum ±50ppm Maximum ±100ppm Maximum | | | |
| Operating Temperature Range | 0°C to +70°C, -10°C to +60°C, -10°C to +70°C, -20°C to +70°C, -30°C to +75°C, or -40°C to +85°C | | | |
| Supply Voltage (Vdd) (±5%) | 1.8V, 2.5V, 2.7V, 3.0V, 3.3V, 1.62V - 3.63V | | | |
| Input Current | 20mA Maximum | | | |
| Output Logic Type | CMOS | | | |
| Output Drive Capability | 15pF Maximum 30pF Maximum | | | |
| Aging | ±3ppm/year Maximum | | | |
| Duty Cycle (Measured at 50% of waveform) | 50 ±5(%) or 50 ±10(%) | | | |
| Rise / Fall Time (Measured from 20% to 80% of waveform) | 6nSec Maximum | | | |
| Output Voltage Logic High | 90% of Vdd Minimum | | | |
| Output Voltage Logic Low | 10% of Vdd Maximum | | | |
| Pin 1 Connection | Tri-State (High Impedance) | | | |
| Input Voltage Logic High | 70% of Vdd Minimum or No Connect to Enable Output | | | |
| Input Voltage Logic Low | 30% of Vdd Maximum to Disable Output (High Impedance) | | | |
| Standby Current (Disabled Output, High Impedance) | 10μΑ Maximum | | | |
| Startup Time | 10mSec Maximum | | | |
| RMS Phase Jitter (12kHz to 20MHz offset frequency) | 1pSec Maximum | | | |
| Period Jitter (RMS) (20k adjacent periods) | 5pSec Maximum | | | |
| Period Jitter (pk-pk) (100k adjacent periods) | 50pSec Maximum | | | |



•All minimum and maximum limits are specified over temperature and rated operating voltage with 15pF output unless otherwise stated.

 $\bullet \dot{A}$ 0.1µF bypass capacitor is recommended between Vdd (pad 4) and GND (pad 2) to minimize power supply noise.





| Pin | Connection |
|-----|-------------------------|
| 1 | Tri-State or No Connect |
| 2 | Case/Ground |
| 3 | Output |
| 4 | Supply Voltage |

All Dimensions in Millimeters



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Absolute Maximum Limits:

| Storage Temperature Range | -55°C to +125°C |
|---------------------------|------------------------|
| Supply Voltage Range | -0.3Vdc to Vdd +0.3Vdc |
| Electrostatic Discharge | 2000V Maximum |
| Solder Temperature | 260°C Maximum |
| Junction Temperature | 150°C Maximum |

Environmental Specifications:

| Mechanical Shock | MIL-STD-202, Method 213 |
|------------------------------|--------------------------|
| Mechanical Vibration | MIL-STD-202, Method 204 |
| Resistance to Soldering Heat | MIL-STD-202, Method 210 |
| Solderability | J-STD-002 |
| Gross Leak | MIL-STD-883, Method 1014 |
| Fine Leak | MIL-STD-883, Method 1014 |
| Moisture Sensitivity Level | MSL 1 (+260°C) |

Test Circuit: Enable/Disable Option



Waveform: Enable/Disable Option



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Pb Free Solder Reflow Profile:



| Ts max to T∟ (Ramp-up Rate) | 3ºC / second max | | |
|-------------------------------|--------------------------|--|--|
| Preheat | | | |
| Temperature min (Ts min) | 150°C | | |
| Temperature typ (Ts typ) | 175°C | | |
| Temperature max (Ts max) | 200°C | | |
| Time (Ts) | 60 to180 seconds | | |
| Ramp-up Tate (T⊾ to Tp | 3°C / second max | | |
| Time Maintained Above | | | |
| Temperature (T _L) | 217°C | | |
| | 60 to 150 seconds | | |
| Peak Temperature (Tp) | 260°C max for 10 seconds | | |
| Time within 5°C to Peak | 20 to 40 secondo | | |
| Temperature (Tp) | 20 to 40 seconds | | |
| Ramp-down Rate | 6ºC / second max | | |
| Tune 25°C to Peak Temperature | 8 minutes max | | |

Package Information:

Termination = e4 (Au over Ni over W base metallization). Terminal Plating Thickness: Gold (0.3μ m to 1.0μ m), Nickel (1.27μ m to 8.89μ m)

Tape and Reel Information:



| Part Number Guide Sample Pa | | art Number: ISM95 - 3251BH - 20.000 MHZ | | | | | |
|-----------------------------|-------------------|---|--------------------------|----------------------------|-----------------------|---------------------|-------------|
| Package | Input Voltage | Operating Temperature | Symmetry (Duty Cycle) | Output Drive Capability | Stability (in ppm) | Enable / Disable | Freaquency |
| ICMOS | 3 = 3.3 V | 1 = 0° C to +70° C | 5 = 45 / 55 Max. | 1 = 15 pF | A = ±25 | H = Enable | -20.000 MHz |
| 131/190 - | 7 = 3.0 V | 8 = -10° C to +60° C | 6 = 40 / 60 Max. | 6 = 30 pF | B = ±50 | O = N/C | |
| | 2 = 2.7 V | 6 = -10° C to +70° C | | | C = ±100 | | |
| | 6 = 2.5 V | 3 = -20° C to +70° C | | | D = ±15 | | |
| | 1 = 1.8 V | 4 = -30° C to +75° C | | | E = ±10 | | |
| | 8 = 1.62V – 3.63V | 2 = -40° C to +85° C | | | F = ±20 | | |