



Product Change Notification / SYST-05HTVW873

Date:

07-Dec-2022

Product Category:

Microprocessors

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAMA5D2 Series

Affected CPNs:

[SYST-05HTVW873_Affected_CPN_12072022.pdf](#)

[SYST-05HTVW873_Affected_CPN_12072022.csv](#)

Notification Text:

SYST-05HTVW873

Microchip has released a new Datasheet for the SAMA5D2 Series of devices. If you are using one of these devices please read the document located at [SAMA5D2 Series](#).

Notification Status: Final

Description of Change: Revision includes:

Global

- Editorial changes throughout.

Power Management Controller (PMC)

- Main Clock Source Selection: updated naming to ULP1 mode.
- CKGR_MOR: updated naming to ULP1 mode.
- CKGR_MCFR: updated access for MAINF.
- PMC_SR: updated access for XT32KERR.

DDR-SDRAM Controller (MPDDRC)

- Renamed and updated Bus Monitor, Performance Monitor

Static Memory Controller (SMC)

- HSMC_ELPRIM, HSMC_MODE, HSMC_PMECCx: updated reset values.
- HSMC_MODE: added PS field.

DMA Controller (XDMAC)

- Description: updated.
- XDMAC_CC: updated reset value.

Gigabit Ethernet MAC (GMAC)

- Receive Buffer List: updated.
- Transmit Buffer List: updated.
- GTSUCOMP External Connection: updated.

USB Device High-Speed Port (UDPHS)

- 40.6.9. Transfer Without DMA: modified code content.

Synchronous Serial Controller (SSC)

- Audio Sampling Rate Limitations: added.
- SSC_WPMR: updated WPEN bit description.

Two-Wire Interface (TWIHS)

- Asynchronous Partial Wake-Up: updated.

Flexible Serial Communication Controller (FLEXCOM)

- Updated:
 - SPI Comparison Function on Received Character
 - SPI Asynchronous and Partial Wake-Up
 - TWI Asynchronous and Partial Wake-Up
- Bus Clear Command, FIFO Pointer Error, FLEX_TWI_CR: modified.
- FLEX_TWI_SR: updated reset value

Quad Serial Peripheral Interface (QSPI)

- QSPI Bus Clock Modes: updated.

Secure Digital MultiMedia Card Controller (SDMMC)

- SDMMC_CAOR: added Note 2
- SDMMC_PSR: modified reset value

Image Sensor Controller (ISC)

- Index 16:31 now 'reserved' in:
 - ISC_DST0
 - ISC_DST1
 - ISC_DST2
- Descriptor Memory Mapping: updated column "Address" in tables Table 51-4, Table 51-5, Table 51-6
- ISC_DCTRL: updated DVIEW description.

Pulse Width Modulation Controller (PWM)

- Fault Protection: figure updated.
- PWM_SMMR: updated.
- PWM_ETRGx, PWM_LEBRx: updated.

Advanced Encryption Standard (AES)

- Secure Protocol layers Improved Performances: updated.
- AES_MR: updated reset value.

Triple Data Encryption Standard (TDES)

- TDES_MR: updated reset value.

Analog Comparator Controller (ACC)

- Description, Embedded Characteristics: updated.

Analog-to-Digital Controller (ADC)

- Asynchronous Partial Wakeup: updated.
- ADC_EMR: updated.

Electrical Characteristics

- Absolute Maximum Ratings: added injected current information.
- DC Characteristics: added. VIL and VIH values updated.
- Table 66-5 to Table 66-8: added.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 07 Dec 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[SAMA5D2 Series](#)

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