Analog Devices Wiki

This version (12 Oct 2022 12:31) was *approved* by Ciprian Carbunaru [https://ez.analog.com/members/ccarbuna].
The Previously approved version (/resources/eval/user-guides/ad-synchrona14-ebz?rev=1662964557) (12 Sep 2022 08:35) is available.

This is an old revision of the document!

AD-SYNCHRONA14-EBZ User Guide

Overview

The **AD-SYNCHRONA14-EBZ** is an ideal self-contained device suitable for applications that require a highly accurate frequency and phase-controlled source clock. It is designed around the AD9545 [https://www.analog.com/AD9545], a quad input synchronizer and jitter cleaner, and the HMC7044 [https://www.analog.com/HMC7044], a 3.2 GHz (Gigahertz), 14-output high performance jitter attenuator. This board greatly simplifies clock distribution and multichannel synchronization in complex systems. Using popular industry connectors such as SMA and Samtec Circular RF Twinax [https://www.samtec.com/cables/high-speed/assemblies/shielded], most labs have cables that are compatible with this device. It is intended for use in a lab environment by trained professionals for evaluation and prototyping purposes and can be used as a reference design for integrating into custom applications.

With its on-board internal oven-controlled crystal oscillator (OCXO), the AD-SYNCHRONA14-EBZ can operate in standalone mode or be fed from a choice of external sources such as three separate high speed differential clock inputs, a 10 MHz (megahertz) reference, and a 1 pps input. This flexibility, combined with the capability to select either of the internal voltage-controlled crystal oscillator (VCXO) options of 100 MHz (megahertz) or 122.88 MHz (megahertz), gives almost unlimited choice for the frequency of interest and accuracy needed for a wide variety of application areas.

(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/synchrona_front.jpg?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz)

(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/synchrona_back.jpg?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 1. AD-SYNCHRONA14-EBZ Front and Back Panel*

Applications

- High accuracy reference clock distribution
- Systems clocked from a single source
- Use cases requiring 100 MHz (megahertz) or 122.88 MHz
- Phased array systems, radar, EW, SATCOMS
- Bench equipment
- Remote controlled operation

Key Features

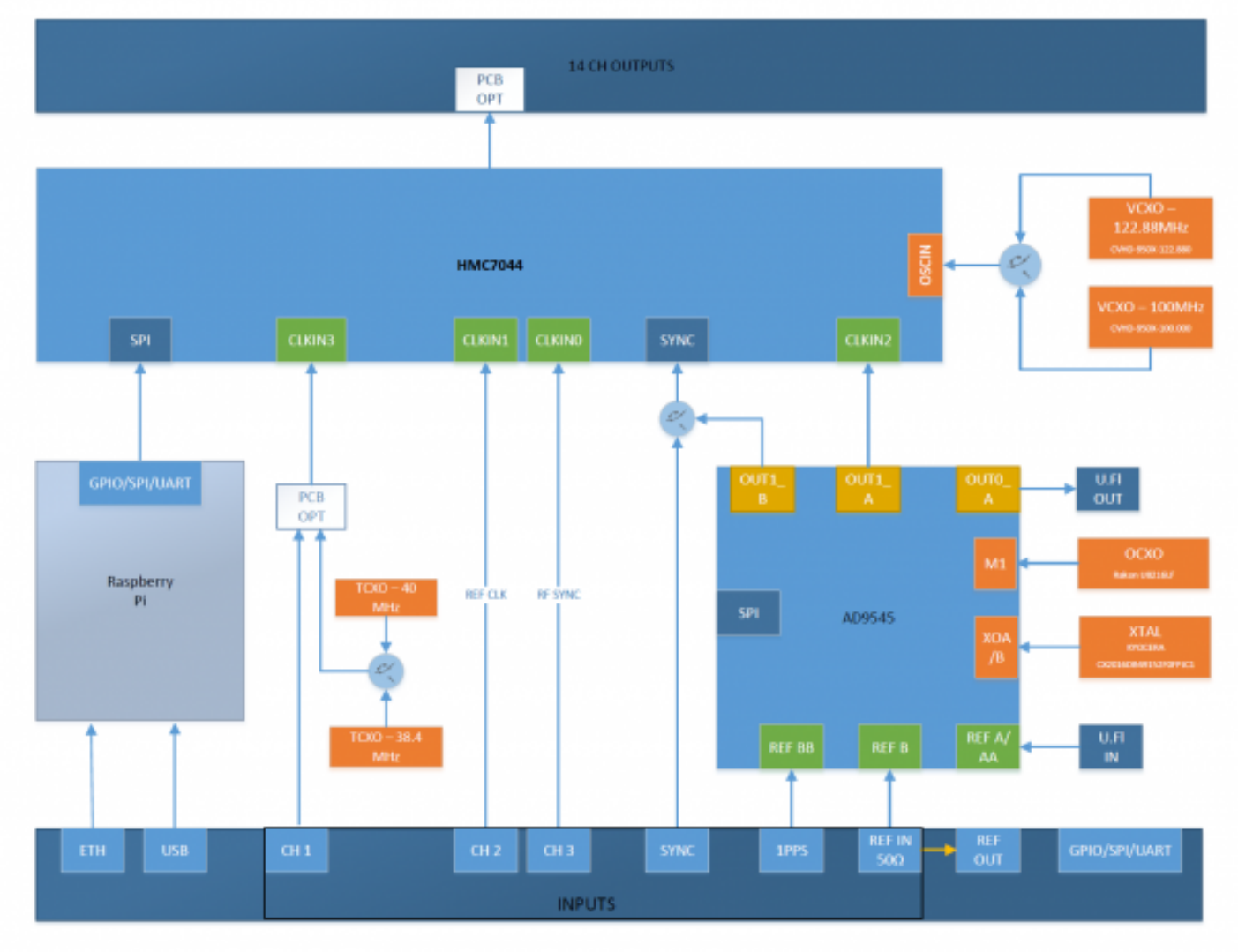
User Interfaces	Gigabit Ethernet Male pin header (SPI (Serial Peripheral Interface) & GPIO (General Purpose Input/Output)) USB (Universal Serial Bus) Status LEDs
Clock Inputs	3 differential 100 Ω SMA clock inputs 1 pps input SYNC input 10 MHz (megahertz) input
Clock Outputs	4 x Twinax LVPECL dc-coupled, 100 Ω 2 x SMA LVPECL ac-coupled* 4 x SMA CMOS* 4 x SMA LVDS ac-coupled* **Configurable differential outputs, 50 Ω diff*
Processing System	Raspberry Pi 4, ARM Cortex-A72, 2 GB (Gigabyte) SDRAM (synchronous dynamic random access memory (system memory))
Power Supply	DC 12V, 3A barrel jack
Internal References	100 MHz (megahertz) and 122.88 MHz (megahertz) ultralow phase noise VCXOs (-165 dBc (decibels relative to the carrier)/Hz) 40 MHz (megahertz) and 38.4 MHz (megahertz) TCXOs (±1 ppm) 50 MHz (megahertz) OCXO (±10 ppb) *Internal references are software configurable.*
Clock Processing Devices	HMC7044 (High performance, 3.2 GHz (Gigahertz), 14-output Jitter Attenuator) AD9545 (1 PPS Synchronizer and Adaptive Clock Translator)

Hardware

Power Supply

Use a 12 Volts dc power supply with a minimum power of 36 W and a 2.1 x 5.5 mm barrel jack.

Block Diagram



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/block_diagram.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 2. AD-SYNCHRONA14-EBZ Simplified Block Diagram*

Clock Output Configuration

There are a total of 14 high speed clocks that come out of the final clock mux; these can range from 2150 MHz (megahertz) to 3550 MHz (megahertz) in different modes and connection schemes. The maximum clock output is 2400 MHz (megahertz), which can be divided down by 1, 2, 3, 4, 5, 6, and even numbers up to 4094. Moreover, the output clock resolution depends on the "Clock Distribution Frequency", and the divider value.

The outputs are hardware configurable as **LVPECL**, **LVDS**, and **CMOS**.

Maximum Operating Frequency

LVPECL	2400 MHz (megahertz) (3 dB (decibel) bandwidth)
LVDS	1700 MHz (megahertz)

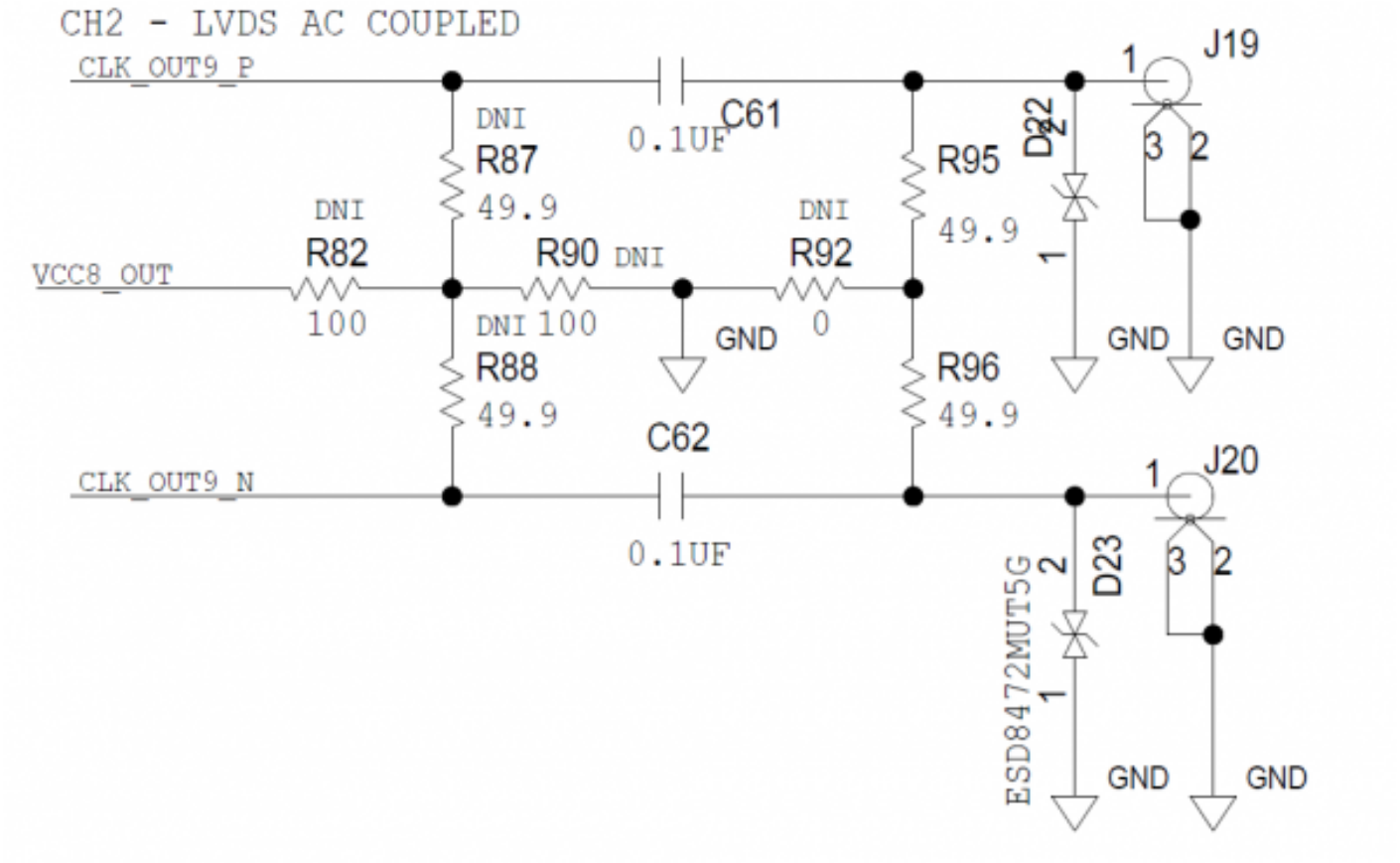
CMOS	600 MHz (megahertz)

The table below shows the default configuration:

HMC7044 Pin Name	Enclosure Designator	Board Connector Designator	Default Configuration
CLKOUT0	CH11	P6	LVPECL AC-COUPLED
CLKOUT1	CH12	P5	LVPECL AC-COUPLED
CLKOUT2	CH14	P3	LVPECL DC-COUPLED
CLKOUT3	CH13	P4	LVPECL DC-COUPLED
CLKOUT4	CH8	J9 (P), J11 (N)	CMOS
CLKOUT5	CH10	J12 (P), J15 (N)	LVPECL AC-COUPLED
CLKOUT6	CH6	J13 (P), J16 (N)	CMOS
CLKOUT7	CH4	J10 (P), J14 (N)	LVDS AC-COUPLED
CLKOUT8	CH1	J17 (P), J18 (N)	LVDS AC-COUPLED
CLKOUT9	CH2	J19 (P), J20 (N)	LVDS AC-COUPLED
CLKOUT10	CH3	J1 (P), J2 (N)	LVDS AC-COUPLED
CLKOUT11	CH5	J3 (P), J4 (N)	CMOS
CLKOUT12	CH9	J5 (P), J7 (N)	LVPECL AC-COUPLED
CLKOUT13	CH7	J6 (P), J8 (N)	CMOS

The default configuration can be changed. Each channel has all the footprints for the passive components.

```
Example: CH2 - LVDS ac-coupled
```



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/channel_configuration.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 3. AD-SYNCHRONA14-EBZ Channel Configuration*

For LVDS ac-coupled	Insert C61, C62 and R95, R96 for downstream devices with high impedance input.
For LVPECL ac-coupled	Insert C61, C62, R87, R88, R90, and then DNI the rest of the passive components.
For LVPECL dc-coupled	Replace C61 and C62 with 0 Ω resistors, insert R87, R88, R90, and then DNI the rest of the passive components.
For CMOS	Replace C61 and C62 with 0 Ω resistors, and then DNI the rest of the passive components.

Check the HMC7044 [https://www.analog.com/HMC7044] data sheet (page 21) for more details on output configuration.

100 Ω Differential Connectors

CH11, CH12, CH13, and CH14 are 100 Ω impedance differential outputs with circular RF Twinax Jack.

The CJT-BH connector series [https://www.samtec.com/products/cjt-bh] from Samtec are paired with C28S connector series [https://www.samtec.com/products/c28s] – Circular RF Twinax Cable Assembly.

Clock Input (Reference Input)

On the back panel, there are 3 differential 100 Ω inputs.
In the standard configuration, **CH1** is disconnected from the SMA connectors. The reason for this is that inside the AD-SYNCHRONA14-EBZ, there are two temperature-compensated crystal oscillators (TCXOs) connected to this channel (38.4 MHz (megahertz) and 40 MHz (megahertz)). To use the SMA cables, insert C69 and C70, and remove C282 and C134.

CH2 goes directly into HMC7044 [https://www.analog.com/HMC7044] and it is ac-coupled.
CH3 goes directly into HMC7044 [https://www.analog.com/HMC7044] and it is dc-coupled.
PPS is a CMOS input for 1 pps reference. The range for this input is from 1.8 V (volt) to 5 V (volt).
SYNC is a 3.3 V (volt) CMOS input that goes directly into HMC7044 [https://www.analog.com/HMC7044] sync pin.
REF_IN is a 50 Ω input with a maximum input power of 10 dBm (decibels relative to 1 milliwatt). With the standard software version, this input is set to function with a 10 MHz (megahertz) reference. The maximum input frequency is 160 MHz (megahertz) (–3dB).
REF_OUT is a CMOS output of the REF_IN buffer.

Internal References

There are two **VCXOs**, ultralow phase noise oscillators (-165 dBc (decibels relative to the carrier)/Hz).

The VCXOs are 100 MHz (megahertz) and 122.88 MHz (megahertz); both of which are software selectable and used to drive the PLL2 of HMC7044 [https://www.analog.com/HMC7044].

There are also two **TCXOs** (±1 ppm), 40 MHz (megahertz) and 38.4 MHz (megahertz) that can be used as reference for PLL1 of HMC7044 [https://www.analog.com/HMC7044].

Switching between VCXOs goes together with switching the TCXOs; 100 MHz (megahertz) with 40 MHz (megahertz), and 122.88 MHz (megahertz) with 38.4 MHz (megahertz).

The AD9545 [https://www.analog.com/AD9545] has a **50 MHz (megahertz) OCXO** (±10 ppb) reference, so AD-SYNCHRONA14-EBZ can be used as a standalone device, providing high frequency stability.

Software

Drivers

HMC7044 Clock Jitter Attenuator with JESD204B Linux Driver (/resources/tools-software/linux-drivers/iio-pll/hmc7044)

AD9545 Quad Input, 10-Output, Dual DPLL/IEEE 1588, 1 pps Synchronizer and Jitter Cleaner (/resources/tools-software/linux-drivers/clk/adi/clk-ad9545.c)

GUI

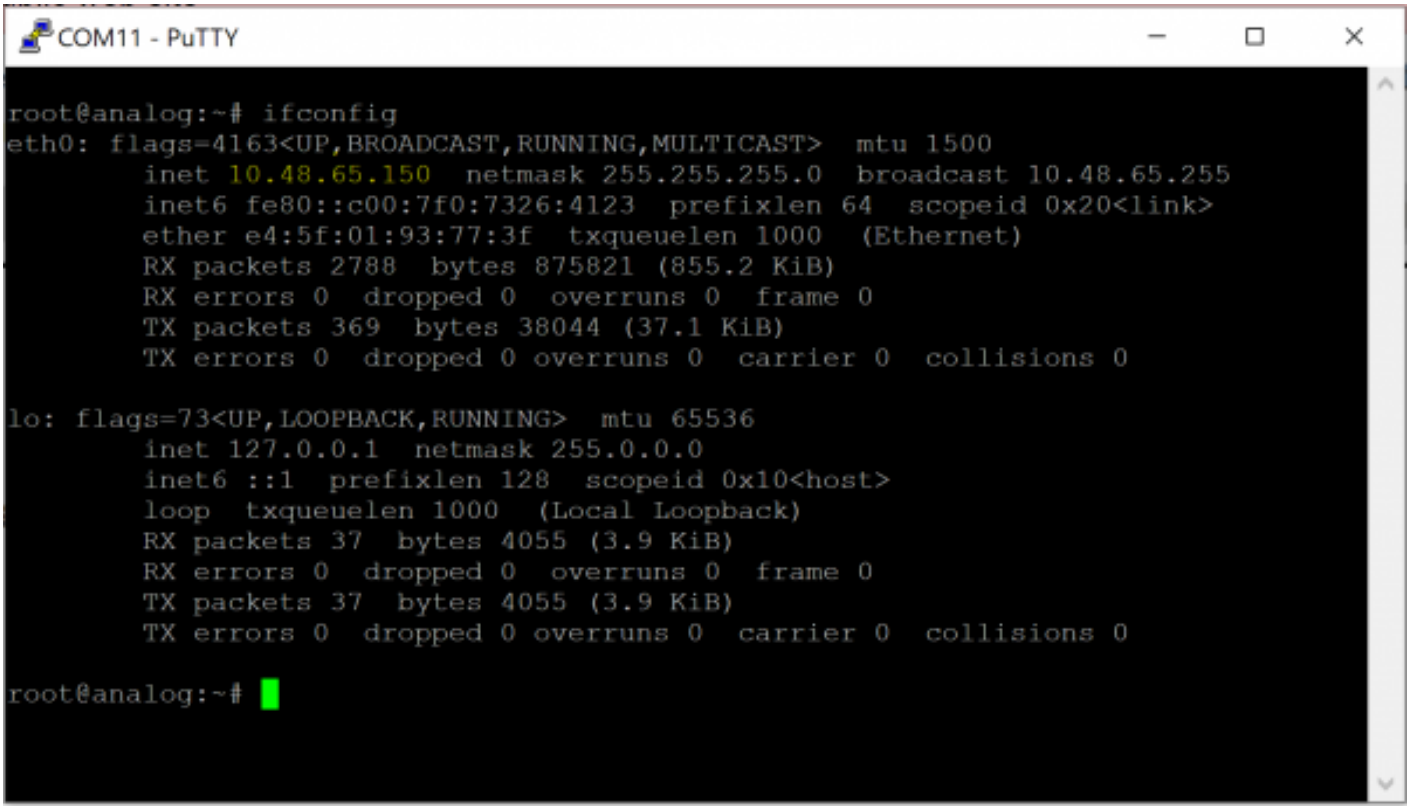
The Raspberry Pi inside AD-SYNCHRONA14-EBZ runs the **RaspAP**, which is an application that gives access to the GUI (Graphical User Interface).

- To access the GUI (Graphical User Interface), the user must first get the IP of the device.
- In the default configuration, AD-SYNCHRONA14-EBZ has the IP set as static **192.168.2.1**

Make sure that you are using an IP in the same class on your PC.

If AD-SYNCHRONA14-EBZ has a DHCP (Dynamic Host Configuration Protocol) setting, follow these steps to configure correctly:

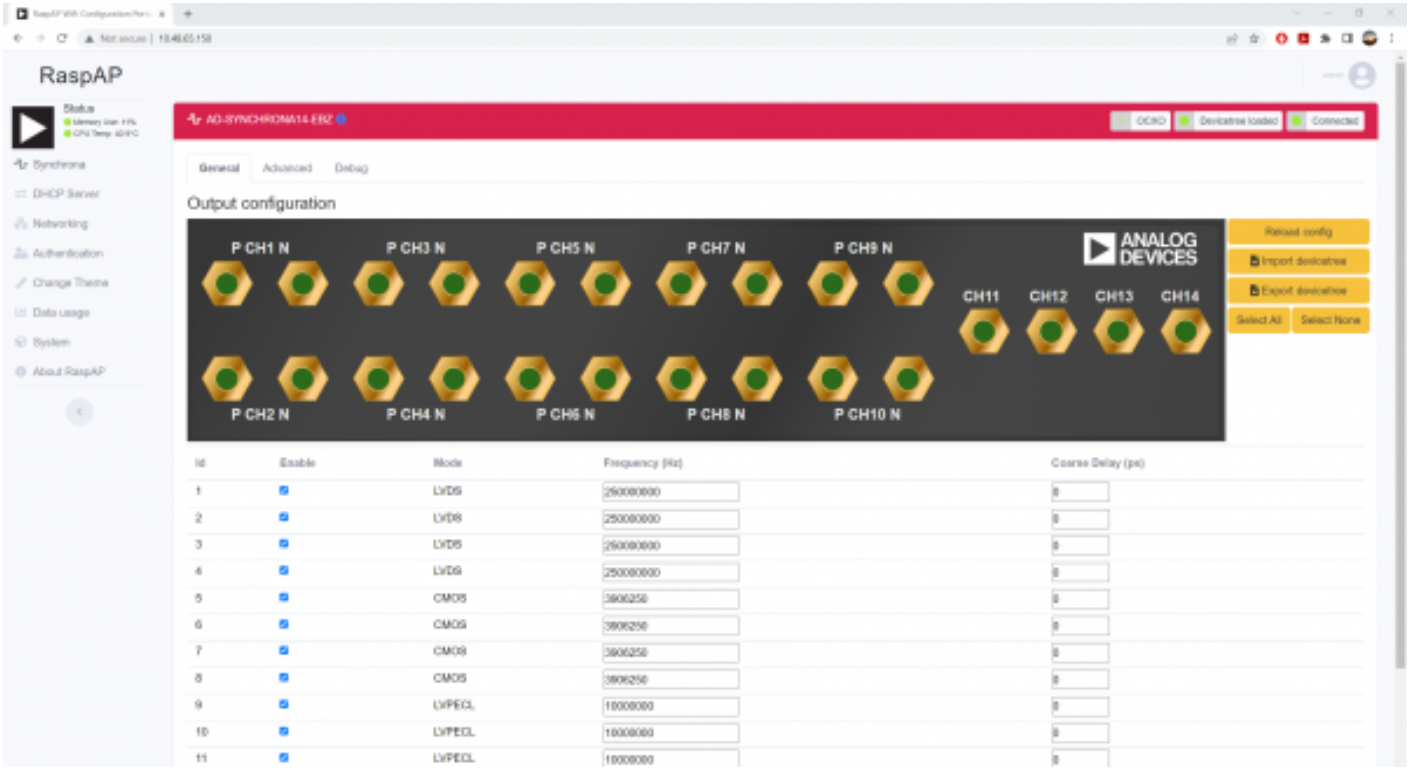
1. Use a Network Discovery tool or connect the add-on board in the back to the GPIO (General Purpose Input/Output) port. This will give access to the UART (universal asynchronous receiver/transmitter) port of the Raspberry Pi.
2. Open a terminal (PuTTY).
3. Select the COM and 115200 baud rate.
4. After opening the terminal, type in **ifconfig**. This command will return the IP of the device (eth0: inet 10.48.65.150).
5. Once you have the correct IP, type it in your browser to access the GUI (Graphical User Interface). The default username is **admin** and the password is **analog**.



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/putty_terminal.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 4. PuTTY Terminal View*

General Page

The General Page of the GUI (Graphical User Interface) allows users to enable/disable channels, and set the frequencies on each channel. Refer to the **Clock Output Configuration** section above for the proper settings.



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/gui_general.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 5. GUI (Graphical User Interface) - General Page View*

There are two VCXOs inside the AD-SYNCHRONA14-EBZ. Based on the frequencies you set in the General Page, the switch between the two VCXOs will be done automatically and the PLL (Phase Locked Loop) frequency will be calculated.

The values on each channel need to be submultiples of the PLL (Phase Locked Loop) frequency.

If one or more of the values cannot be obtained from dividing the PLL (Phase Locked Loop) frequency, the GUI (Graphical User Interface) will return the message:

> **Invalid Frequencies: Cannot solve HMC7044 clock configuration….**

To apply the settings you made, click on the **Reload Config** button.

Coarse delay is another feature you can find in the **General Page**. Coarse delay can be set in step that are calculated based on the VCO frequency. Use the arrows in the coarse delay field to modify the coarse delay. The value is set in picoseconds. This feature can be used to compensate for unmatched RF cables.

Id	Enable	Mode	Frequency (Hz)	Coarse Delay (ps)
1	☑	LVDS	10000000	200
2	☑	LVDS	10000000	400

(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/coarse_delay.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 6. Coarse Delay Settings Menu*

In the General Page, users can see three status icons (left to right):

- The first icon indicates the reference that AD-SYNCHRONA14-EBZ is using;
- The second icon indicates if the devicetree is loaded; and
- The third icon indicates if the device is connected.

To know the updated status, click on the status icons, as shown below.

(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/status_icons.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 7. AD-SYNCHRONA14-EBZ Status Icons*

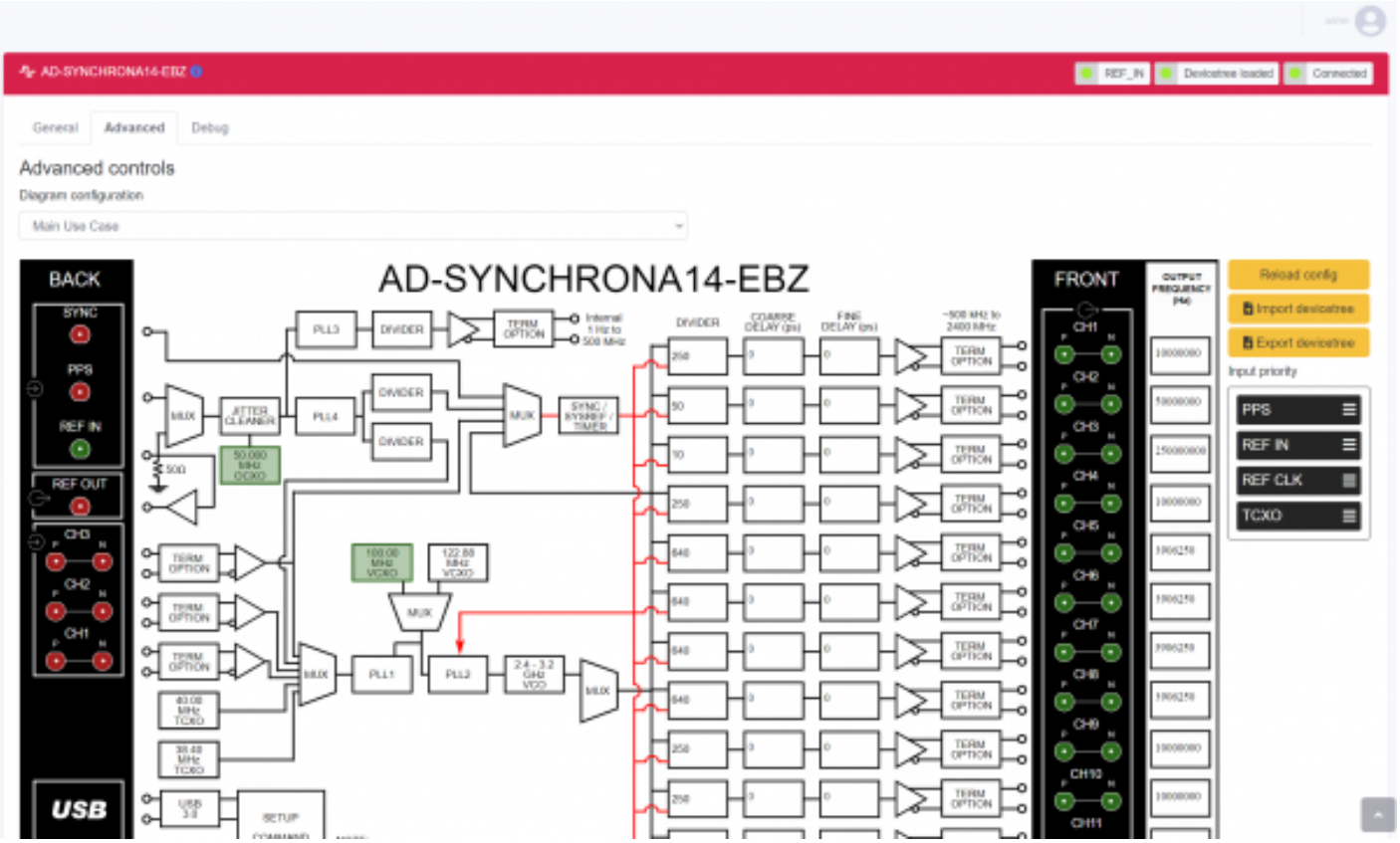
In the General Page, you also have access to importing and exporting a **devicetree** with your settings.

- When importing a devicetree, make sure that the name of the file is **rpi-ad9545-hmc7044.dtbo**
- After importing a devicetree, click on **Reload Config** to apply the settings.

Advanced Page

In the Advanced Page of the GUI (Graphical User Interface), you can find a detailed block diagram of AD-SYNCHRONA14-EBZ.

As shown in the illustration below, you can see the VCXO that is being used (highlighted in green). Also, the valid inputs on the left side are highlighted in green. In this case, a 10 MHz (megahertz) reference is connected into REF_IN.



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/gui_advanced.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 8. GUI (Graphical User Interface) - Advanced Page View*

Input Priority

The input priority table is used to prioritize the input references.

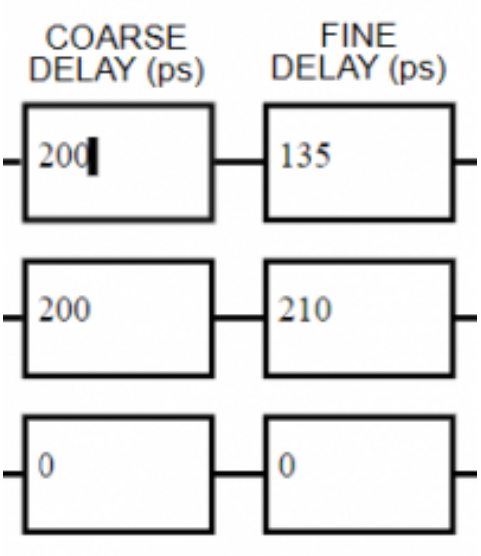
- Set the input priority table by dragging each reference upwards or downwards, as shown in the figure below:

(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/input_table.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 9. Input Priority Menu*

- Click on **Reload Config** to apply the changes.
- If one of the references is invalid, AD-SYNCHRONA14-EBZ will jump automatically to the next valid reference.

Coarse Delay & Fine Delay

Coarse delay and fine delay settings are also available in the **Advanced Page**.

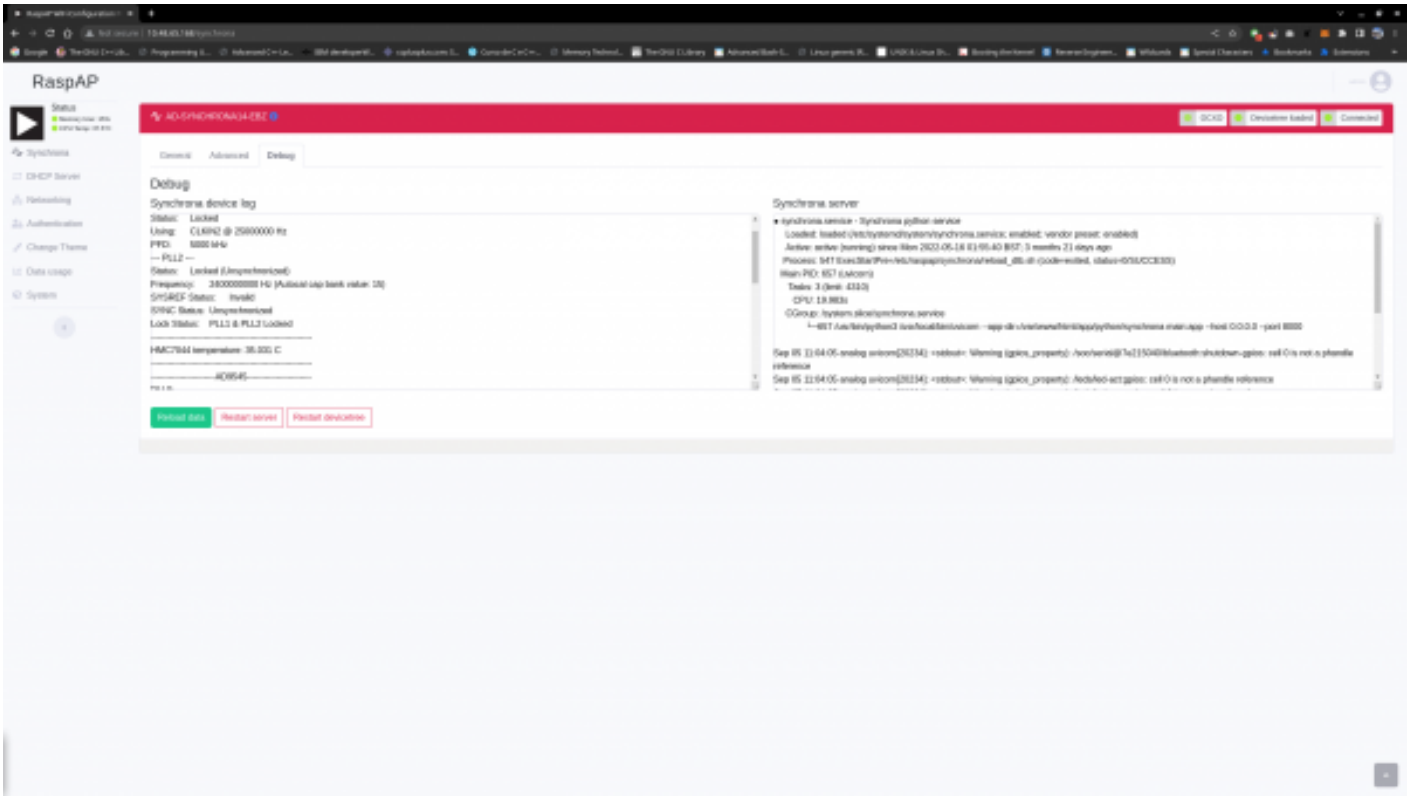


(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/fine_delay.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 10. Coarse and Fine Delay Settings Menu*

- Use the arrows to set the coarse and the fine delay.
- Click on **Reload Config** to apply the changes.

Debug Page

This page features various debug information. On top of this, more actions are available for users' access, as shown in the illustration below:



(/_media/resources/eval/user-guides/ad-synchrona14-ebz/synchrona_debug.png) *Figure 11. Debug Page View*

Features Available in Debug Page	Function
Synchrona device log	This panel presents various information about the **clock chips,** including a special note for the lock status of the various PLLs, which can be handy in ensuring that the **input reference status** displayed in the status LED is coherent. This information, together with the Input Priority list (displayed in the advanced page), is also useful to make sure the expected reference is, in fact, being used.
Synchrona server	This panel displays the status of the Synchrona server running on the device.
Restart server	This button restarts the Synchrona server.
Restart devicetree	This button basically brings the device to its default configuration after installation.
Reload data	This button reloads all debug logs and configurations into the GUI (Graphical User Interface). Note that this function does not change device configuration.

Use Cases

Standalone Use Case

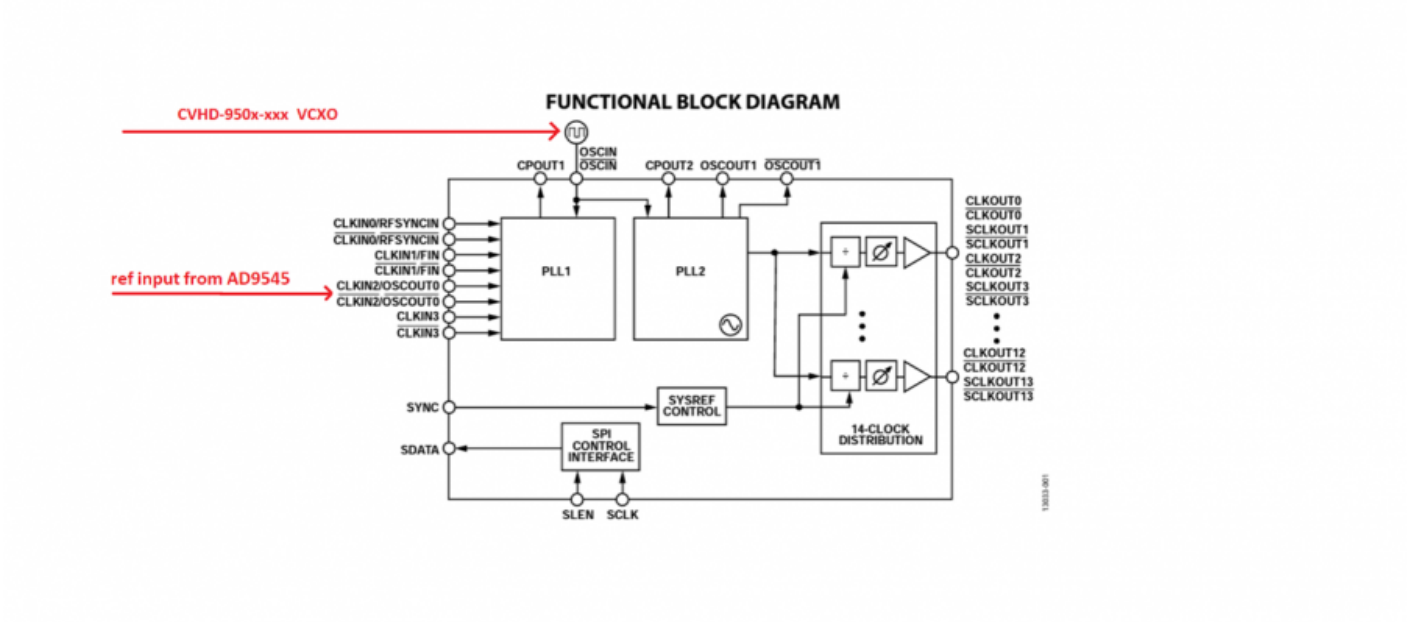
The AD-SYNCHRONA14-EBZ can be used as a standalone device without the need of an external clock reference.

Inside the AD-SYNCHRONA14-EBZ, there is a Raspberry Pi connected to all the clock ICs that run all the drivers.

In the standalone use case, the main clock reference is the 50 MHz (megahertz) OCXO (Rakon U8216LF)

that feeds the AD9545 [https://www.analog.com/AD9545] clock IC. The 50 MHz (megahertz) OCXO used in this design has a frequency stability over temperature of ±10 ppb, and a warm up time of about 60 seconds for the reference frequency to be within ±20 ppb.

The AD9545 [https://www.analog.com/AD9545] can provide any clock frequency up to 500 MHz (megahertz). The differential output OUT1_A of the AD9545 [https://www.analog.com/AD9545] is connected directly (ac-coupled) to PLL1 reference input (CLKIN2) of HMC7044 [https://www.analog.com/HMC7044]. The reference input to PLL2 of HMC7044 [https://www.analog.com/HMC7044] is connected via an RF switch to two ultralow phase noise VCXOs.



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/hmc-refin.png?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 12. AD-SYNCHRONA14-EBZ Functional Block Diagram*

The AD-SYNCHRONA14-EBZ also includes 100 MHz (megahertz) and 122.88 MHz (megahertz) VCXOs, making it capable to provide frequencies for instrumentation and telecom applications. Depending on the type of application and range of frequencies you want to use, the firmware will automatically switch between the VCXOs and change the output frequency of AD9545 [https://www.analog.com/AD9545].

ADD-ON Voltage Translation Board

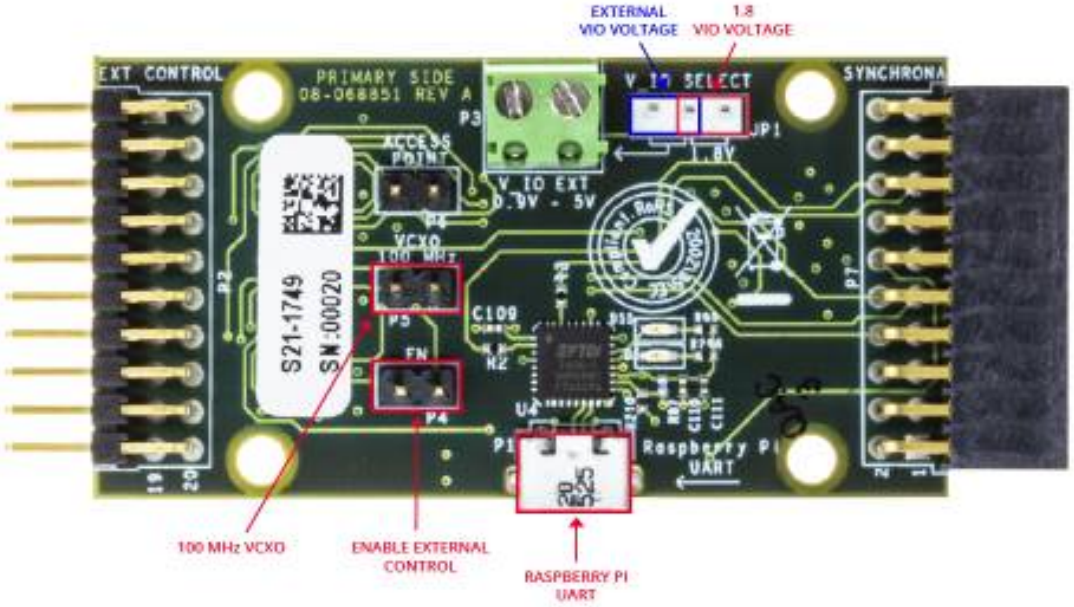
(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/ad-synchrona-ebz.jpg?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 13. Add-on Voltage Translation Board*

Inside the AD-SYNCHRONA14-EBZ package, you can find an ADD-ON board that allows you to connect via SPI (Serial Peripheral Interface) with an external CPU or FPGA. It has voltage translators able to function from 0.9 V (volt) to 5 V (volt). It also gives access to the Raspberry Pi UART (universal asynchronous receiver/transmitter) via USB (Universal Serial Bus).

When the EN jumper (enable) is placed, the SPI (Serial Peripheral Interface) interface is disconnected from the Raspberry Pi inside, allowing external SPI (Serial Peripheral Interface) control.

The VIO_SELECT allows the user to select V (volt)_IO voltage of 1.8 V (volt) (on-board) or the external V (volt)_IO voltage connected on P3.

The VCXO 100 MHz (megahertz) jumper forces the use of the 100 MHz (megahertz) VCXO inside AD-SYNCHRONA14-EBZ.



(/_detail/resources/eval/user-guides/ad-synchrona14-ebz/ad-synchrona14-ebz2_top-1000.jpg?id=resources%3Aeval%3Auser-guides%3Aad-synchrona14-ebz) *Figure 14. Top View of the Add-on Voltage Translation Board*

Design and Integration Files

Schematic AD-SYNCHRONA14-EBZ (/_media/resources/eval/user-guides/ad-synchrona14-ebz/02-064652-01-b.pdf)
Schematic ADD-ON BOARD (/_media/resources/eval/user-guides/ad-synchrona14-ebz/02-068851-01-a.pdf)

End of document