ACPL-072L

3.3V/5V High Speed CMOS Optocoupler

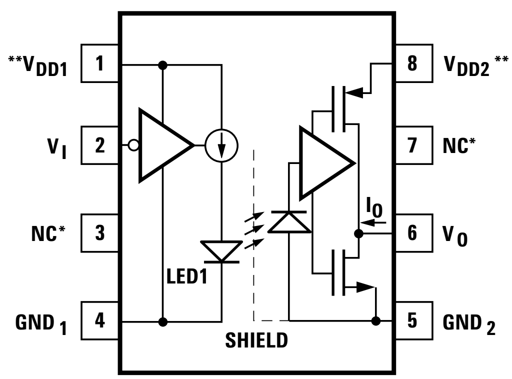
Data Sheet

Description

Available in SO-8 package style, the ACPL -072L optocoupler utilizes the latest CMOS IC technology to achieve outstanding speed performance of minimum 25MBd data rate and 6ns maximum pulse width distortion.

Basic building blocks of this family of products are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



* PIN 3 IS THE ANODE OF THE INTERNAL LED AND MUST BE LEFT UNCONNECTED FOR GUARANTEED DATASHEET PERFORMANCE. PIN 7 IS NOT CONNECTED INTERNALLY.

** A 0.1 µF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 1 AND 4, AND 5 AND 8.

TRUTH TABLE
(POSITIVE LOGIC)

V_I, INPUT	LED1	V_O, OUTPUT
H	OFF	H
L	ON	L

Features

- Dual voltage operation (3.3V and 5V)
- Allow level shifting functionality
- Support high Speed datarate of 25 MBd
- Wide Temperature Operation
- Totem Pole output and buffer input
- Compatible with CMOS and TTL logic level
- Lower power consumption with 3.3V supply
- Good AC performance with lower pulse width distortion
- Lead-free option available

Specifications

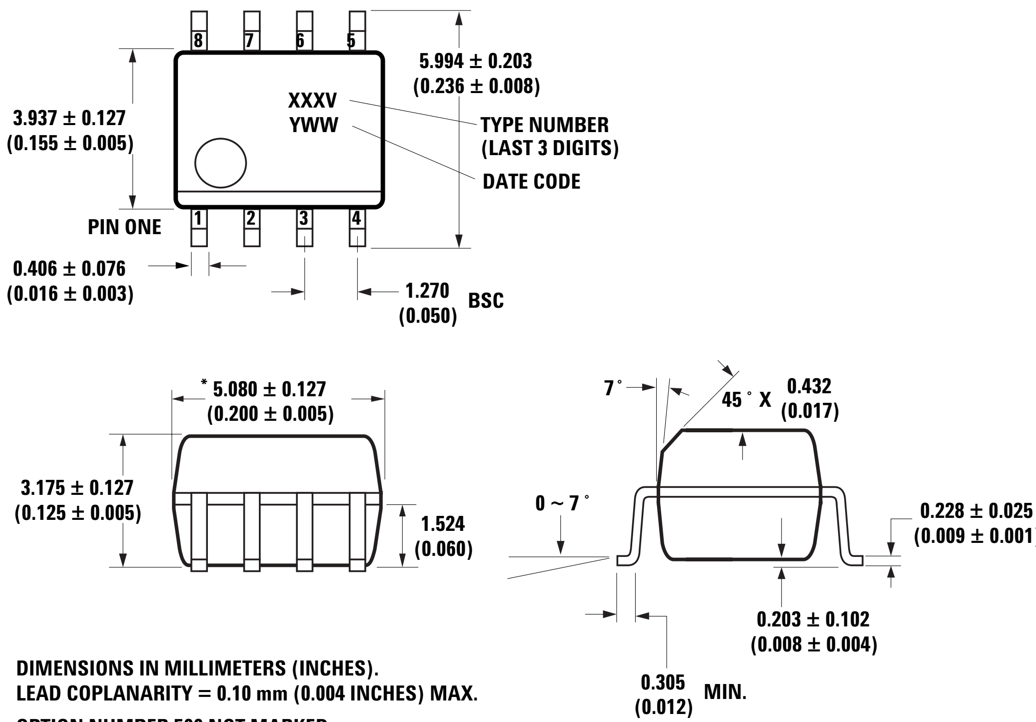
- 3.3V and 5V CMOS Compatibility
- High Speed: DC to 25 MBd
- 6ns max. Pulse Width Distortion
- 40 ns max. Prop. Delay
- 20 ns max. Prop. Delay Skew
- 10 kV/us min. Common Mode Rejection
- -40 to 105 ^{0}C Temperature Range
- Safety and Regulatory Approvals Pending
  UL Recognised
  3750V rms for 1 min. per UL1577 for ACPL-072L
  CSA Component Acceptance Notice #5
  IEC/EN/DIN EN 60747-5-2 for option 060
  - V_{IORM} = 560 Vpeak

Applications

- Digital Fieldbus Isolation: CC-Link, DeviceNet, Profibus, SDS
- Multiplexed Data Transmission
- General Instrument and Data Acquisition
- Computer Peripheral interface
- Microprocessor System Interface

Package Dimensions

ACPL-072L Small Outline SO-8 Package



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.
OPTION NUMBER 500 NOT MARKED.

Device Selection Guide

Small Outline SO-8
ACPL-072L

Ordering Information

Specify Part Number followed by Option Number (if desired)

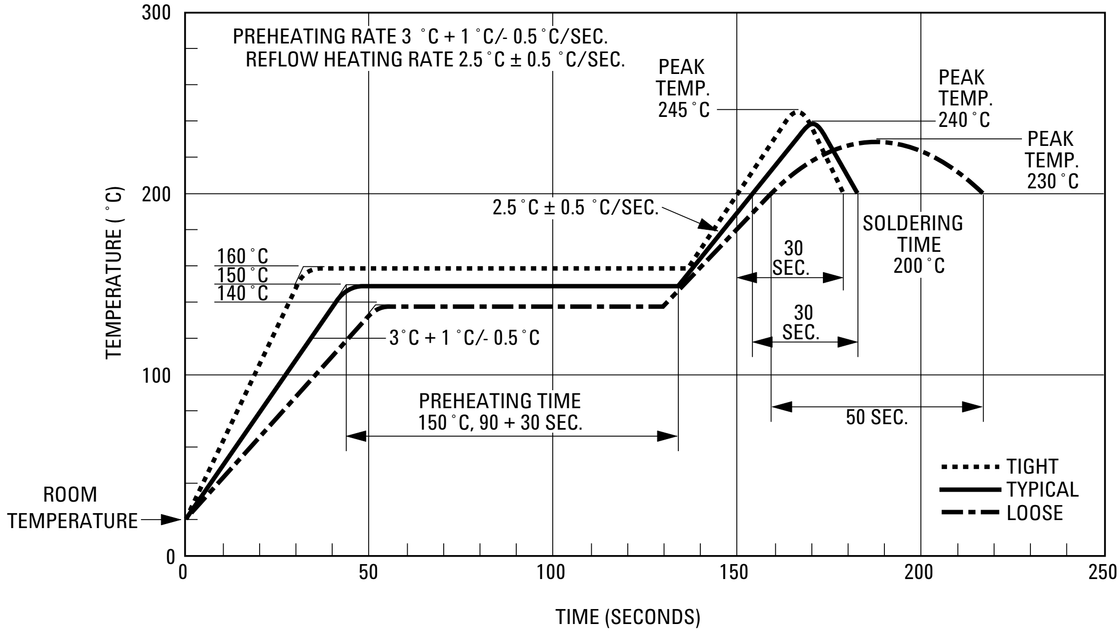
Example:

ACPL-072L-XXX

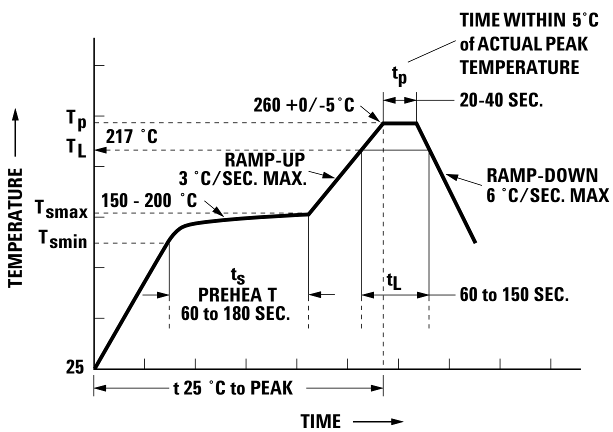
- **060 = IEC/EN/DIN EN 60747-5-2.**
- **500 = Tape and Reel Packaging Option.**
- **XXXE= Lead Free Option.**

No Option and Option 300 contain 100 units per tube. Option 500 contains 1500 units per reel. Option data sheets available. Please contact sales representative or authorized distributor.

Solder Reflow Temperature Profile



Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Regulatory Information

The ACPL-072L is pending approval from the following organizations:

IEC/EN/DIN EN 60747-5-2
Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01.
(option 060 only)

UL
Approved under UL 1577, component recognition program up to VISO = 3750 VRMS. File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics*

Description	Symbol	Characteristic Option 060	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I - IV	
for rated mains voltage ≤ 300 V_{rms}		I - III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V_{peak}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1050	V_{peak}
Input to Output Test Voltage, Method a** V_{IORM} x 1.5=V_{PR}, Try and Sample Test, t_m=60sec, Partial discharge < 5 pC	V_{PR}	840	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage $_{tin}$i = 10 sec)	V_{IOTM}	4000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure, also see Figure 2.			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_{IO}	$>10^9$	Ω

* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

** Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2, for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Note: The surface mount classification is Class A in accordance with CECC 00802.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-072L	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago Technologies data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads mus be considered.

There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	TS	-55	+125	°C
Ambient Operating Temperature[1]	T_A	-40	+105	°C
Supply Voltages	V_{DD1}, V_{DD2}	0	6.0	Volts
Input Voltage	V_I	-0.5	V_{DD1} +0.5	Volts
Output Voltage	V_O	-0.5	V_{DD2} +0.5	Volts
Average Output Current	I_O		5	mA
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	N.A.			

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	+105	°C
Supply Voltages (3.3V operation)	V_{DD1}, V_{DD2}	3.0	3.6	V
Supply Voltages (5V operation)	V_{DD1}, V_{DD2}	4.5	5.5	V
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V
Logic Low Input Voltage	V_{IL}	0.0	0.8	V
Input Signal Rise and Fall Times	t_r, t_f		1.0	ms

Table 3. Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.
The following specifications cover the following power supply combinations:
($4.5V \le V_{DD1} \le 5.5V$, $4.5V \le V_{DD2} \le 5.5V$), ($3V \le V_{DD1} \le 3.6V$, $3V \le V_{DD2} \le 3.6V$),
($4.5V \le V_{DD1} \le 5.5V$, $3V \le V_{DD2} \le 3.6V$) and ($3V \le V_{DD1} \le 3.6V$, $4.5V \le V_{DD2} \le 5.5V$).
All typical specifications are at T_A=+25°C , V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Logic Low Input Supply Current[2]	I_{DD1L}		8.8	15	mA	V_I = 0 V
Logic High Input Supply Current[2]	I_{DD1H}		1.4	5	mA	$V_I = V_{DD1}$
Output Supply Current	I_{DD2L}		4.3	10	mA	
	I_{DD2H}		4.5	10	mA	
Input Current	I_I	-10		10	uA	
Logic High Output Voltage	V_{OH}	2.9	3.3		V	I_O = -20 uA, $V_I = V_{IH}$
		1.9	2.9		V	I_O = -4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 uA, $V_I = V_{IL}$
			0.35	1.0	V	I_O= 4 mA, $V_I = V_{IL}$

Table 4. Switching Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.
The following specifications cover the following power supply combinations:
($4.5V \le V_{DD1} \le 5.5V$, $4.5V \le V_{DD2} \le 5.5V$), ($3V \le V_{DD1} \le 3.6V$, $3V \le V_{DD2} \le 3.6V$),
($4.5V \le V_{DD1} \le 5.5V$, $3V \le V_{DD2} \le 3.6V$) and ($3V \le V_{DD1} \le 3.6V$, $4.5V \le V_{DD2} \le 5.5V$).
All typical specifications are at T_A=+25°C, V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propogation Delay Time to Logic Low Output[3]	t_{PHL}		23.5	40	ns	C_L = 15 pF CMOS Signal Levels
Propogation Delay Time to Logic High Output[3]	t_{PLH}		25.5	40	ns	C_L = 15 pF CMOS Signal Levels
Pulse Width	t_{PW}	40			ns	C_L = 15 pF CMOS Signal Levels
Maximum Data Rate				25	MBd	C_L = 15 pF CMOS Signal Levels
Pulse Width Distortion[4] $\| t_{PHL} - t_{PLH} \|$	$\|PWD\|$		2	6	ns	C_L = 15 pF CMOS Signal Levels
Propagation Delay Skew[5]	t_{PSK}			20	ns	C_L = 15 pF CMOS Signal Levels
Output Rise Time (10% - 90%)	t_R		9		ns	C_L = 15 pF CMOS Signal Levels
Output Fall Time (90% - 10%)	t_F		8		ns	C_L = 15 pF CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output[6]	$\|CM_H\|$	10	20		kV/us	V_{CM} = 1000 V, T_A = 25°C, $V_I = V_{DD1}$, V_O > 0.8 V_{DD1}
Common Mode Transient Immunity at Logic Low Output[6]	$\| CM_L \|$	10	20		kV/us	V_{CM} = 1000 V, T_A = 25°C, V_I = 0V, V_O > 0.8 V

Table 5. Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary With-stand Voltage[7,8,9]	V_{ISO}	3750			V rms	RH ≤ 50%, t = 1 min, T_A = 25 C
Input-Output Resistance[7]	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz
Input Capacitance[10]	C_I		3.0		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		160		°C/W	Thermocouple located at center underside of package
Output IC Junction-to-Case Thermal Resistance	θjco		135		°C/W	
Package Power Dissipation	P_{PD}			150	mW	

Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee functionality.
2. The LED is ON when VI is low and OFF when VI is high.
3. tPHL propagation delay is measured from the 50% level on the falling edge of the VI signal to the 50% level of the falling edge of the VO signal. tPLH propagation delay is measured from the 50% level on the rising edge of the VI signal to the 50% level of the rising edge of the VO signal.
4. PWD is defined as |tPHL - tPLH|. %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
5. tPSK is equal to the magnitude of the worst case difference in tPHL and/or tPLH that will be seen between units at any given temperature within the recommended operating conditions.
6. CMH is the maximum common mode voltage slew rate that can be sustained while maintaining VO > 0.8 VDD2. CML is the maximum common mode voltage slew rate that can be sustained while maintaining VO < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
7. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
8. In accordance with UL1577, each ACPL-072L is proof tested by applying an insulation test voltage ³ 3000 VRMS for 1 second (leakage detection current limit, II-O £ 5 mA). Each ACPL-772L is proof tested by applying an insulation test voltage ³ 4500 Vrms for 1 second (leakage detection current limit. II-O £ 5 mA.)
9. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled “Optocoupler Input-Output Endurance Voltage.”
10. CI is the capacitance measured at pin 2 (VI).

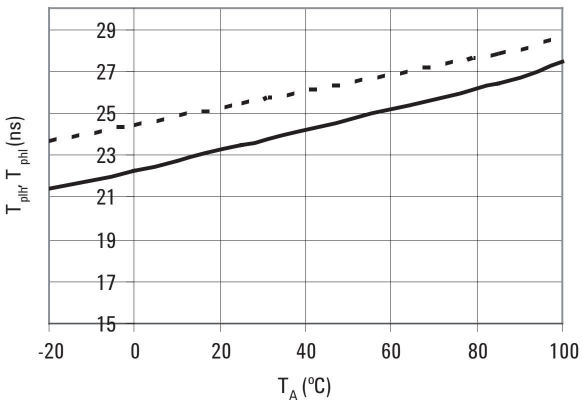


Figure 1: Typical Propagation delays vs temperature

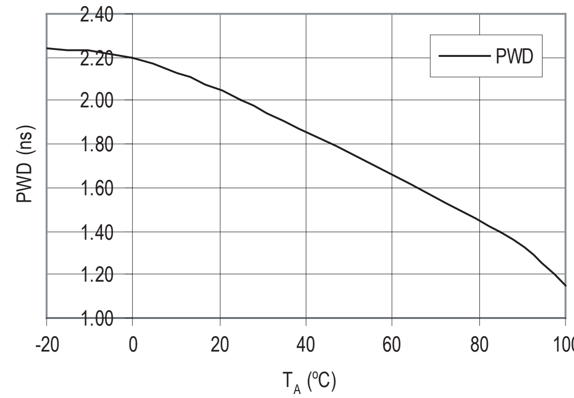


Figure 2: Typical pulse width distortion vs temperature

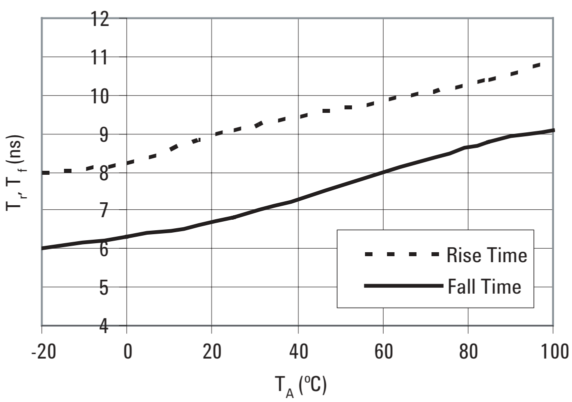


Figure 3: Typical Rise and Fall Time vs temperature

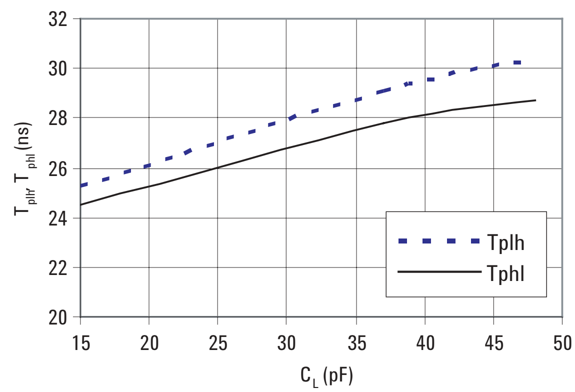


Figure 4: Typical Propagation delays vs load capacitance

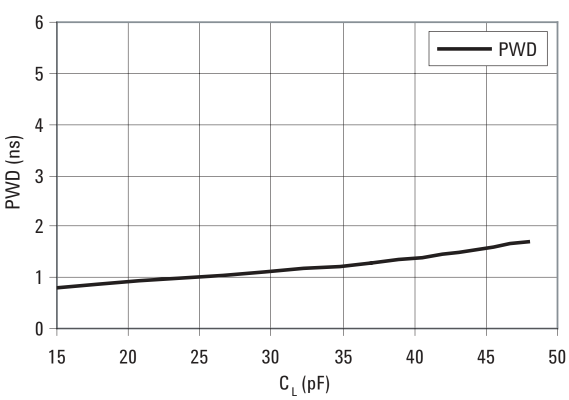


Figure 5: Typical Pulse Width Distortion vs load capacitance

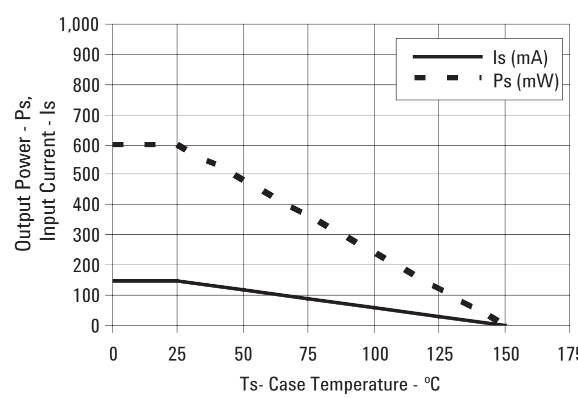


Figure 6: Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-2.

Application Information

Bypassing and PC Board Layout

The ACPL-072L optocoupler is extremely easy to use. No external interface circuitry is required because ACPL-072L uses high speedCMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 7, the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01µF and 0.1µF. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20mm. Figure 8 illustrates the recommended printed circuit board layout for ACPL-072L.

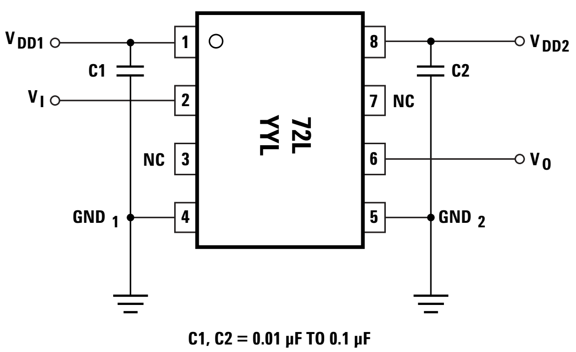


Figure 7. Recommended Circuit Diagram

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation Delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from a low to high(t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low. Please see Figure 9.

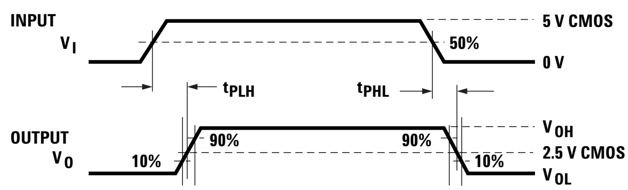


Figure 9. Signal plot shows how propagation delay is defined

Pulse-width distortion (PWD) is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable. The PWD specification for ACPL-072L is 6ns (15%) maximum across recommended operating conditions.

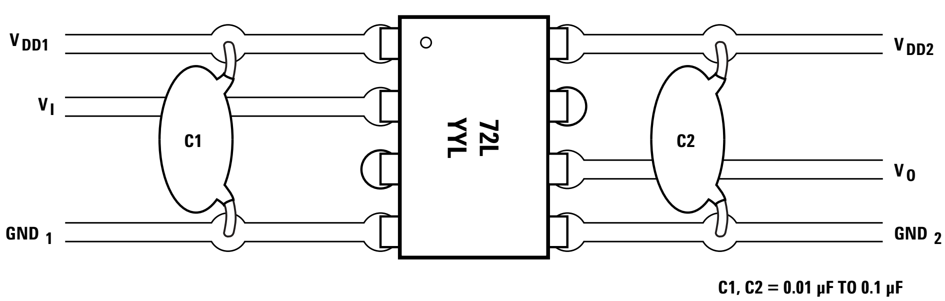


Figure 8. Recommended Printed Circuit Board Layout

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} for any given group of optocouoplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL} and the longest propagation delay, either t_{PLH} and t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and data lines being sent through the optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. In this case the data is assumes to be clocked off of the rising edge of the clock.

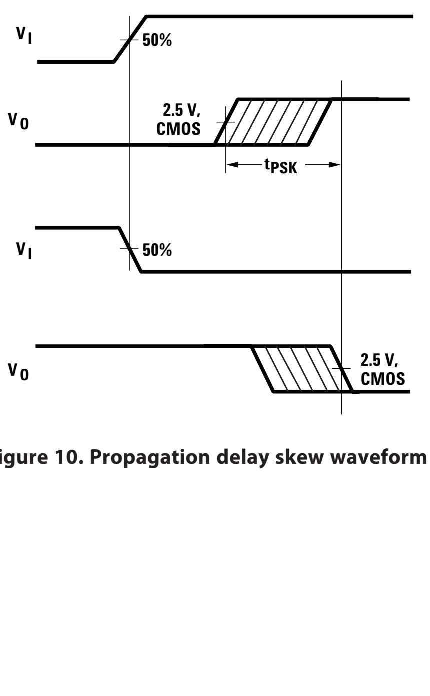


Figure 10. Propagation delay skew waveform

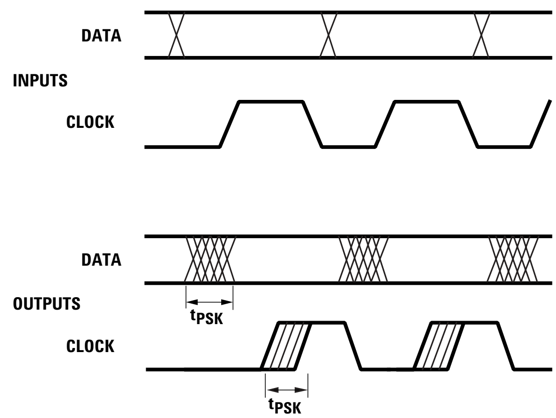


Figure 11. Parallel data transmission example.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The ACPL-072L optocoupler offers the advantage of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature and power supply ranges.

5989-4786EN - February 13, 2006