General-purpose Operational Amplifier / Comparator

Low Voltage CMOS Comparator
BU7251G, BU7251SG, BU7231G, BU7231SG, BU7252F/FVM, BU7252S F/FVM, BU7232F/FVM, BU7232S F/FVM

● Description
CMOS comparator BU7251/BU7231 family and BU7252/BU7232 family are input full swing and push pull output comparator. These ICs integrate one op-amp or two independent op-amps and phase compensation capacitor on a single chip. The features of these ICs are low operating supply voltage that is +1.8V to +5.5V (single supply) and low supply current, extremely low input bias current.

● Features
1) Low operating supply voltage (+1.8[V] ~ +5.5[V])
2) +1.8[V] ~ +5.5[V] (single supply)
   ±0.9[V] ~ ±2.75[V] (split supply)
3) Input and Output full swing
4) Push-pull output type
5) High speed operation
   (BU7251 family, BU7252 family)
6) Low supply current
   (BU7231 family, BU7232 family)
7) Internal ESD protection
   Human body model (HBM) ±4000[V] (Typ.)
8) Wide temperature range
   −40[°C] ~ +85[°C]
   (BU7251G, BU7252 family, BU7231G, BU7232 family)
   −40[°C] ~ +105[°C]
   (BU7251SG, BU7252S family, BU7231SG, BU7232S family)

● Pin Assignments

SSOP5
BU7251G
BU7251SG
BU7231G
BU7231SG

SOP8
BU7252F
BU7252SF
BU7232F
BU7232SF

MSOP8
BU7252FVM
BU7252SFVM
BU7232FVM
BU7232SFVM
### Electrical characteristics

**BU7251 family, BU7252 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Temperature range</th>
<th>Guaranteed Limit</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Current (*2)</td>
<td>Iio</td>
<td>25℃</td>
<td>- 1 11 - 1 11</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (*2)</td>
<td>Ib</td>
<td>25℃</td>
<td>- 1 - 1 -</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Input Common-mode voltage Range</td>
<td>Vcm</td>
<td>25℃</td>
<td>0 - - 0 - 3</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>AV</td>
<td>25℃</td>
<td>- 90 - - 90 -</td>
<td>dB</td>
<td>RL=10[kΩ]</td>
</tr>
<tr>
<td>Supply current (*4)</td>
<td>IDD</td>
<td>- 15 35 - 35 65</td>
<td>µA</td>
<td>RL=100</td>
<td></td>
</tr>
<tr>
<td>Power supply rejection ratio</td>
<td>PSRR</td>
<td>25℃</td>
<td>- 80 - - 80 -</td>
<td>dB</td>
<td>–</td>
</tr>
<tr>
<td>Common-mode rejection ratio</td>
<td>CMRR</td>
<td>25℃</td>
<td>- 80 - - 80 -</td>
<td>dB</td>
<td>–</td>
</tr>
<tr>
<td>Output source current (3)</td>
<td>IOH</td>
<td>25℃</td>
<td>1 2 1 2</td>
<td>mA</td>
<td>VDD-0.4</td>
</tr>
<tr>
<td>Output sink current (3)</td>
<td>IOL</td>
<td>25℃</td>
<td>3 6 3 6</td>
<td>mA</td>
<td>VSS+0.4</td>
</tr>
<tr>
<td>High Level Output Voltage (4)</td>
<td>VOH</td>
<td>25℃</td>
<td>- VDD-0.1 - - VDD-0.1 -</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage (4)</td>
<td>VOL</td>
<td>25℃</td>
<td>- - VSS+0.1 - - VSS+0.1</td>
<td>–</td>
<td>RL=10[kΩ]</td>
</tr>
<tr>
<td>Output rise time</td>
<td>Tr</td>
<td>25℃</td>
<td>- 50 - - 50 -</td>
<td>ns</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Output fall time</td>
<td>Tf</td>
<td>25℃</td>
<td>- 20 - - 20 -</td>
<td>ns</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Propagation delay L to H</td>
<td>TPLH</td>
<td>25℃</td>
<td>- 0.55 - - 0.55 -</td>
<td>µs</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Propagation delay H to L</td>
<td>TPHL</td>
<td>25℃</td>
<td>- 0.25 - - 0.25 -</td>
<td>µs</td>
<td>CL=15pF 100mV over drive</td>
</tr>
</tbody>
</table>

**BU7231 family, BU7232 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Temperature range</th>
<th>Guaranteed limit</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage (*5)</td>
<td>Vio</td>
<td>25℃</td>
<td>Min. Typ. Max.</td>
<td>mV</td>
<td>–</td>
</tr>
<tr>
<td>Input Offset Current (*5)</td>
<td>Iio</td>
<td>25℃</td>
<td>- 1 - - 1 -</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current (*5)</td>
<td>Ib</td>
<td>25℃</td>
<td>- 1 - - 1 -</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Input Common-mode voltage Range</td>
<td>Vcm</td>
<td>25℃</td>
<td>0 - - 0 - 3</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>AV</td>
<td>25℃</td>
<td>- 90 - - 90 -</td>
<td>dB</td>
<td>RL=10[kΩ]</td>
</tr>
<tr>
<td>Supply current</td>
<td>IDD</td>
<td>- 5 15 - 10 25</td>
<td>µA</td>
<td>RL=100</td>
<td></td>
</tr>
<tr>
<td>Power supply rejection ratio</td>
<td>PSRR</td>
<td>25℃</td>
<td>- 80 - - 80 -</td>
<td>dB</td>
<td>–</td>
</tr>
<tr>
<td>Common-mode rejection ratio</td>
<td>CMRR</td>
<td>25℃</td>
<td>- 80 - - 80 -</td>
<td>dB</td>
<td>–</td>
</tr>
<tr>
<td>Output source current (6)</td>
<td>IOH</td>
<td>25℃</td>
<td>1 2 1 2</td>
<td>mA</td>
<td>VDD-0.4</td>
</tr>
<tr>
<td>Output sink current (6)</td>
<td>IOL</td>
<td>25℃</td>
<td>3 6 3 6</td>
<td>mA</td>
<td>VSS+0.4</td>
</tr>
<tr>
<td>High Level Output Voltage (7)</td>
<td>VOH</td>
<td>25℃</td>
<td>VDD-0.1 - VDD-0.1 -</td>
<td>–</td>
<td>RL=10[kΩ]</td>
</tr>
<tr>
<td>Low Level Output Voltage (7)</td>
<td>VOL</td>
<td>25℃</td>
<td>- - VSS+0.1 - - VSS+0.1</td>
<td>–</td>
<td>RL=10[kΩ]</td>
</tr>
<tr>
<td>Output rise time</td>
<td>Tr</td>
<td>25℃</td>
<td>- 50 - - 50 -</td>
<td>ns</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Output fall time</td>
<td>Tf</td>
<td>25℃</td>
<td>- 20 - - 20 -</td>
<td>ns</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Propagation delay L to H</td>
<td>TPLH</td>
<td>25℃</td>
<td>- 1.7 - - 1.7 -</td>
<td>µs</td>
<td>CL=15pF 100mV over drive</td>
</tr>
<tr>
<td>Propagation delay H to L</td>
<td>TPHL</td>
<td>25℃</td>
<td>- 0.5 - - 0.5 -</td>
<td>µs</td>
<td>CL=15pF 100mV over drive</td>
</tr>
</tbody>
</table>

**Note:** Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out absoluted maximum rated temperature environment may cause deterioration of characteristics.

(*4) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VEE.

### Absolute maximum ratings (Ta=25[℃])

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VDD-VSS</td>
<td>BU7251G, BU7252 F/FVM BU7231G, BU7232 F/FVM</td>
<td>V</td>
</tr>
<tr>
<td>Differential Input Voltage (*1)</td>
<td>VId</td>
<td>BU7251G, BU7252 F/FVM BU7231G, BU7232 F/FVM</td>
<td>V</td>
</tr>
<tr>
<td>Input Common-mode voltage range</td>
<td>Vcm</td>
<td>(VSS – 0.3) to VDD + 0.3</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Topr</td>
<td>- 40 to +85 - 40 to +105</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>- 55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum junction Temperature</td>
<td>Tjmax</td>
<td>+ 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:** Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out absoluted maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.

(*2) Absolute values

(*3) Reference to power dissipation under the high temperature environment and decide the output current.

(*4) Continuous short circuit is occurring the degenerate of output current characteristics.

(*5) Full range

(*6) Reference to power dissipation under the high temperature environment and decide the output current.

(*7) Continuous short circuit is occurring the degenerate of output current characteristics.

(*8) Full range

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2/16
Example of electrical characteristics

BU7251 family

(*) The above date is ability value of sample, it is not guaranteed. BU7251G: -40°C to +85°C, BU7251SG: -40°C to +105°C
The above data is ability value of sample, it is not guaranteed. BU7251G: -40[°C] to +85[°C]  BU7251SG: -40[°C] to +105[°C]
BU7252 family

(* The above date is ability value of sample, it is not guaranteed.  BU7252 F/FVM : -40°C to +85°C  BU7252S F/FVM : -40°C to +105°C)
BU7252 family

(*) The above date is ability value of sample, it is not guaranteed.

BU7252 F/FVM: -40[°C] to +85[°C]  
BU7252S F/FVM: -40[°C] to +105[°C]
BU7231 series

(*) The above date is ability value of sample, it is not guaranteed.  BU7231G : -40[℃] to +85[℃]  BU7231SG : -40[℃] to +105[℃]
BU7231 series

(*) The above date is ability value of sample, it is not guaranteed. BU7231G : −40[℃] to +85[℃]  BU7231SG : −40[℃] to +105[℃]
(*) The above value is the ability value of the sample, it is not guaranteed.

BU7232 F/FVM: -40°C to +85°C
BU7232S FVM: -40°C to +105°C
BU7232 family

Fig. 13
Input Offset Voltage – Ambient Temperature

Fig. 14
Input Offset Voltage – Ambient Temperature

Fig. 15
Input Offset Voltage – Input Voltage

Fig. 16
Large Signal Voltage Gain – Supply Voltage

Fig. 17
Large Signal Voltage Gain – Ambient Temperature

Fig. 18
Common Mode Rejection Ratio – Supply Voltage

Fig. 19
Common Mode Rejection Ratio – Ambient Temperature

Fig. 20
Power Supply Rejection Ratio – Ambient Temperature

Fig. 21
Propagation Delay L-H – Ambient Temperature

Fig. 22
Propagation Delay H-L – Ambient Temperature

(*) The above date is ability value of sample, it is not guaranteed.  
BU7232 F/FVM : −40[℃] to +85[℃]  
BU7232S F/FVM : −40[℃] to +105[℃]
### Test circuit1 NULL method

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VF</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>Calculation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset voltage</td>
<td>VF1</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>3</td>
</tr>
<tr>
<td>Large signal voltage gain</td>
<td>VF2</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>3</td>
</tr>
<tr>
<td>Common-mode rejection ratio</td>
<td>VF3</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>3</td>
</tr>
<tr>
<td>Power supply rejection ratio</td>
<td>VF4</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>VF5</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>5.5</td>
</tr>
</tbody>
</table>

#### Calculation

1. Input offset Voltage (\(\text{V}_{\text{io}}\))
   \[
   \text{V}_{\text{io}} = \frac{|\text{VF}|}{1 + R_f/R_s} \text{[V]}
   
2. Large signal voltage gain (\(\text{Av}\))
   \[
   \text{Av} = 20 \log \frac{V_{\text{f1}}}{V_{\text{f2}} \cdot V_{\text{f3}}} \text{[dB]}
   
3. Common-mode rejection ratio (CMRR)
   \[
   \text{CMRR} = 20 \log \frac{3V_{\text{f1}}}{V_{\text{f4}} \cdot V_{\text{f5}}} \text{[dB]}
   
4. Power supply rejection ratio (PSRR)
   \[
   \text{PSRR} = 20 \log \frac{3.7V_{\text{f1}}}{V_{\text{f6}} \cdot V_{\text{f7}}} \text{[dB]}

---

**Fig.1 Simplified schematic**

**Fig.2 Test Circuit 1 (one channel only)**
### Test circuit 2 switch condition

<table>
<thead>
<tr>
<th>SW No.</th>
<th>SW 1</th>
<th>SW 2</th>
<th>SW 3</th>
<th>SW 4</th>
<th>SW 5</th>
<th>SW 6</th>
<th>SW 7</th>
<th>SW 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>supply current</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>maximum output voltage RL=10 [kΩ]</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>output current</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>response time</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

![Test Circuit 2 Diagram](image)

**Fig3. Test circuit 2 (one channel only)**

![Input Wave](image)

**Fig4. Slew rate**
1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage \((VDD/VSS)\)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage \((Vid)\)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range \((Vicm)\)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation \((Pd)\)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics item

2.1 Input offset voltage \((Vio)\)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V].

2.2 Input offset current \((Iio)\)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current \((Ib)\)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Input common-mode voltage range \((Vicm)\)

Indicates the input voltage range where IC operates normally.

2.5 Large signal voltage gain \((AV)\)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

\[ Av = \frac{\text{Output voltage fluctuation}}{\text{Input offset fluctuation}} \]

2.6 Circuit current \((ICC)\)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.7 Output sink current \((OL)\)

Indicates the maximum current that can be output under specified output condition (such as output voltage and load condition).

2.8 Output saturation voltage, Low level output voltage \((VOL)\)

Indicates the voltage range that can be output under specified load conditions.

2.9 Output leakage current, High level output current \((Ileak)\)

Indicates the current that flows into IC under specified input and output conditions.

2.10 Response Time \((Tre)\)

The interval between the application of an input and output condition.

2.11 Common-mode rejection ratio \((CMRR)\)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

\[ CMRR = \frac{\text{Change of Input common-mode voltage}}{\text{Input offset fluctuation}} \]

2.12 Power supply rejection ratio \((PSRR)\)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.

\[ PSRR = \frac{\text{Change of power supply voltage}}{\text{Input offset fluctuation}} \]
Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol $\theta_{ja}$ [°C/W]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.6 (a) shows the model of thermal resistance of the package. Thermal resistance $\theta_{ja}$, ambient temperature $T_a$, junction temperature $T_j$, and power dissipation $P_d$ can be calculated by the equation below:

$$\theta_{ja} = \frac{(T_j - T_a)}{P_d} \ [°C/W] \quad \cdots \cdots \ (1)$$

Derating curve in Fig.6 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance $\theta_{ja}$. Thermal resistance $\theta_{ja}$ depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.7 (c)-(f) show a derating curve for an example of BU7251 family, BU7252 family, BU7231 family, BU7232 family.

When using the unit above $T_a=25°C$, subtract the value above per degree [°C]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted.
Cautions on use

1) Absolute maximum ratings
   Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
   For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD+0.3[V]. Then, regardless of power supply voltage VSS-0.3[V] can be applied to input terminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
   The voltage comparator operates if a given level of voltage is applied between VDD and VSS. Therefore, the operational amplifier can be operated under single power supply or split power supply.

4) Power dissipation (pd)
   If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability. Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
   Short circuits between pins and incorrect mounting when mounting the IC on a printed circuit board, take notice of the direction and positioning of the IC. If IC is mounted erroneously, it may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Using under strong electromagnetic field
   Be careful when using the IC under strong electromagnetic field because it may malfunction.

7) Usage of IC
   When stress is applied to the IC through warp of the printed circuit board, the characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

8) Testing IC on the set board
   When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress. When removing IC from the set board, it is essential to cut supply voltage. As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

9) The IC destruction caused by capacitive load
   The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor. When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

10) Decoupling capacitor
    Insert the decouling capacitance between VDD and VSS, for stable operation of operational amplifier.

11) Latch up
    Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise
Dimensions

Model number construction

- Specify the product by the model number when placing an order.
- Make sure of the combinations of items.
- Start with the leftmost space without leaving any empty space between characters.

ROHM
- BU7251 BU7251S
- BU7231 BU7231S
- BU7252 BU7252S
- BU7232 BU7232S

Package type
- G: SSOP5
- F: SOP8
- FVM: MSOP8

E2 Embossed tape on reel with pin 1 near far when pulled out
TR Embossed tape on reel with pin 1 near far when pulled out

Packing specification reference

<table>
<thead>
<tr>
<th>Package</th>
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Appendix

Notes

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