Video/Audio Interfaces for TV and DVD Recorders

NTSC-PAL Video I/O Interface

BH7625KS2

●**Description**

BH7625KS2 is a video signal selector with two built-in sync separation circuits, and two sync detector circuits. It includes 5-composit, 5-Y, 5-C, and 1-component video signal inputs that can be selected freely for each output. Additionally, The existance of the signal outputted from outside can be judged by only this chip.

●**Features**

1) Built-in 5-video, 5-Y, 5-C and 1-component inputs
2) Input terminal of the S2 standard suitability
3) I^2C-BUS control (High impedance when power supply off)
4) Built-in 0/3dB switch AMP（CVBS OUT, C OUT）
5) Built-in 0/6dB switch AMP（Y/CVBS OUT）
6) Built-in sync separation circuit（2 circuits SYNC OUT, V SYNC OUT）
7) Built-in sync detector circuit（2 circuits）
8) Built-in 3 LPF circuits（4 order + TRAP）

●**Applications**

DVD-Recorder, visual instrument, etc

●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V	7.0	V
Power dissipation	Pd	1300 ＊1	mW
Operating temperature range	Topr	-25～+75	°C
Storage temperature range	Tstg	-55～+125	°C

＊1 Reduced by 13 mW/°C at 25°C or higher.

●**Operating range** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	VCC1 VCC2 VCC3 DVCC SYNC VCC VCC	4.5～5.5	V

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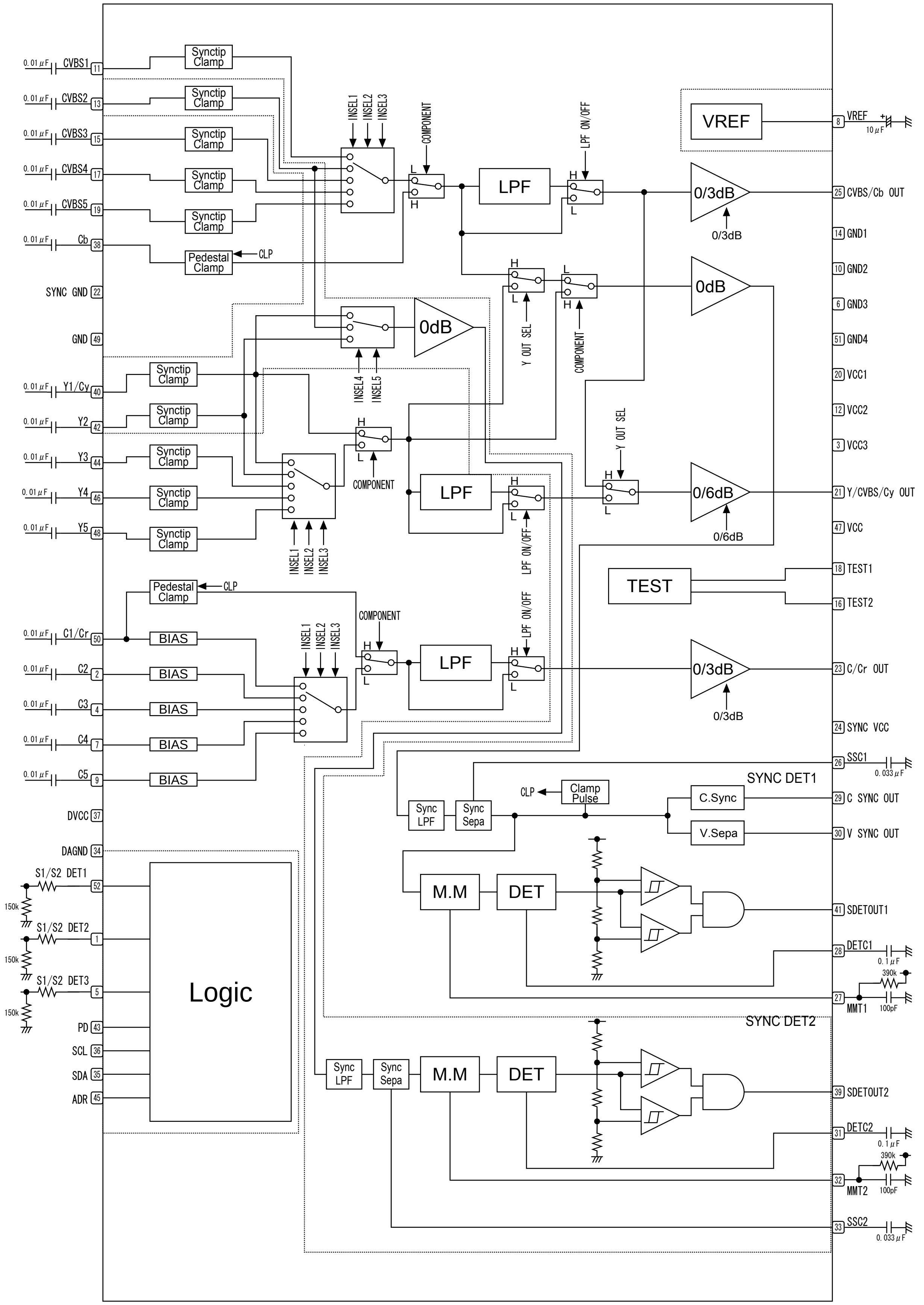
●**Electrical characteristics** (Unless otherwise specified, Vcc1, Vcc2, Vcc3, DVCC, SYNC VCC, VCC=5V, Ta=25°C)

Item		Symbol	Limit			Unit	Conditions
			MIN.	TYP.	MAX.		
＜Whole＞							
VCC Circuit Current		I_{CC}	71	95	128	mA	Normal Condition
VCC STBY Circuit Current		I_{CCST}	9.38	12.5	16.9	mA	Standby Condition
VCC PD Circuit Current		I_{CCPD}	−	0	10	μA	Power Down Condition
＜SW Part＞							
CVBS OUT Cb OUT	Voltage Gain H	G_{V1H}	2.4	2.9	3.4	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
CVBS OUT Cb OUT	Voltage Gain L	G_{V1L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT	Voltage Gain H	G_{V2H}	5.5	6.0	6.5	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT	Voltage Gain L	G_{V2L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
C OUT Cr OUT	Voltage Gain H	G_{V3H}	2.4	2.9	3.4	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
C OUT Cr OUT	Voltage Gain L	G_{V3L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
CVBS OUT Cb OUT	Voltage Gain H	G_{V4H}	2.2	2.7	3.2	dB	Vin=1.0Vpp , f=100kHz, LPF ON
CVBS OUT Cb OUT	Voltage Gain L	G_{V4L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
Y/CVBS OUT Cy OUT	Voltage Gain H	G_{V5H}	5.3	5.8	6.3	dB	Vin=1.0Vpp , f=100kHz, LPF ON
Y/CVBS OUT Cy OUT	Voltage Gain L	G_{V5L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
C OUT Cr OUT	Voltage Gain H	G_{V6H}	2.2	2.7	3.2	dB	Vin=1.0Vpp , f=100kHz, LPF ON
C OUT Cr OUT	Voltage Gain L	G_{V6L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
CVBS OUT Cb OUT	Maximum Output Level	V_{OM1}	2.6	3.0	−	Vpp	f=100kHz(10kHz), THD=1%
Y/CVBS OUT Cy OUT	Maximum Output Level	V_{OM2}	2.6	3.0	−	Vpp	f=100kHz(10kHz), THD=1%
C OUT Cr OUT	Maximum Output Level	V_{OM3}	2.6	3.0	−	Vpp	f=100kHz(10kHz), THD=1%
＜SW Part＞							
CVBS OUT Cb OUT	Frequency Characteristic 1	G_{F11}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz(LPF ON)
CVBS OUT Cb OUT	Frequency Characteristic 2	G_{F12}	−	−38	−27	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=27MHz/100kHz (LPF ON)

Item		Symbol	Limit			Unit	Conditions
			MIN.	TYP.	MAX.		
CVBS OUT Cb OUT	Frequency Characteristic 3	G_{F13}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
Y/CVBS OUT Cy OUT	Frequency Characteristic 1	G_{F21}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz (LPF ON)
Y/CVBS OUT Cy OUT	Frequency Characteristic 2	G_{F22}	−	−38	−27	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=27MHz/100kHz (LPF ON)
Y/CVBS OUT Cy OUT	Frequency Characteristic 3	G_{F23}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
C OUT Cr OUT	Frequency Characteristic 1	G_{F31}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz (LPF ON)
C OUT Cr OUT	Frequency Characteristic 3	G_{F33}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
V-SW	Difference In Switch Voltage Gain	$\angle G_V$	−0.5	0.0	0.5	dB	f=100kHz, Vin=1.0Vpp
Y-SW	Difference In Switch Voltage Gain	$\angle G_Y$	−0.5	0.0	0.5	dB	f=100kHz, Vin=1.0Vpp
C-SW	Difference In Switch Voltage Gain	$\angle G_C$	−0.5	0.0	0.5	dB	f=100kHz, Vin=1.0Vpp
V-SW	Switch Crosstalk	C_{TSV}	−	−60	−55	dB	f=4.43MHz, Vin=1.0Vpp
Y-SW	Switch Crosstalk	C_{TSY}	−	−60	−55	dB	f=4.43MHz, Vin=1.0Vpp
C-SW	Switch Crosstalk	C_{TSC}	−	−60	−55	dB	f=4.43MHz, Vin=1.0Vpp
V⇔Y⇔C Channel Crosstalk		C_{TCH}	−	−60	−55	dB	f=4.43MHz, Vin=1.0Vpp
C IN Input Impedance		Z_{CIN}	12.5	18.0	23.5	kΩ	
＜SYNC DETECTOR Part＞							
Minimum sync separation level		SL_{MIN}	−	0.08	0.15	Vpp	LPF Condition “111”
V SYNC OUT Output Voltage H		V_{VSH}	Vcc −0.5	Vcc −0.1	Vcc	V	No Load
V SYNC OUT Output Voltage L		V_{VSL}	−	0.1	0.5	V	No Load
VD Pulse Width		T_{WV1}	−	185	−	μsec	Vin＝1.0Vpp, Standard staircase signal LPF Condition “111”
HD Pulse Width		T_{WH1}	−	4.5	−	μsec	Vin＝1.0Vpp, Standard staircase signal LPF Condition “111”
C SYNC OUT Output Voltage H		V_{VCH}	Vcc −0.5	Vcc −0.1	Vcc	V	No Load
C SYNC OUT Output Voltage L		V_{VCL}	−	0.1	0.5	V	No Load

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
SYNC DET OUT Output Voltage H	V_{SDH}	Vcc −0.5	Vcc −0.1	Vcc	V	No Load
SYNC DET OUT Output Voltage L	V_{SDL}	−	0.1	0.5	V	No Load
＜I^2C-BUS Control＞						
S1/S2 DET Detection Level H	DL_H	3.4	−	Vcc	V	16:9 Squeeze Signal
S1/S2 DET Detection Level M	DL_M	1.3	1.9	2.5	V	4:3 Letter Box Signal
S1/S2 DET Detection Level L	DL_L	0.0	−	0.7	V	4:3 Video Signal, No Signal
＜ADR＞						
Input Voltage H	V_{IHADR}	2.0	−	Vcc	V	
Input Voltage L	V_{ILADR}	0.0	−	1.0	V	
Input Impedance	Z_{INADR}	65	100	135	kΩ	Pull Down Resistance
＜SCL、SDA＞						
Input Voltage H	V_{IHIIC}	2.0	−	Vcc	V	
Input Voltage L	V_{ILIIC}	0.0	−	1.0	V	
Input Bias Current	I_{BIIC}	0	−1	−10	μA	
＜PD＞						
Input Voltage H	V_{IHPD}	2.0	−	Vcc	V	
Input Voltage L	V_{ILPD}	0.0	−	0.7	V	
Input Impedance	Z_{INPD}	65	100	135	kΩ	Pull Down Resistance
＜Guaranteed design parameter＞						
Differential Gain	D_G	−	0.5	−	%	CVBS OUT, Y/CVBS OUT, C OUT
Differential Phase	D_P	−	0.5	−	deg	CVBS OUT, Y/CVBS OUT, C OUT
Y S/N	S_{NY}	−	−70	−	dB	CVBS OUT, Y/CVBS OUT 50% White signal Filter : 100kHz～6MHz
C S/N	S_{NC}	−	−70	−	dB	C OUT 100% Chroma signal Filter : 100Hz～500kHz

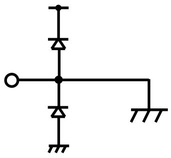
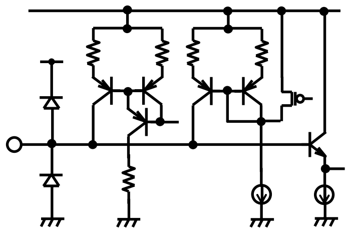
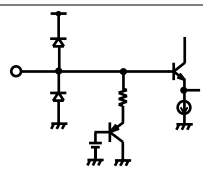
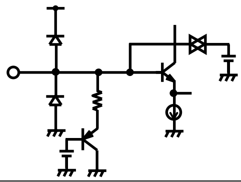
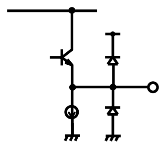
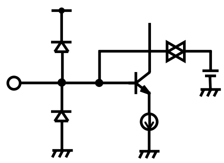
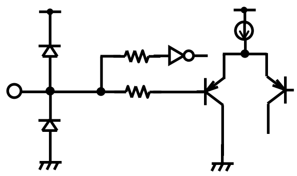
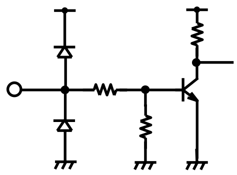
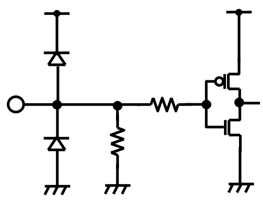
●Block diagram

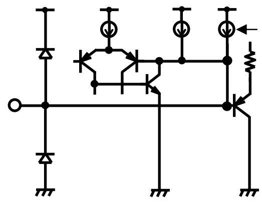
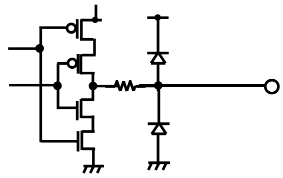
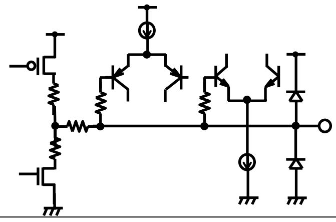
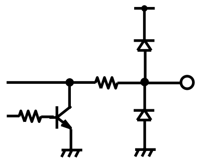
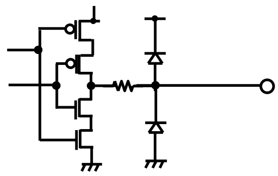
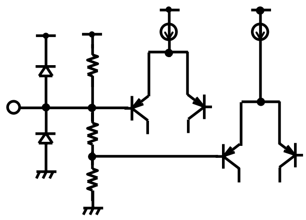
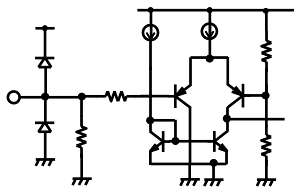
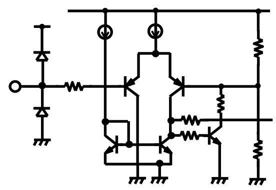
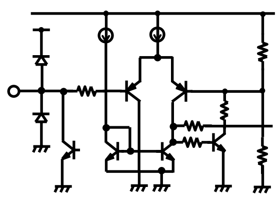


Blocks inside the dotted line operate at a standby mode

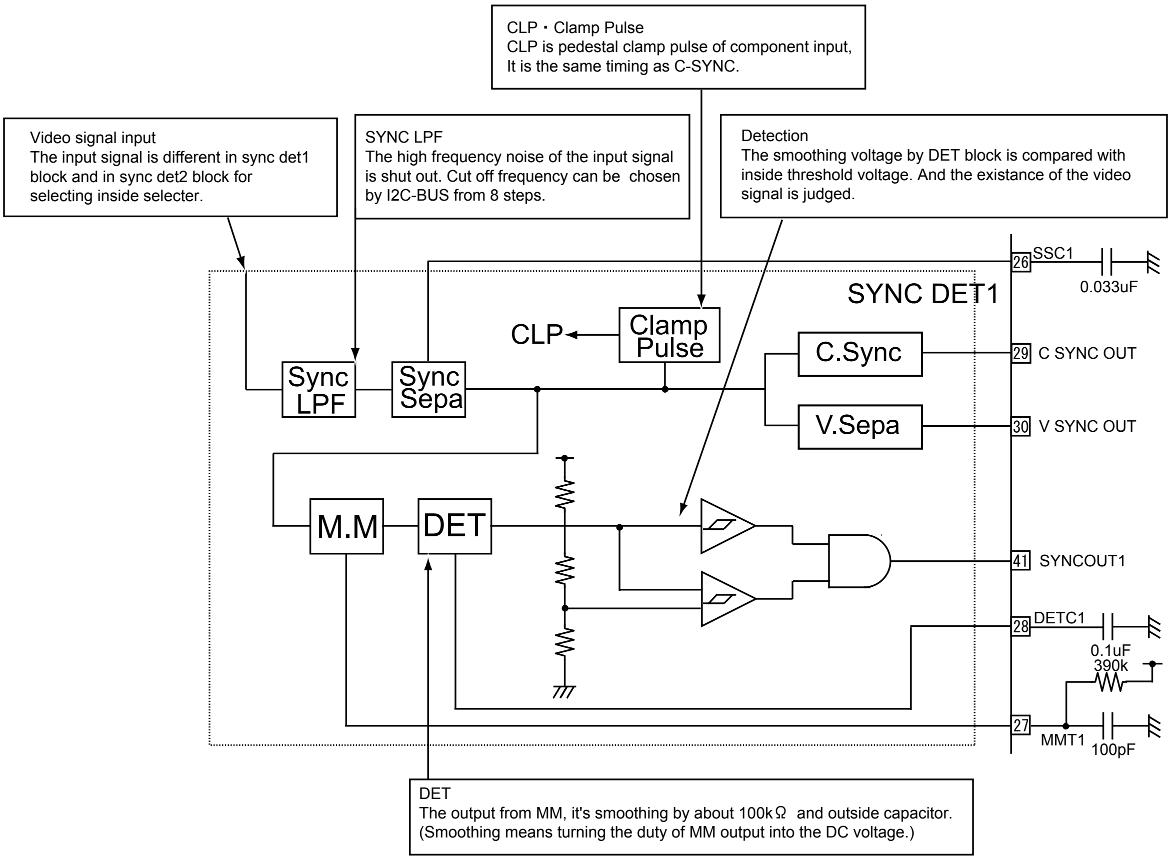
Fig.1

●Equivalent circuit

Pin NO./Pin Name (Input/Output)	Function	Equivalent Circuit	Input Range(V) / Terminal Voltage (V)
14. GND1 10. GND2 6. GND3 51. GND4	GND terminal		0
11. CVBS1 13. CVBS2 15. CVBS3 17. CVBS4 19. CVBS5 40. Y1_Cy 42. Y2 44. Y3 46. Y4 48. Y5	Signal input terminal The video signal input pins is a sync-tip-clamp.		1.4
2. C2 4. C3 7. C4 9. C5	Signal input terminal The video signal input pins is a resistance bias.		2.9
50. C1_Cr	Signal input terminal This pin is input of chroma signal1 (C1) and Cr. Change resistor bias and pedestal clamp.		2.9
25. CVBS/Cb OUT 21. Y/CVBS/Cy OUT 23. C/Cr OUT	Signal output terminal The gain can be selected by I^2C-BUS.		0.7 2.1
38. Cb	Signal input terminal The video signal input pin (Cb) is a pedestal clamp.		—
52. S1/S2 DET1 1. S1/S2 DET2 5. S1/S2 DET3	Signal input terminal The state of inputted signal can be read by I^2C-BUS.		—
43. PD	PD terminal Sets power down mode.		0
18. TEST1 16. TEST2	TEST terminal Shorts to GND.		0

26. SSC1 33. SSC2	SSC terminal Makes reference voltage for sync separation.		–
29. C SYNC OUT 30. V SYNC OUT	C, V sync signal output terminal Outputs sync separation signal.		5.0
28. DETC1 31. DETC2	Generate DET voltage terminal Turns the MM duty pulse into the DC voltage.		–
27. MMT1 32. MMT2	MM adjusting terminal Determines the MM time constant by the outside capacitor and resister.		–
41. SDET OUT1 39. SDET OUT2	Signal output terminal These pins output sync detecting signal.		0
8. VREF	Reference voltage terminal A capacitor is connected to opposite GND.		2.8
25. ADR	ADR terminal The pin to set slave address 90H (91H) or 92H (93H).		0
36. SCL	I^2C-BUS Clock input terminal The pin is input clock of I^2C-BUS. Uses pull up resistor.		–
35. SDA	I^2C-BUS Data terminal The pin is data of I^2C-BUS. Uses pull up resistor.		–

●Description of operations



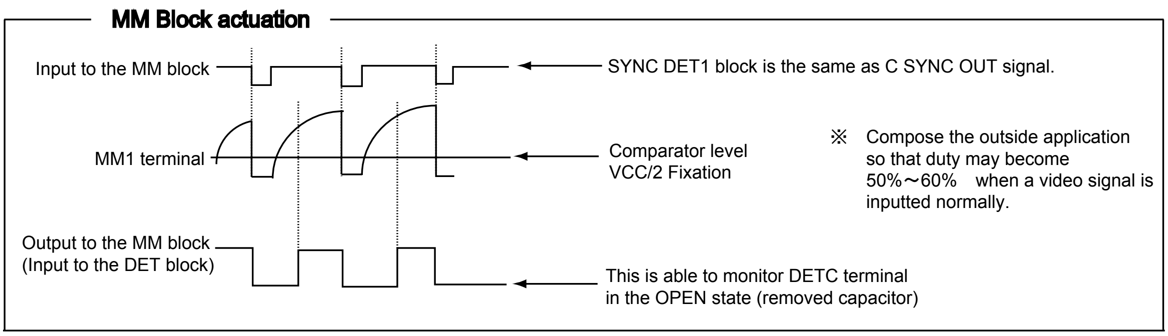


Fig.2

※ The detection sensitivity level of this LSI can be different depending on the tuner used. Therefore, change the detection level setting by selecting LPF cut off and the outside part value of MMT (27 pin, 32 pin) for each tuner when using this feature.

●Description of operations

■I²C-BUS Control input specifications

・I²C-BUS Format (WRITE MODE)

S	SLAVE ADDRESS	A	DATA1	A	DATA2	A	P

S : Start Condition A : Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	B0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	5	4	3	2	1	L2	L1	L0
	INSEL							
DATA2	Y-OUT SEL	Component	LPF ON/OFF	GAIN 0/6dB	STBY	T2	T1	T0

#（Don't Care）

* At power on, BH7625KS2 becomes " * "condition.
* ADR and S1/S2 DET terminal inputs value's must be set between start and stop condition and must be consistent, as a change in value may result in poor operation.

○ SELECT INPUT SWITCH・SETTING MODE

	Explanation		Explanation
ADR	Slave Address (write mode) set by ADR pin 0 : Address is "90H", when ADR pin input is set to L 1 : Address is "92H", when ADR pin input is set to H	INSEL5～4	SYNC DET2 input setting 00 : Y1/Cy * 01 : Y1/Cy 10 : CVBS2 11 : Y2
R/W	READ/WRITE Setting Mode 0 : WRITE 1 : READ	INSEL3～1	Change setting of input selector SW. Refer to the next page SW correspondence table.
Y-OUT SEL	Y-OUT SEL SW output setting 0 : L * 1 : H	Component	Component SEL SW output setting 0 : L (Composit) * 1 : H (Component)
LPF ON/OFF	LPF ON/OFF setting 0 : L （OFF） * 1 : H （ON）	GAIN0/6dB	AMP GAIN setting 0 : L (0dB) * 1 : H (6dB or 3dB)
Stand-By	Stand-By Mode setting 0 : L (move) 1 : H(standby) ※In standby condition, activate only the circuits in the block diagram.		

○ INPUT SW CONTROL table

INSEL 3	INSEL 2	INSEL 1	Y-OUT SEL	Component	CVBS OUT	Y OUT	C OUT	CSYNC etc.
0	0	0	1	0	CVBS1	CVBS1	C1	CVBS1
0	0	1	1	0	CVBS2	CVBS2	C2	CVBS2
0	1	0	1	0	CVBS3	CVBS3	C3	CVBS3
0	1	1	1	0	CVBS4	CVBS4	C4	CVBS4
1	0	0	1	0	CVBS5	CVBS5	C5	CVBS5
0	0	0	0	0	CVBS1	Y1	C1	Y1
0	0	1	0	0	CVBS2	Y2	C2	Y2
0	1	0	0	0	CVBS3	Y3	C3	Y3
0	1	1	0	0	CVBS4	Y4	C4	Y4
1	0	0	0	0	CVBS5	Y5	C5	Y5
-	-	-	0	1	Cb	Y1(Cy)	C1(Cr)	Y1(Cy)
-	-	-	1	1	Cb	Cb	C1(Cr)	Y1(Cy)

	Explanation		Explanation
L2-L0	SYNC SEPA LPF Cut-off conditioning 000 : LOW (Normal) 001 : ↓ 010 : ↓ 011 : ↓ 100 : ↓ 101 : ↓ 110 : ↓ 111 : High *	T2-T0	DET Output decision comparator threshold conditioning. 000 : LOW (Normal) 001 : ↓ 010 : ↓ 011 : ↓ * 100 : ↓ 101 : ↓ 110 : ↓ 111 : High

○ I^2C-BUS Format (READ MODE)

S	SLAVE ADDRESS	A	DATA1	A/N	P

S : Start Condition A : Acknowledge A/N : NO acknowledge P: Stop Condition

	B7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	SD1		SD2		SD3		V-DET2	V-DET1

#（Don't Care）

* ADR and S1/S2 DET terminal inputs value's must be set between start and stop condition and must be consistent, as a change in value may result in poor operation.

	Explanation		Explanation
ADR	Slave Address (read mode) Set by ADR pin. 0 : Address is "91H", when ADR pin input is set to L 1 : Address is "93H", when ADR pin input is set to H	SD1 SD2 SD3	The state of S1/S2 DET1～S1/S2 DET3 is read out. 00 : 4:3Video signal （0～0.7V） 01 : 4:3Letter Box signal （1.3～2.5V） 11 : 16:9Squeeze signal （3.4V～Vcc）
V-DET1, V-DET2	The signal SDET OUT is read out. 0 : H (VIDEO signal ON) 1 : L (VIDEO signal OFF)		

■**Power down state**

Power down state occurs when PD terminal is LOW. Internal circuit becomes non-active in this state.

LOW : Power down state
HI : Active state

●Application circuit

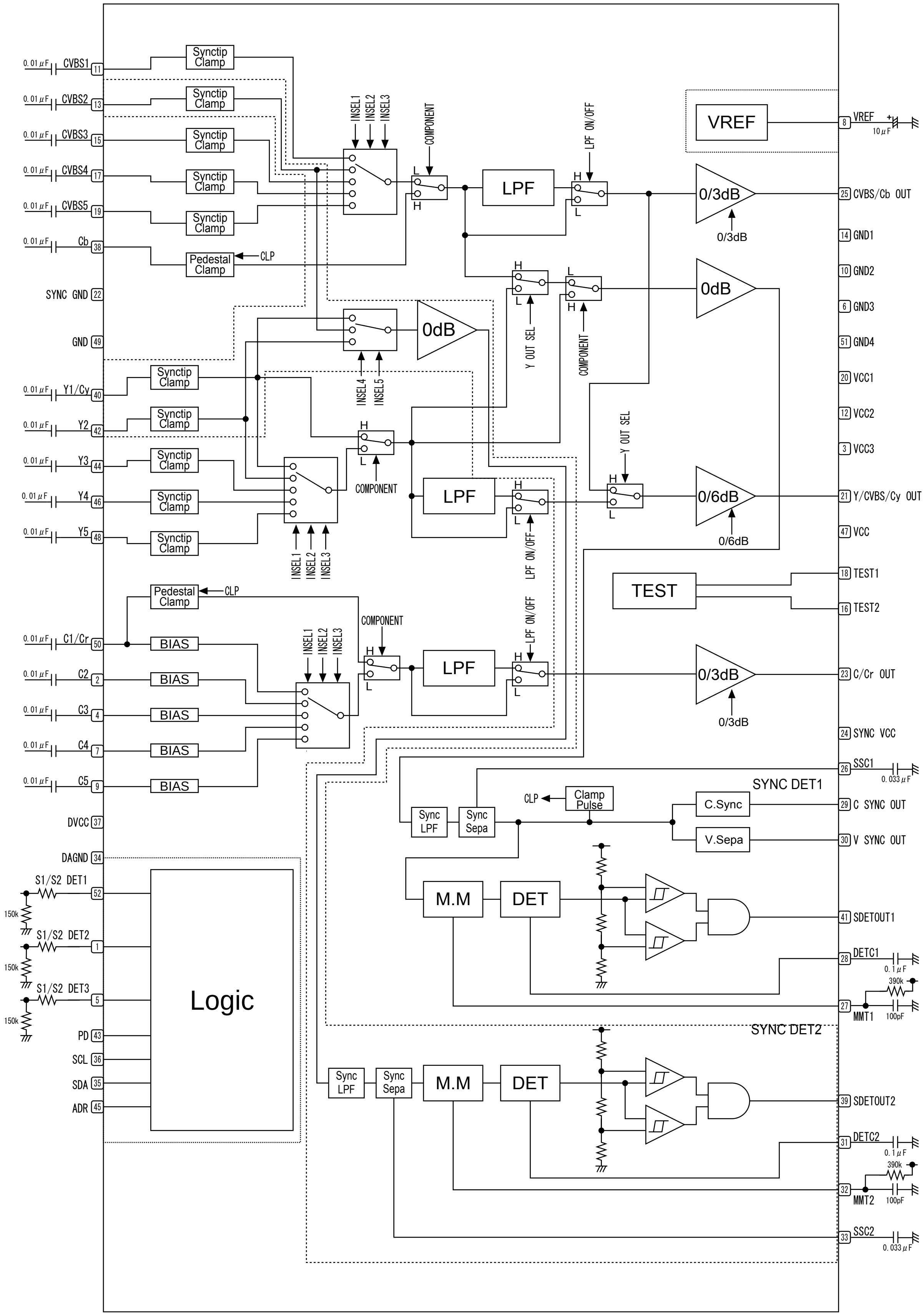


Fig.3

●Description of external components

① Video signal terminal（Clamp terminal）

Use a capacitor above 0.01μF. If a capacitor is too small, a video signal may become distorted.

② Video signal input terminal（Bias terminal）

Input impedance is 20kΩ(TYP) with this terminal. Therefore, set so that a chroma signal may pass fully.

③ S1/S2 DET terminal

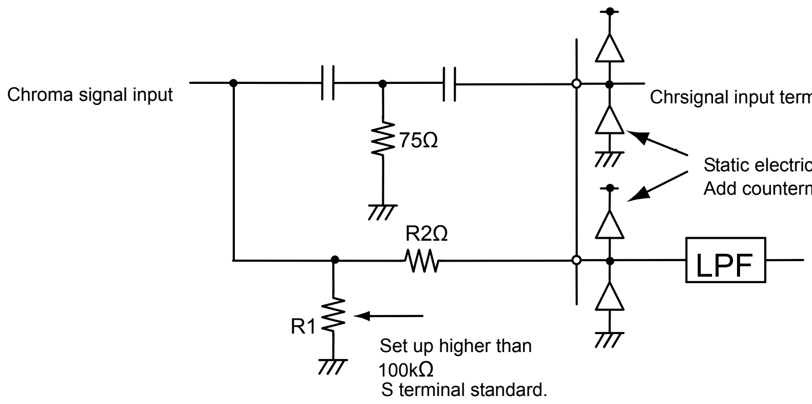


Fig.4

R2: Overvoltage transient can affect the static electricity protection diode connected to the VCC side. Therefore, add a limit current resistor (R2).

④ SSC terminal

This terminal sets the sensitivity of the sync-tip level detection.
When a capacitor is large, sensitivity becomes low, but becomes too sensitive when the capacitor is small.
But, when it is too small, it becomes poor at the noise.

⑤ MMT

Adjusting the value of the outside RC, and duty of the pulse output in DETC is set.
(Pulse can be monitored when the capacitor of DETC is removed.)
Set duty to 50%～60% in the state so that there is no noise in the input signal.
The duty is not equal to the same time constant (RC=constant) when R is small.

⑥ DETC

When a capacitor is small, detection reaction becomes fast, When it is large, detection reaction becomes slow.
Pulse is smoothed by the output impedance of 100kΩ and a capacitor connected to this terminal.
The status of the video signal is monitored by this DC voltage value.

●Reference data

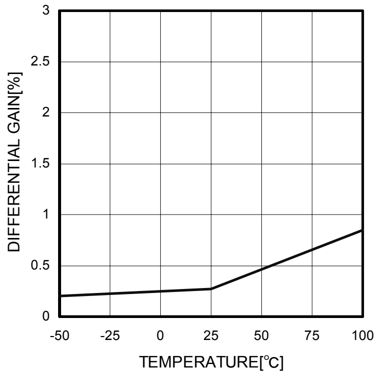


Fig.5 Differential Gain

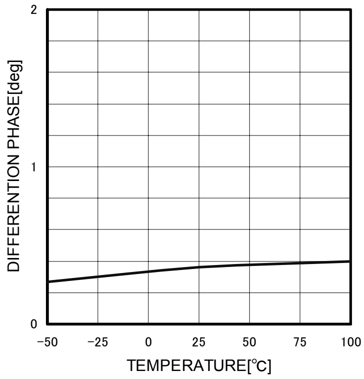


Fig.6 Differential Phase

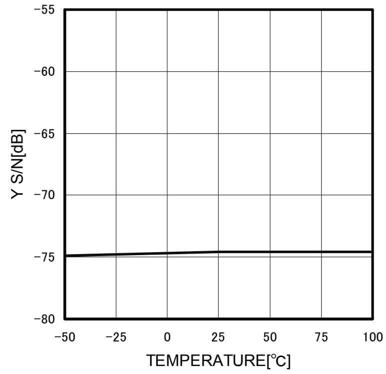


Fig.7 Y S/N ratio

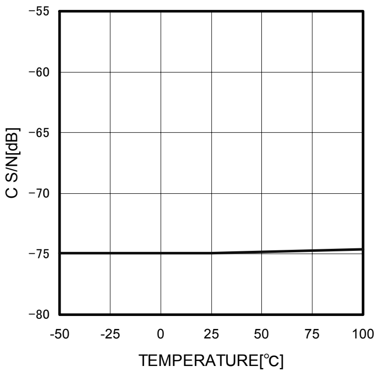


Fig.8 C S/N ratio

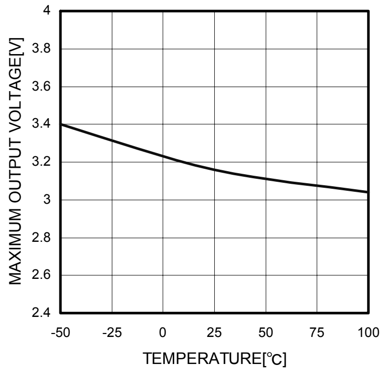


Fig.9 Maximum output voltage
(Temperature dependence)

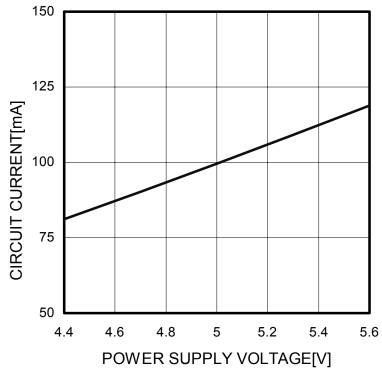


Fig.10 VCC Circuit current
(Supply voltage dependence)

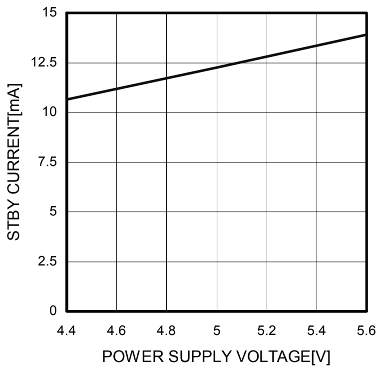


Fig.11 VCC Circuit current (STBY)
(Supply voltage dependence)

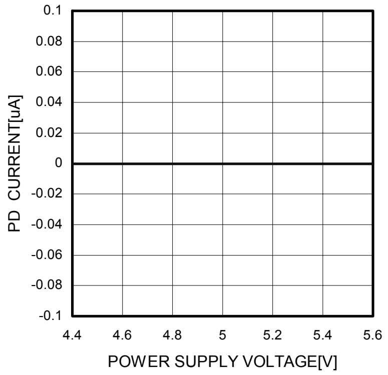


Fig.12 VCC Circuit current (PD)
(Supply voltage dependence)

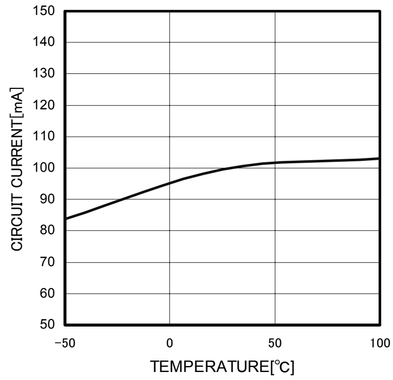


Fig.13 VCC Circuit current
(Temperature dependence)

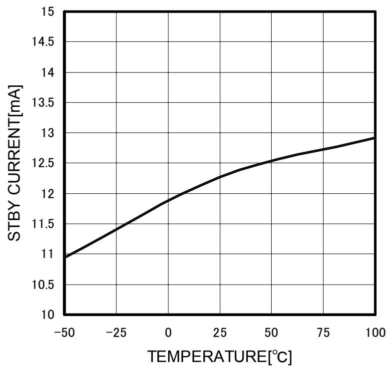


Fig.14 VCC Circuit current
(Temperature dependence)

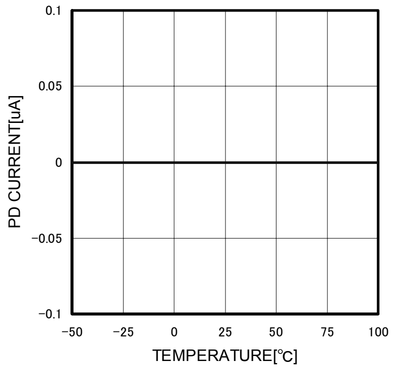


Fig.15 VCC Circuit current PD
(Temperature dependence)

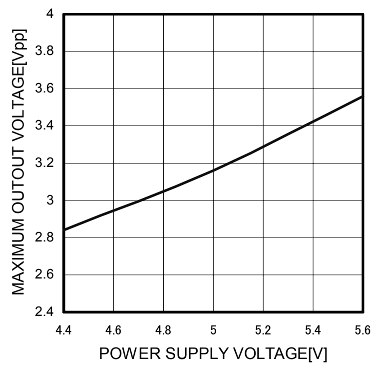


Fig.16 Maximum output voltage
(Supply voltage dependence)

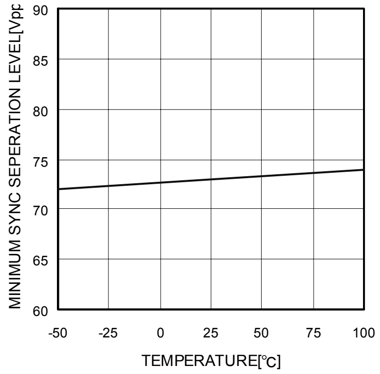


Fig.17 Min synchronous isolation level
(Temperature dependence)

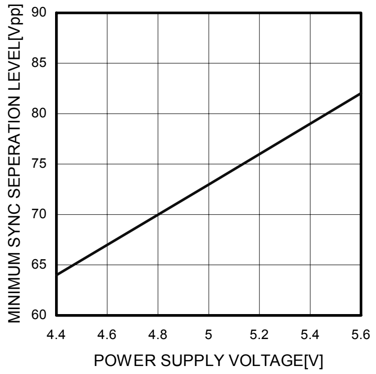


Fig.18 Min synchronous isolation level
(Supply voltage dependence)

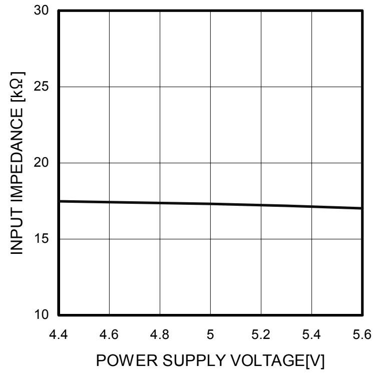


Fig.19 CIN input impedance
(Supply voltage dependence)

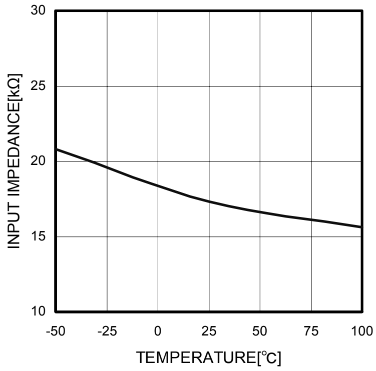


Fig.20 CIN input impedance
(Temperature dependence)

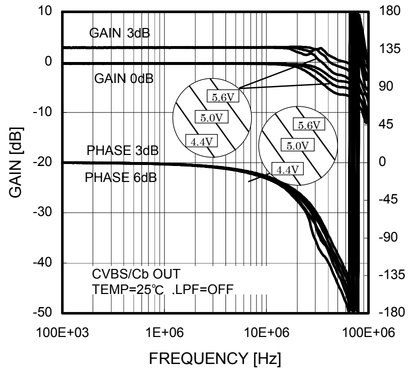


Fig.21 Frequency characteristic
(Supply voltage dependence)

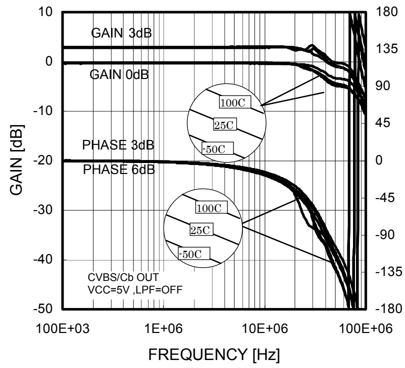


Fig.22 Frequency characteristic
(Temperature dependence)

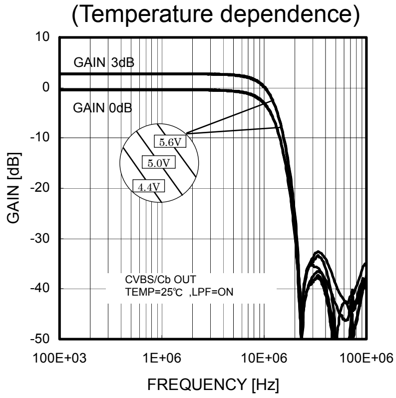


Fig.23 Frequency characteristic
(Supply voltage dependence)

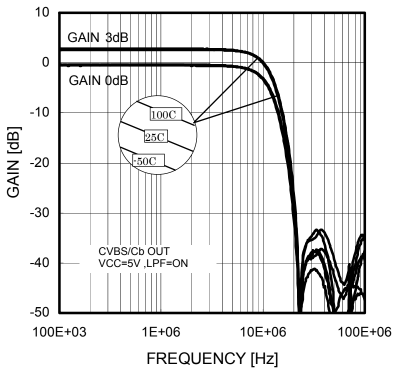


Fig.24 Frequency characteristic
(Temperature dependence)

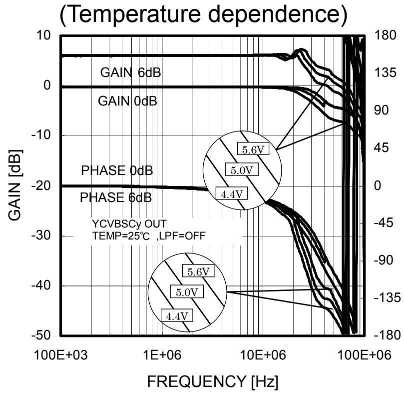


Fig.25 Frequency characteristic
(Supply voltage dependence)

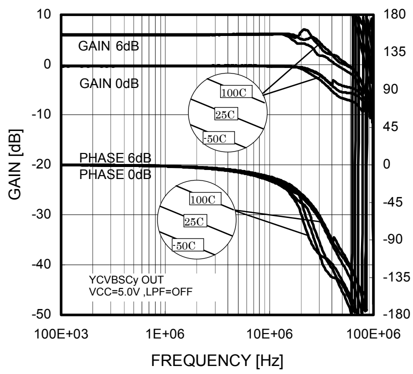


Fig.26 Frequency characteristic
(Temperature dependence)

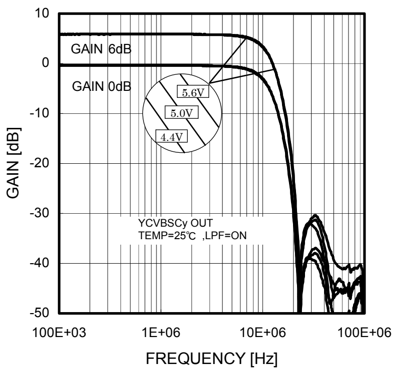


Fig.27 Frequency characteristic
(Supply voltage dependence)

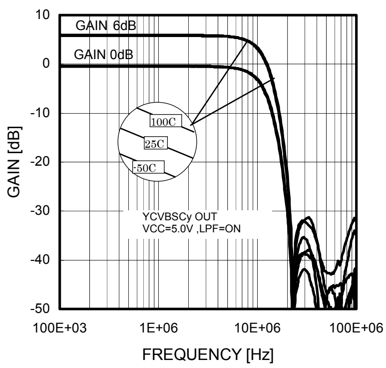


Fig.28 Frequency characteristic
(Temperature dependence)

●**Cautions on use**

1. Numbers and data in entries are representative design values and are not guaranteed values of the items.
2. Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.
3. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
4. GND potential
   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
5. Thermal design
   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.
6. Short circuit between terminals and erroneous mounting
   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
7. Operation in strong electromagnetic field
   Using the ICs in a strong electromagnetic field can cause operation malfunction.
8. Supply voltage of operation
   Although basic circuit function is guaranteed under normal voltage operation (4.75V～5.25V), ensure each parameter complies with appropriate electrical characteristics, when using this device.
9. The outside parts must be layout nearest to the IC and lines from amplifier must be short.
10. The coupling capacitor must be layout nearest to the IC and each pin.
11. VCC for this IC should use the same power source. Impedance should be connected as low as possible for each VCC pin and for each GND pin.

●**Thermal derating characteristics**

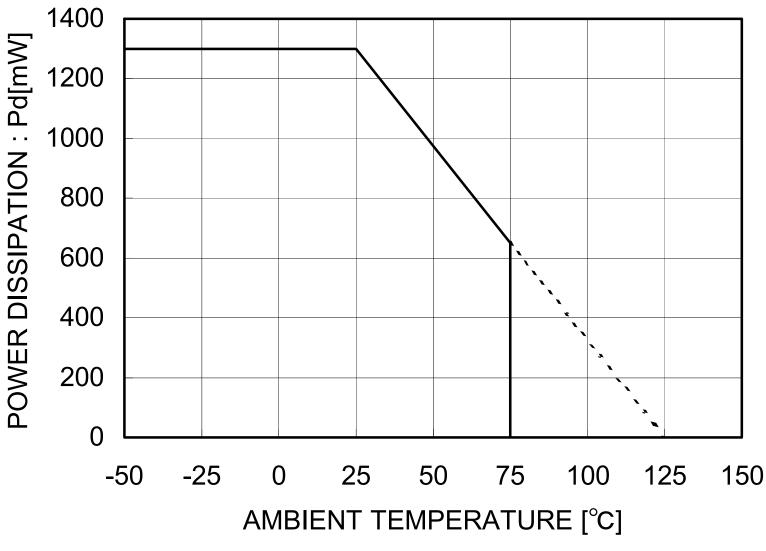


Fig. 29

●Selection of order type

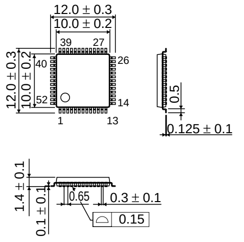
B	H	7	6	2	5	K	S	2

TYPE

BH7625KS2

SQFP-T52

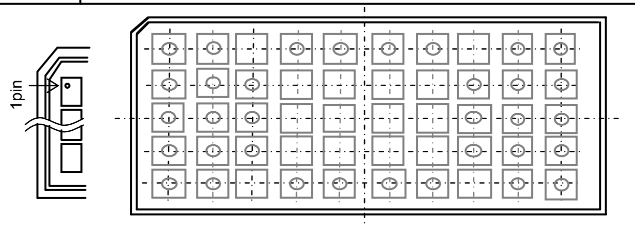
<Dimension>



(Unit:mm)

<Packing information>

Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



※Orders are available in complete units only.

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