

Products	High side switch IC
Туре	BD2061AFJ
Block diagram	Fig. 1
Package	Fig. 4

♦Description

The BD2061AFJ is high side switch IC for Universal Serial BUS (USB) applications. Low ON Resistance and low supply current are realized in this IC. An over-current limit circuit, thermal shutdown circuit, and an under voltage lockout circuit are built-in as protection circuits.

♦Features

Low on resistance 80mΩ MOSFET Switch 1.0A Continuous current load Active "Low" control logic Soft start circuit Over current detection Thermal shutdown Under voltage lockout Open drain error flag output Reverse-current protection when power switch off Power supply voltage range 2.7V~5.5V TTL Enable input 1.2ms typical rise time 1µA Max Standby Current Operating temperature range -40°C~85°C

DESIGN	CHECK	APPROVAL	DATE: JUN. 6 2007	SPECIFICATION No. : TENTATIVE
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♦Absolute maximum ratings

Symbol	Rating	Unit
V _{IN}	-0.3 ~ 6.0	V
V _{/EN}	-0.3 ~ 6.0	V
V _{/OC}	-0.3 ~ 6.0	V
IS _{/OC}	~ 10	mA
V _{OUT}	-0.3 ~ 6.0	V
T _{STG}	-55 ~ 150	°C
PD	560 ^{*1}	mW
	V _{IN} V _{/EN} V _{/OC} IS _{/OC} V _{OUT} T _{STG}	V_{IN} -0.3 ~ 6.0 $V_{/EN}$ -0.3 ~ 6.0 $V_{/OC}$ -0.3 ~ 6.0 $IS_{/OC}$ ~ 10 V_{OUT} -0.3 ~ 6.0 T_{STG} -55 ~ 150

TYPE

*1 In the case of exceeding Ta = 25° C,

4.48mW should be reduced per 1°C.

\diamondsuit Operating conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit
Operating voltage	V _{IN}	2.7	5.0	5.5	V
Operating temperature	T _{OPR}	-40	-	85	°C
Continuous output current	I _{LO}	0	-	1.0	А

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Symbol		Тур.	Max.	Unit	Condition
I _{DD}	-	90	120	μA	V _{/EN} = 0V
I _{STB}	-	0.01	1	μA	V _{/EN} = 5V
V _{/EN}	2.0	-	-	V	High input
	-	-	0.8	V	Low input
V/EN	-	-	0.4	V	Low input 2.7V≦V _{IN} ≦4.5V
I _{/EN}	-1.0	0.01	1.0	μA	$V_{\rm /EN}$ = 0V or $V_{\rm /EN}$ = 5V
V _{OCL}	Ī		0.5	>	I _{/OC} = 5mA
IL _{oc}	-	0.01	1	μA	V _{/OC} = 5V
R _{ON}	-	80	100	mΩ	I _{OUT} = 1.0A
I _{SC}	1.1	1.5	1.9	A	V _{IN} = 5V , V _{OUT} = 0V, C _L = 100µF (RMS)
T _{ON1}	-	1.2	10	ms	$R_L = 5\Omega, C_L = OPEN$
T _{ON2}	-	1.5	20	ms	$R_L = 5\Omega, C_L = OPEN$
T _{OFF1}	-	1	20	μs	$R_L = 5\Omega, C_L = OPEN$
T _{OFF2}	-	3	40	us	$R_L = 5\Omega, C_L = OPEN$
V_{TUVH}	2.1	2.3	2.5	V	Increasing V _{IN}
V_{TUVL}	2.0	2.2	2.4	V	Decreasing V _{IN}
				♦Timing	diagram
S _L				JT 10% ↑ T _{ON2}	TOFF1 90% 90% 10% TOFF2 50%
	V/EN I/EN VOCL ILOC RON ISC TON1 TON2 TOFF1 TOFF2 VTUVH	Image: Name - V/EN - I/EN -1.0 VOCL - ILOC - ILOC - RON - ISC 1.1 TON1 - TOFF1 - TOFF2 - VTUVH 2.1 VTUVL 2.0	$\begin{array}{c c c c c c c } & & & & & & & & \\ \hline V_{IEN} & & & & & & & \\ \hline I_{IEN} & & -1.0 & 0.01 \\ \hline V_{OCL} & & & & & & & \\ \hline V_{OCL} & & & & & & & \\ \hline IL_{OC} & & - & & 0.01 \\ \hline \end{array}$ $\begin{array}{c c c c c c c c c c c c c c c c c c c $	Image - - 0.8 V/EN - - 0.4 I/EN -1.0 0.01 1.0 VOCL - - 0.5 ILOC - 0.01 1 VOCL - - 0.5 ILOC - 0.01 1 VOCL - 0.01 1 RON - 80 100 ISC 1.1 1.5 1.9 TON1 - 1.2 10 TON2 - 1.5 20 TOFF1 - 1 20 TOFF2 - 3 40 VTUVH 2.1 2.3 2.5 VTUVL 2.0 2.2 2.4	$\begin{array}{c c c c c c c c c c c c c c c c c c c $

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◇Block diagram	GND C	UVLC	OCD OUT Charge OCD OUT Gate logic OUT TSD //OC	
<pre>◇Pin description</pre>		F	Fig. 1 Block diagram	
<pre>◇Pin description</pre> Pin No.	Pin Name	F I/O	Fig. 1 Block diagram	
	Pin Name GND	1/O		
Pin No.		1/0 1 1	Function	r supply input
Pin No.	GND		Function Ground Power supply input. Input terminal to the power switch and power	r supply input
Pin No. 1 2, 3	GND	1/O 1 1 1	Function Ground Power supply input. Input terminal to the power switch and power terminal of the internal circuit. Enable input.	

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♦I/O circuit				
	Pin Name	Pin No.	Equivalent circuit	
	/EN	4		
	/OC	5		
	OUT	6, 7, 8		
	$\langle \langle$	Fig. 2 1	erminal circuit	



♦ Operations Explanation

1. Over current detection circuit (OCD)

The overcurrent detection circuit limits the current and outputs an error flag when the current flowing in each switch MOSFET exceeds a specified value.

TYPE

The over current detection circuit works when the switch is on (/EN signal is active).

2. Thermal shutdown circuit(TSD)

The thermal shutdown circuit turns off the switch and outputs an error flag when the junction temperature exceeds 140°C (typ.). When the thermal shutdown is activated, the switch turns off and error flag is output.

The thermal shut down circuit works when the switch is on (/EN signal is active).

3. Under voltage lockout(UVLO)

UVLO circuit prevents the switch from turning on until the V_{DD} exceeds 2.3V(Typ.). If the V_{IN} drops below 2.2V(Typ.) while the switch turns on, then UVLO shuts off the power switch. UVLO has hysteresis of a 100mV(Typ).

Under voltage lockout circuit works when the switch is on (/EN signal is active).

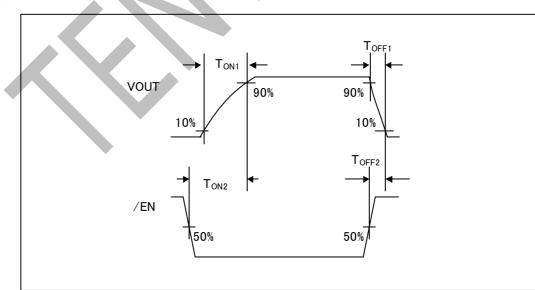
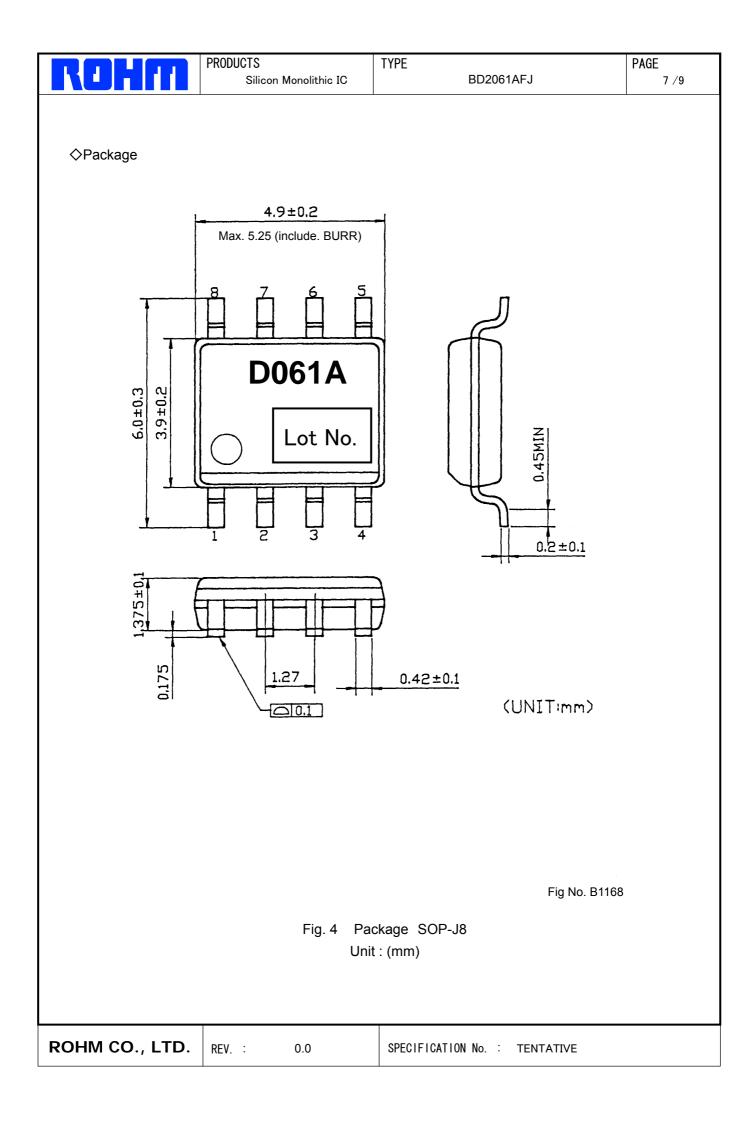


Fig. 3 Timing chart at rise / fall time of switch.





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Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

TYPE

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 140°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

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